

Signetics

Memories – Bipolar F.P.L.A.

N92S100, N82S101 Bipolar Field Programmable Logic Array (16 x 48 x 8)

GENERAL DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (F_p), or true active-low (F_p^*). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range 0°C to +75°C specify N82S100/101, I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101.I.

APPLICATIONS

- CRT display systems
- Random logic
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Sequential controllers
- Data security encoders
- Fault detectors
- Frequency synthesizers

MAXIMUM RATINGS

PARAMETER	RATING		UNIT
	Min	Max	
VCC Supply voltage		+7	Vdc
VIN Input voltage		+5.5	Vdc
VOU Output voltage		+5.5	Vdc
IIN Input currents	-30	+30	mA
IOUT Output currents		+100	mA
TA Temperature range			°C
	Operating		
TSTG Storage			
	N82S100/101	0	+75
	S82S100/101	-55	+125
		-65	+150

LOGIC FUNCTION

Typical Product Term:

$$P_0 = I_0 \cdot I_1 \cdot \overline{I_2} \cdot I_5 \cdot \overline{I_{13}}$$

Typical Output Functions

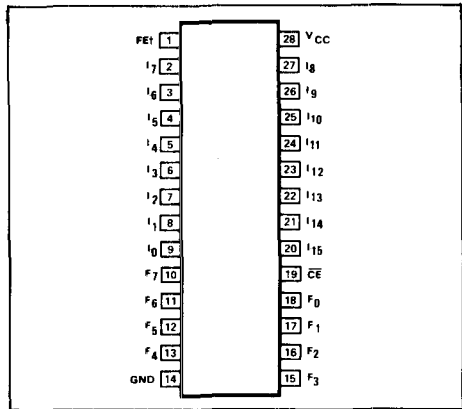
$$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2) @ S = \text{Closed}$$

$$F_0^* = (\overline{CE}) + (P_0 \cdot P_1 \cdot P_2) @ S = \text{Open}$$

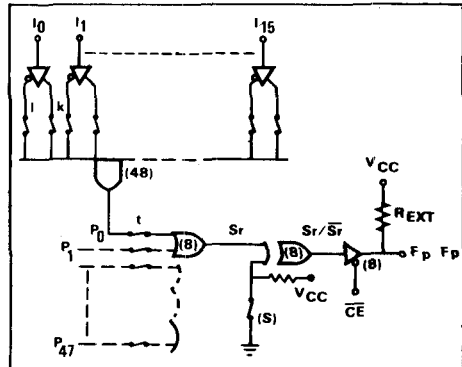
NOTE

For each of the 8 outputs, either the function F_p (active-high) or F_p^* (active low) is available, but not both. The required function polarity is programmed via link (S).

CONNECTION DIAGRAM



FPLA EQUIVALENT LOGIC PATH



TRUTH TABLE

MODE	Pn	CE	Sr	f(Pn)	Fp	Fp*
Disabled (82S101)					1	1
Disabled (82S100)	X	1	X		Hi-Z	Hi-Z
Read	1	0	Yes		1	0
	0	0	No		0	1
	X	0	No		0	1

REFERENCE TABLE

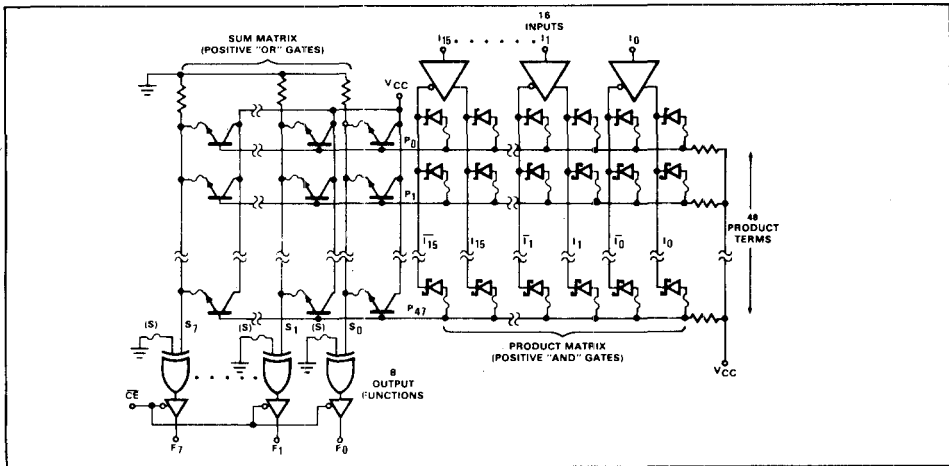
TYPE NO.	STOCK NO.	OUTLINE DRWG. NO.
N82S100N	56355R	5
N82S101N	56356G	5

ITT GEMINI

FOR CURRENT PRICES PHONE HARLOW (0279) 29644

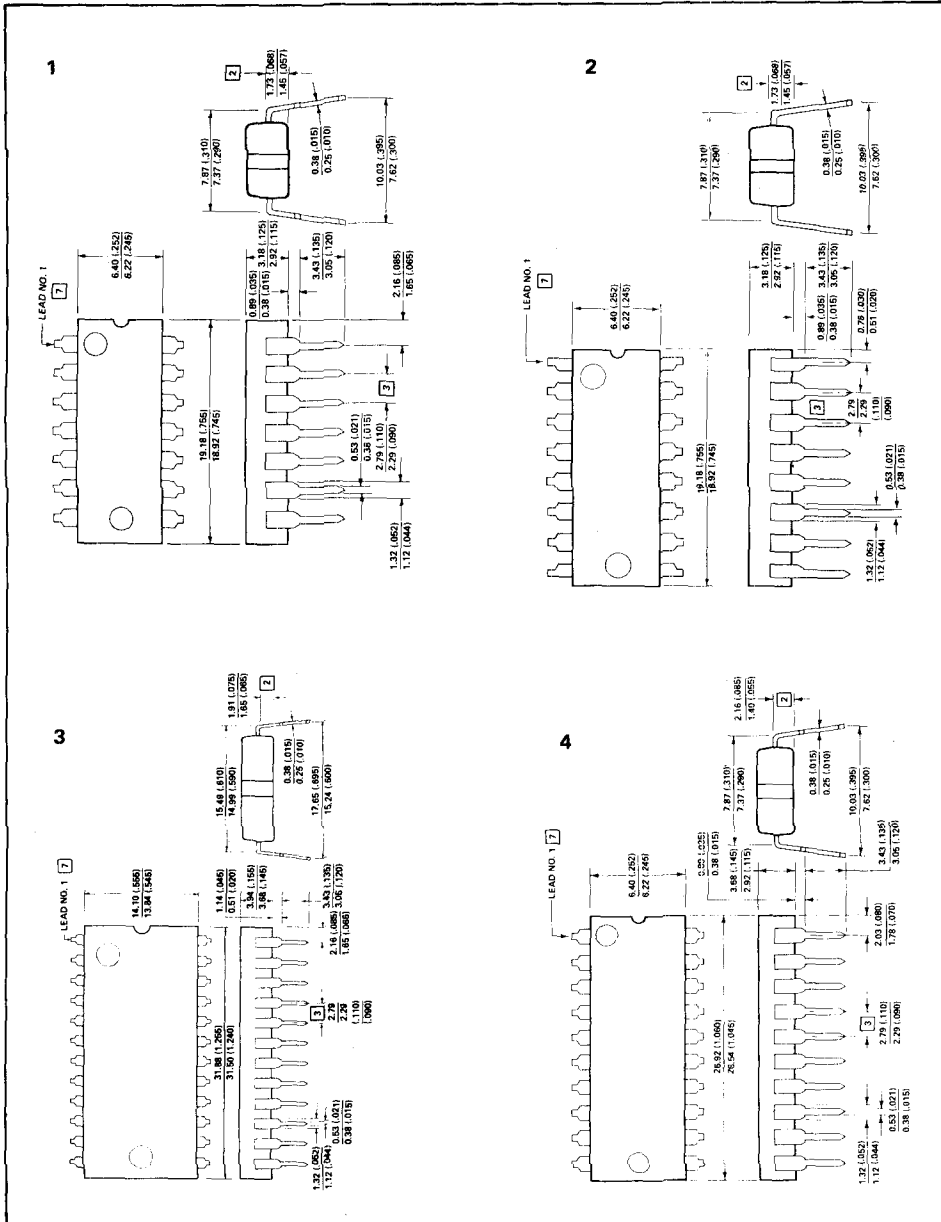
N82S100, N82S101 *Cont.*

LOGIC DIAGRAM



PLEASE QUOTE STOCK NO.
AND MANUFACTURERS PART NO. WHEN ORDERING



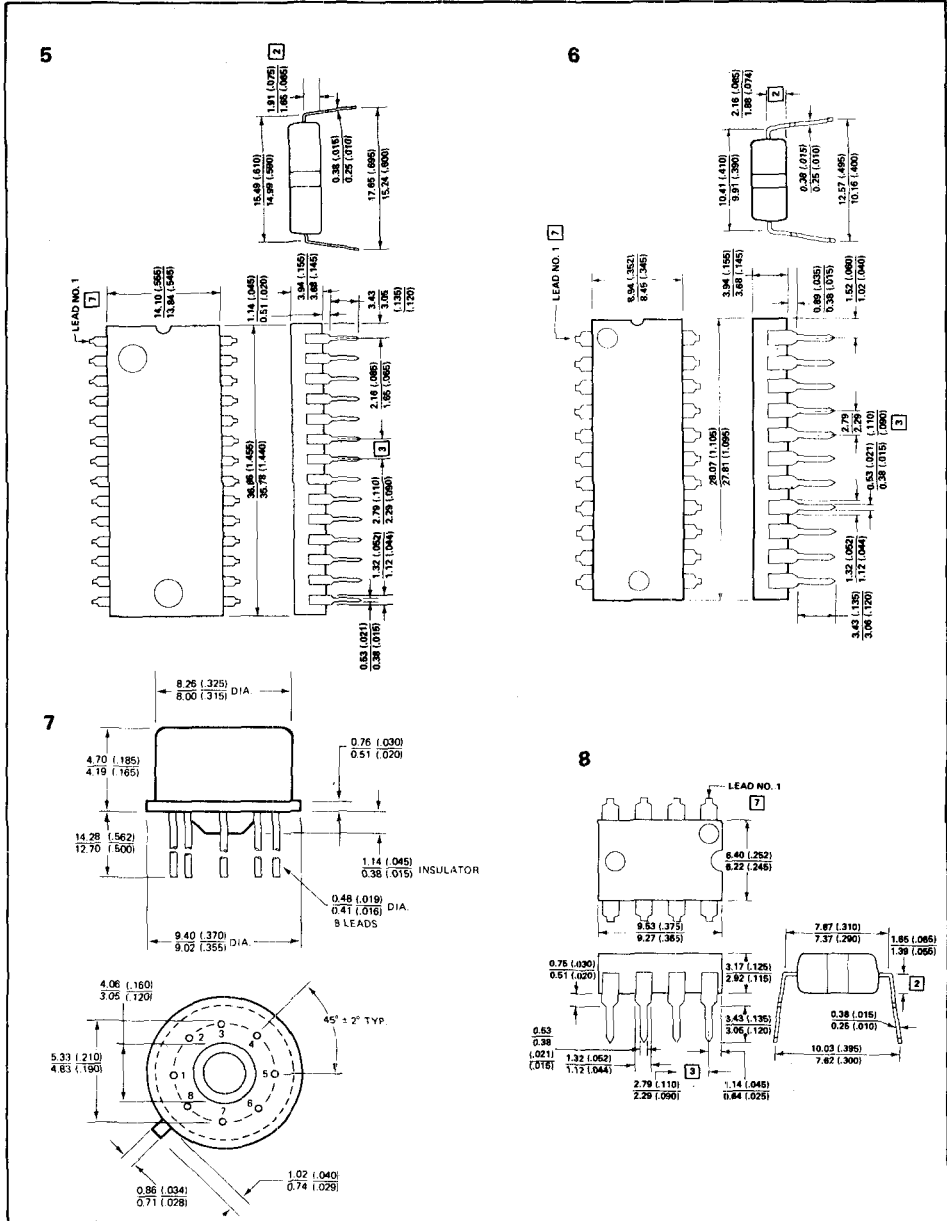


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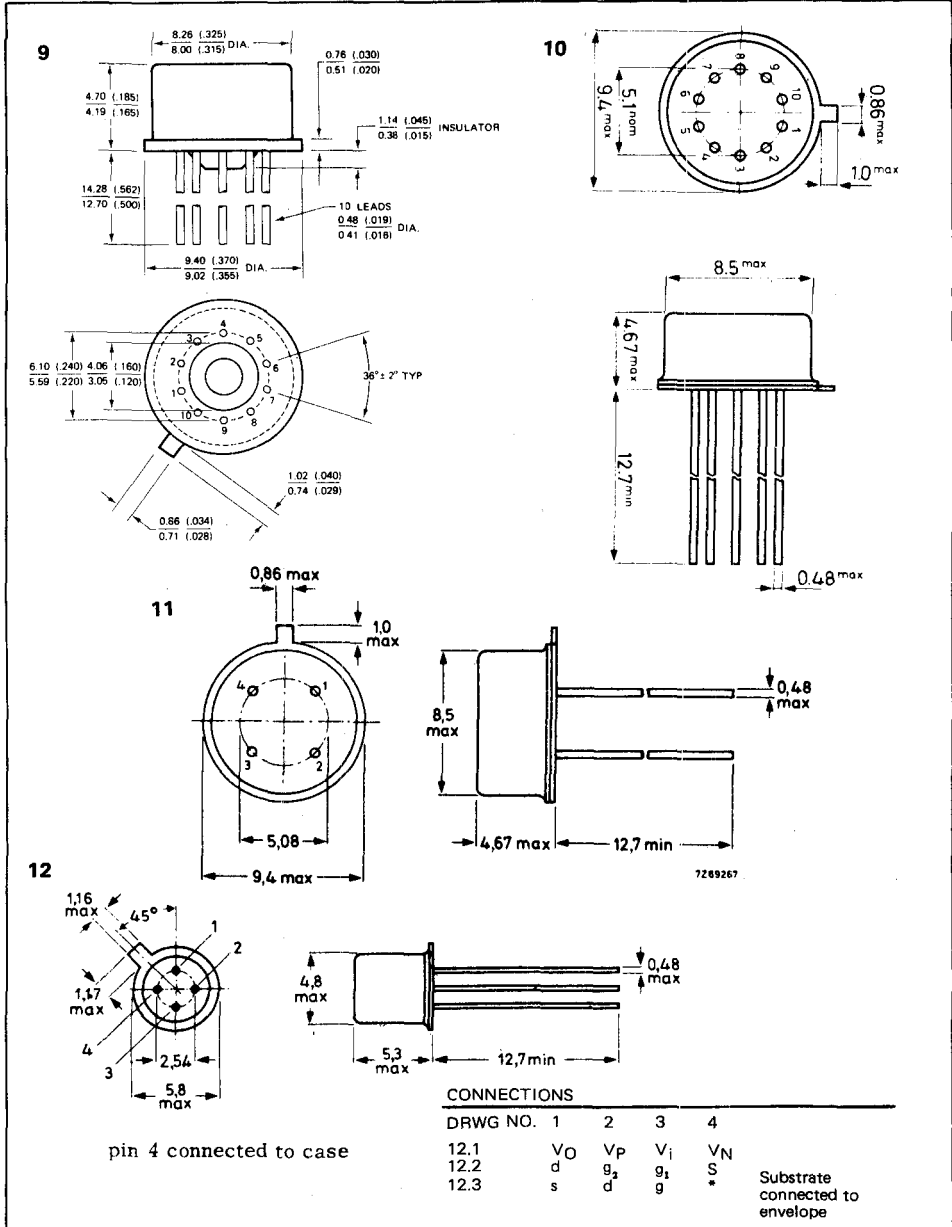
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Outline Drawings



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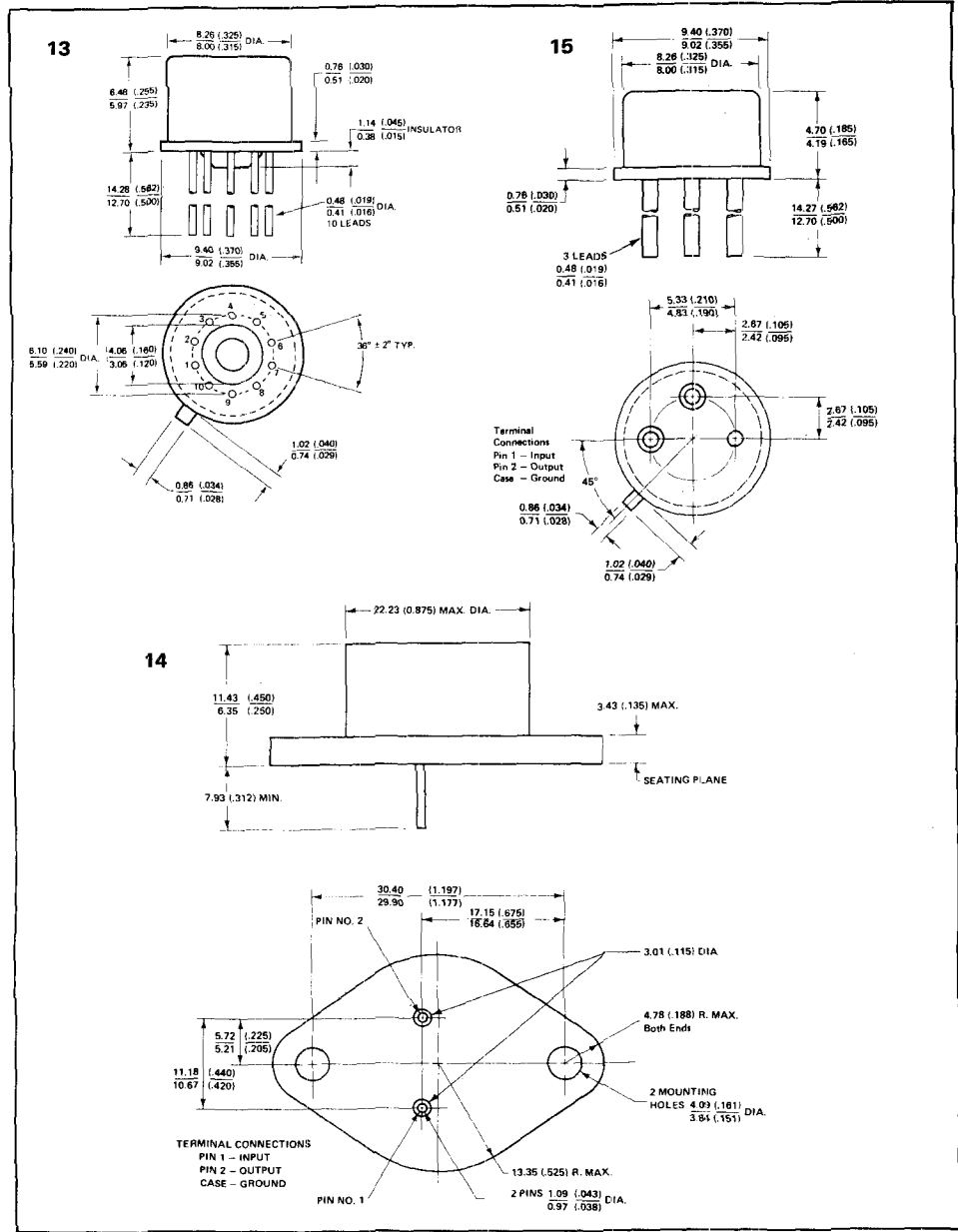


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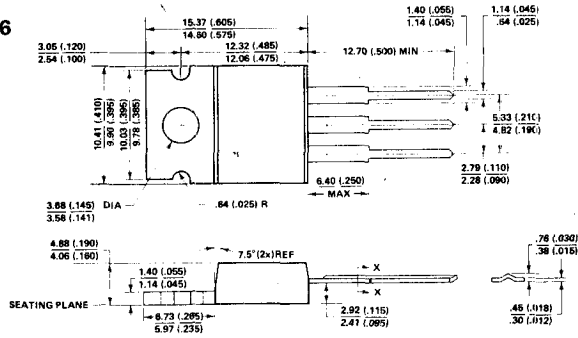
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Outline Drawings

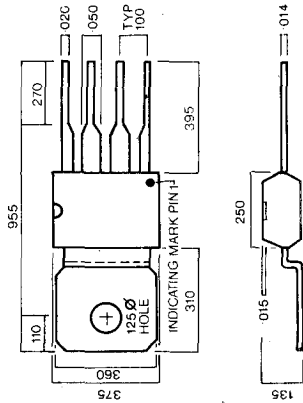


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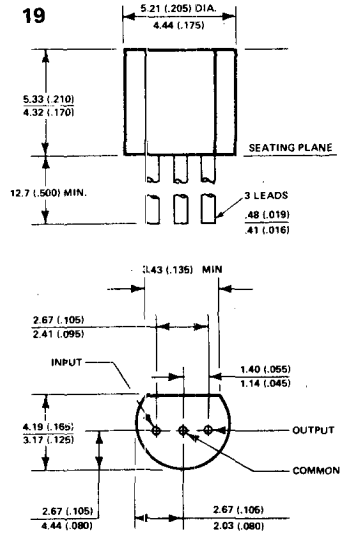
16



17



19



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