

3N165, 3N166 Dual P-Channel Enhancement Mode MOS FET

FEATURES

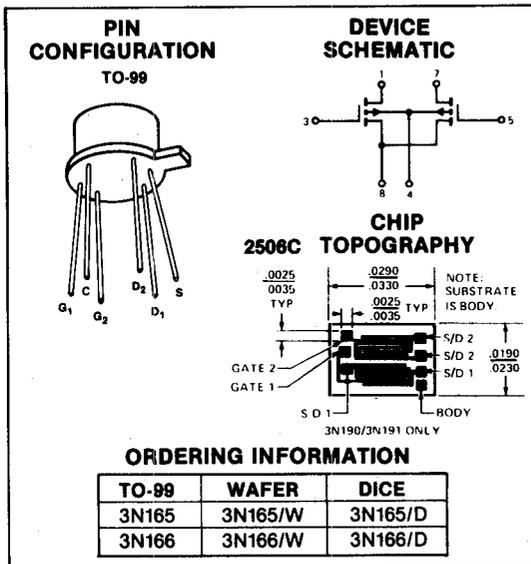
- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance

MAXIMUM RATINGS (@ 25°C ambient unless noted)

| | | |
|---------------------------------|---|---------------|
| V _{GSS} | Static Gate to Source Voltage | ±40V |
| V _{GSS} ⁽¹⁾ | Transient Gate to Source Voltage | ±125V |
| V _{DSS} | Drain to Source Voltage | -40V |
| V _{GDS} | Source to Drain Voltage | -40V |
| V _{GG} | Gate to Gate | ±80V |
| V _G | Any Lead to Case | ±40V |
| I _D | Drain Current | 50 mA |
| P _D | Power Dissipation (each side) | 300 mW |
| | (both sides) | 525 mW |
| | Total Derating Factor | 4.2 mW/°C |
| T _J | Operating Junction Temperature | -55 to +150°C |
| T _{stg} | Storage Temperature | -65 to +200°C |
| T _L | Lead Temperature 1/16" from Case for 10 sec max | +300°C |

⁽¹⁾ Devices must not be tested at ±125V more than once or for longer than 300 ms.

NOTE: See handling precautions on 3N170 data sheet.



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ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

| | MIN | MAX | UNITS | TEST CONDITIONS | |
|----------------------|---------------------------------------|------|-------|--|--|
| I _{GSS} | Gate Reverse Leakage Current | 10 | pA | V _{GS} = 40V | |
| I _{G(f)} | Gate Forward Leakage Current | -10 | pA | V _{GS} = -40V | |
| I _{G(f)} | Gate Forward Leakage Current (+125°C) | -25 | pA | V _{GS} = -40V | |
| I _{DSS} | Drain to Source Leakage Current | -200 | pA | V _{DS} = -20V | |
| I _{SDS} | Source to Drain Leakage Current | -400 | pA | V _{SD} = -20, V _{DB} = 0 | |
| I _{D(on)} | On Drain Current | -5 | -30 | mA | V _{DS} = -15V, V _{GS} = -10V |
| V _{GS(th)} | Gate Source Threshold Voltage | -2 | -5 | V | V _{DS} = -15V, I _D = -10μA |
| V _{GS(th)} | Gate Source Threshold Voltage | -2 | -5 | V | V _{DS} = V _{GS} , I _D = -10μA |
| r _{fs(on)} | Drain Source On Resistance | | 300 | ohms | V _{GS} = -20V, I _D = -100μA |
| g _{fs} | Forward Transconductance | 1500 | 3000 | μmhos | V _{DS} = -15V, I _D = -10mA, f = 1kHz |
| g _{os} | Output Admittance | | 300 | μmhos | V _{DS} = -15V, I _D = -10mA, f = 1kHz |
| C _{iss} | Input Capacitance | | 3.0 | pF | V _{DS} = -15V, I _D = -10mA, f = 1MHz |
| C _{rss} | Reverse Transfer Capacitance | | 0.7 | pF | V _{DS} = -15V, I _D = -10mA, f = 1MHz |
| C _{oss} | Output Capacitance Input Shorted | | 3.0 | pF | V _{DS} = -15V, I _D = -10mA, f = 1MHz |
| Re(Y _{fs}) | Real Part Forward Transconductance | | 1200 | μmhos | V _{DS} = -15V, I _D = -10mA, f = 100MHz |

MATCHING CHARACTERISTICS 3N165

| | MIN | MAX | UNITS | TEST CONDITIONS | |
|------------------------------------|--|------|-------|-----------------|--|
| Y _{fs1} /Y _{fs2} | Forward Transconductance Ratio | 0.90 | 1.0 | | V _{DS} = -15V, I _D = -1500μA, f = 1KHz |
| V _{GS1-2} | Gate-Source Threshold Voltage Differential | | 100 | mV | V _{DS} = -15V, I _D = -500μA |
| ΔV _{GS1-2} | Gate Source Threshold Voltage Differential Change with Temperature | | 8 | mV | V _{DS} = -15V, I _D = -500μA T = -55°C to +25°C |
| ΔV _{GS1-2} | Gate-Source Threshold Voltage Differential Change with Temperature | | 10 | mV | V _{DS} = -15V, I _D = -500μA T = +25°C to +125°C |