INTERSIL

LM114/H, LM114A/AH Dual NPN Monolithic Transistor

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GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Collector-base capacitance is only ≈ 100pF at 5V.

ABSOLUTE MAXIMUM RATINGS

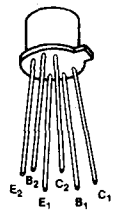
Collector-Base Voltage (BV_{CBO})	45V
Collector-Emitter Voltage (BV_{CER})	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (BV_{EBO})	6V
Collector Current	20mA
Total Power Dissipation (Note 1)	0.8W
Operating Junction Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

FEATURES

- Low offset voltage — 0.5mV maximum
- Low drift — 2μV/°C maximum from −55°C to +125°C
- High current gain — 500 minimum at 10μA
- Tight beta match — 10% maximum
- High breakdown voltage — to 60V
- Matching guaranteed over a 0V to 45V collector-base voltage range
- CMRR > 100dB

PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

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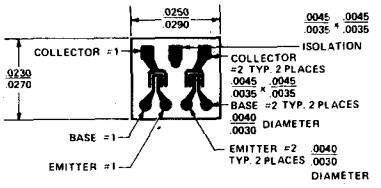

ORDERING INFORMATION

TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MAXIMUM LIMITS LM114A, AH	MAXIMUM LIMITS LM114, H	UNITS
Offset Voltage	$1\mu A \le I_C \le 100\mu A$	0.5	2.0	mV
Offset Current	$I_C = 10\mu A$	2.0	10	nA
	$I_C = 1\mu A$	0.5		nA
Bias Current	$I_C = 10\mu A$	20	40	nA
	$I_C = 1\mu A$	3.0		nA
Offset Voltage Change	$0V \le V_{CB} \le V_{MAX}$, $I_C = 10\mu A$	0.2	1.5	mV
Offset Current Change	$0V \le V_{CB} \le V_{MAX}$, $I_C = 10\mu A$	1.0	4.0	nA
Offset Voltage Drift	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	2.0	10	μV/°C
Offset Current	$-55°C \le T_A \le +125°$, $I_C = 10\mu A$	12	50	nA
Bias Current	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	60	150	nA
Collector-Base Leakage Current	$V_{CB} = V_{MAX}$			
	$T_A = +25°C$	10	50	pA
	$T_A = +125°C$	10	50	nA
Collector-Emitter Leakage Current	$V_{CE} = V_{MAX}$, $V_{EB} = 0V$			
	$T_A = +25°C$	50	200	pA
	$T_A = +125°C$	50	200	nA
Collector-Collector Leakage Current	$V_{CC} = V_{MAX}$			
	$T_A = +25°C$	100	300	pA
	$T_A = +125°C$	100	300	nA

Note 1: The maximum dissipation given is for a +25°C case temperature. For operation under other conditions, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +70°C/W junction to case of +230°C/W junction to ambient.

Note 2: These specifications apply for T_A = +25°C and $0V \le V_{CB} \le V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, V_{MAX} 30V.