INTERSIL

2N4117-19, 2N4117A-19A
N-Channel JFET

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FEATURES

- Low Leakage – $I_{GSS} < 1$ pA
- Low Capacitance – $C_{rss} < 1.5$ pF

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	300°C

Maximum Power Dissipation

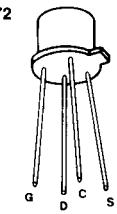
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS} Gate to Source Voltage	-40 V
V_{GD} Gate to Drain Voltage	-40 V
I_G Gate Current	50 mA

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

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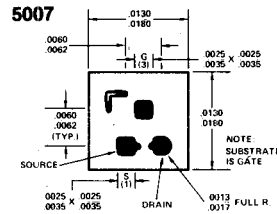

ORDERING INFORMATION

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	2N4117A/W	2N4117A/D
2N4118	2N4118/W	2N4118/D
2N4118A	2N4118A/W	2N4118A/D
2N4119	2N4119/W	2N4119/D
2N4119A	2N4119A/W	2N4119A/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		-10		-10		-10	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
I_{GSS} (+100°C)	Gate Reverse Current		-25		-25		-25	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
V_{GS} (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	$V_{DS} = 10$ V, f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	60		70		90		μmho	$V_{GS} = 0$, f = 30 MHz
g_{os}	Common-Source Output Conductance		3		5		10	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		3		3		3	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.