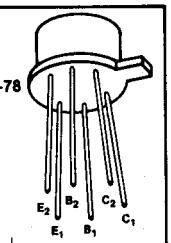
INTERSIL

2N5117-2N5119
Dual Monolithic PNP Transistor

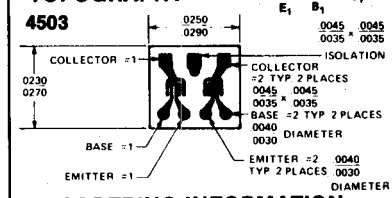
ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise noted) (Note 1)

Dissipation at 25°C Case Temperature	
Each side (Note 1)	0.4W
Both sides	0.75W
Derating Factor	
Each side	2.3mW/°C
Both sides	4.3mW/°C
Voltage	
Collector to Base	45V
Collector to Emitter	45V
Emitter to Base (Note 2)	7.0V
Collector to Collector	100V
Collector Current	10mA
Storage Temperature	−65 to +200°C
Lead Temperature for 10 Seconds	+300°C

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 2N5118		2N5119		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
h_{FE}	DC Current Gain	100	300	50			I_C = 10 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain	100		50			I_C = 500 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain (−55°C)	30		20			I_C = 10 μA, V_{CE} = 5.0 V	
I_{CBO}	Collector Cutoff Current		0.1		0.1	nA	I_E = 0, V_{CB} = 30 V	
I_{CBO}	Collector Cutoff Current (150°C)		0.1		0.1	μA	I_E = 0, V_{CB} = 30 V	
I_{EBO}	Emitter Cutoff Current		0.1		0.1	nA	I_C = 0, V_{EB} = 5.0 V	
$I_{C_1-C_2}$	Collector-Collector Leakage		5.0		5.0	pA	V_{CC} = 100 V	
GBW	Current Gain Bandwith Product	100		100		MHz	I_C = 500 μA, V_{CE} = 10 V	
C_{ob}	Output Capacitance		0.8		0.8	pF	I_E = 0, V_{CB} = 5.0 V	
C_{te}	Emitter Transition Capacitance		1.0		1.0	pF	I_C = 0, V_{EB} = 0.5 V	
$C_{C_1-C_2}$	Collector-Collector Capacitance		0.8		0.8	pF	V_{CC} = 0	
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	I_C = 1.0 mA, I_B = 0	
NF	Narrow Band Noise Figure		4.0		4.0	dB	I_C = 10 μA, V_{CE} = 5.0 V BW = 200 Hz	f = 1 KHz, R_G = 10 KΩ
$V_{(BR)CBO}$	Collector Base Breakdown Voltage	45		45		V	I_C = 10 μA, I_E = 0	
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage	7.0		7.0		V	I_E = 10 μA, I_C = 0	

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117		2N5118		2N5119		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1.0	0.85	1.0	0.8	1.0		I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$V_{BE_1}-V_{BE_2}$	Base-Emitter Voltage Differential		3.0		5.0		5.0	mV	I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$I_{B_1}-I_{B_2}$	Base Current Differential		10.0		15		40	nA	I_C = 10 μA, V_{CE} = 5.0 V	
$\Delta(V_{BE_1}-V_{BE_2})$	Base Voltage Differential Change with Temperature		3.0		5.0		10	μV/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = −55°C to +125°C
$\Delta(I_{B_1}-I_{B_2})$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	nA/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = −55°C to +125°C

1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200°C.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.