INTERSIL

2N5911, 2N5912
IT5911, IT5912
Dual Monolithic N-Channel JFET

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FEATURES

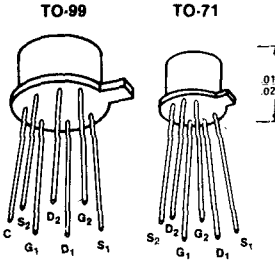
- Tracking < 20 μV/°C
- g_{fs} < 5000 μmho, 0 –100 MHz
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, I_G, g_{fs}

ABSOLUTE MAXIMUM RATINGS

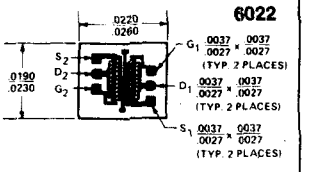
@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	–25V
Gate Current	50 mA
Device Dissipation (Each Side),	367 mW
Linear Derating	3 mW/°C
Total Device Dissipation,	500 mW
Linear Derating	4 mW/°C
Storage Temperature Range	–65°C to +200°C

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		–100	pA	V_{GS} = –15 V, V_{DS} = 0	
			–250	nA		150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1	–5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	–0.3	–4		V_{DG} = 10 V, I_D = 5 mA	
I_G	Gate Operating Current		–100	pA		
			–100	nA		125°C
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
g_{os}	Common-Source Output Conductance		100			f = 1 kHz
g_{oss}	Common-Source Output Conductance		150			f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz, R_G = 100KΩ

	PARAMETER	IT, 2N5911 MIN	IT, 2N5911 MAX	IT, 2N5912 MIN	IT, 2N5912 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 μs, duty cycle ≤ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			20		40			T_A = –55°C, T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz