INTERSIL

U257
Dual Monolithic N-Channel JFET

FEATURES

- $g_{fs} > 5000\ \mu mho$ from dc to 100 MHz
- Matched V_{GS}, g_{fs} and g_{os}

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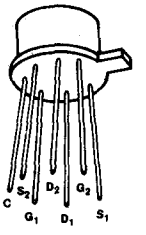
ABSOLUTE MAXIMUM RATINGS
@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 3.85 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 7.7 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C

PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

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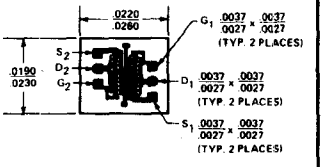

ORDERING INFORMATION

TO-99	WAFER	DICE
U257	U257/W	U257/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−100	pA	V_{GS} = 15 V, V_{DS} = 0	
			−250	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−5		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\overline{e_n}$	Equivalent Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 1)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.85	1			f = 1 kHz
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.