INTERSIL

J174-J177
P-Channel JFET

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

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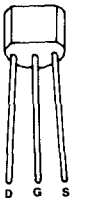
FEATURES
- Low Insertion Loss
  r_{ds} (on) < 85Ω (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)}$ < 5.5 pF
  $C_{dg(off)}$ < 5.5 pF
- Fast Switching
  $t_{d(on)} + t_r$ = 7 ns Typical

PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

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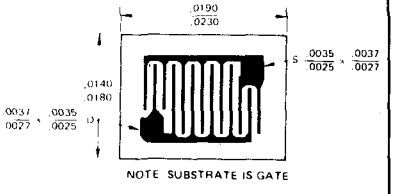

ORDERING INFORMATION

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current ..... 50 mA
Total Device Dissipation (25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... −55 to +125°C
Operating Temperature Range ..... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J174 MIN	J174 TYP	J174 MAX	J175 MIN	J175 TYP	J175 MAX	J176 MIN	J176 TYP	J176 MAX	J177 MIN	J177 TYP	J177 MAX	UNIT	TEST CONDITIONS	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = −15V, I_D = −10nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	−20		−100	−7		−60	−2		−25	−1.5		−20	mA	V_{DS} = −15V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 2)			−1			−1			−1			−1	nA	V_{DS} = −15V, V_{GS} = 10V	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = −0.1V	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance		40			40			40			40		pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		5			10			20			25		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		5			10			15			20		ns		
13	DYNAMIC	t_f	Fall Time		10			20			20			25		ns		

	J174	J175	J176	J177
V_{DD}	−10V	−6V	−6V	−6V
$V_{GS(off)}$	12V	8V	6V	3V
R_L	560Ω	12KΩ	5.6KΩ	10KΩ
$V_{GS(on)}$	0V	0V	0V	0V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration ~300μs; duty cycle ≤ 3%.