

# INTEGRATED CIRCUITS LIST OF COMPARABLE TYPES T T L RANGE

## COMMERCIAL VERSIONS

<i>Type No.</i>	<i>Mullard types</i>	<i>Type No.</i>	<i>Mullard types</i>
7400N	FJH131	7454N	FJH181
7401N	FJH231	7460N	FJY101
7401AN	FJH311	7470N	FJJ101
7402N	FJH221	7472N	FJJ111
7403N	FJH291	7473N	FJJ121
7403AN	FJH301	7474N	FJJ131
7404N	FJH241	7475N	FJJ181
7405N	FJH251	7476N	FJJ191
7405AN	FJH321	7480N	FJH191
7410N	FJH121	7482N	FJH201
7420N	FJH111	7490N	FJJ141
7430N	FJH101	7491AN	FJJ151
7440N	FJH141	7492N	FJJ251
7441AN	FJL101	7493N	FJJ211
7442N	FJH261	7496N	FJJ241
7450N	FJH151	74107N	FJJ261
7451N	FJH161	74121N	FJK101
7453N	FJH171		
<i>Type No.</i>	<i>Mullard types</i>	<i>Type No.</i>	<i>Mullard types</i>
6400N	FJH136	6453N	FJH176
6410N	FJH126	6454N	FJH186
6420N	FJH116	6460N	FJY106
6430N	FJH106	6470N	FJJ106
6440N	FJH146	6472N	FJJ116
6450N	FJH156	6473N	FJJ126
6451N	FJH166	6474N	FJJ136
		6476N	FJJ196

There is also a limited range of devices available in the '2' series (extended temperature range —55 to +125°C).

# T.T.L. SINGLE 8-INPUT NAND GATES

# FJH101 FJH101A FJH106

Correspond to 74 Series types 7430N, 6430N

## TENTATIVE DATA

These devices are transistor-transistor logic single 8-input NAND gates in the FJ series of integrated circuits. The FJH101 corresponds to '74 Series' type 7430N, the FJH106 corresponds to '64 Series' type 6430N.

QUICK REFERENCE DATA			
Supply voltage (nominal)		5.0	V
Fan-out (max.)		10	
Noise immunity (typ.)		1.0	V
		0.4	V
Operating temperature range	FJH101/1A	0 to +70	<sup>o</sup> C
	FJH106	-40 to +85	<sup>o</sup> C
Propagation delay (typ.)		13	ns
Average power dissipation (50% duty cycle, $T_{amb} = 25^{\circ}C$ )		10	mW
Fan-in		8	

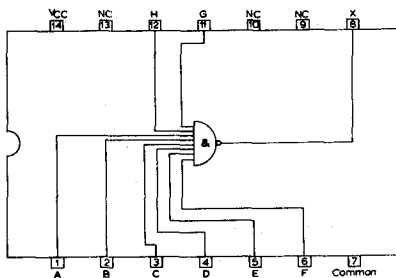
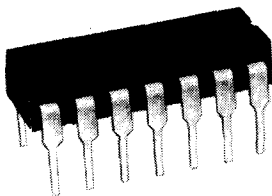
## OUTLINE

Conforms to J.E.D.E.C. TO-116 (see page 4)

FJH101 - 14-lead all plastic dual-in-line package

FJH101A - 14-lead hermetic-in-plastic dual-in-line package

FJH106 - 14-lead all plastic dual-in-line package



## LOGIC FUNCTION

The logic function of the gate is a NAND when the most positive signal voltage is a '1' and a NOR when the most positive signal voltage is a '0'. All inputs to the gate are to be 'High' in order for the output to be 'Low'. A 'Low' input to any gate input will give the output 'High'.

DESIGN DATA (Maximum adverse operating conditions assumed)

		Min.	Nom.	Max.	
<b>Temperature</b>					
Operating ambient	FJH101/1A	0	-	70	°C
	FJH106	-40	-	85	°C
<b>Supply</b>					
Supply voltage	FJH101/1A	4.75	-	5.25	V
	FJH106	4.5	-	5.5	V
Supply current (output 'Low') per gate		-	3.0	-	mA
Supply current (output 'High') per gate		-	1.0	-	mA
<b>Inputs</b>					
Voltage for 'High' input state	S.N.I. = 0	2.0	-	-	V
	S.N.I. = 0.4V	2.4	-	-	V
*Current for 'High' input state (each input)		-	-	40	μA
Voltage for 'Low' input state	S.N.I. = 0	-	-	0.8	V
	S.N.I. = 0.4V	-	-	0.4	V
**Current for 'Low' input state		-	-	1.6	mA
<b>Outputs</b>					
Voltage for 'High' output state		2.4	-	-	V
Output resistance in 'High' output state		-	100	-	Ω
Voltage for 'Low' output state		-	-	0.4	V
Output resistance in 'Low' output state		-	12	-	Ω
Current capability at 'Low' output state		-	-	16	mA
Fan-out		-	-	10	

Truth table (for two input terminals)

Input 1	Input 2	Output
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

<b>Performance</b>	Min.	Nom.	Max.	
Signal noise immunity	0.4	1.0	-	V
Average propagation delay time (C <sub>L</sub> = 15pF)	-	13	-	ns

This is equivalent to a propagation delay time to the 'Low' state of 8.0ns and to the 'High' state of 18ns.

\*The 'High' state normally corresponds to a voltage level between 1.4 and 5.25V.  
 \*\*The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.



# T.T.L. SINGLE 8-INPUT NAND GATES

# FJH101 FJH101A FJH106

CHARACTERISTICS (Supply voltage = 5.0V,  $T_{amb} = 25^{\circ}\text{C}$ )

		Min.	Typ.	Max.	
$V_{TH}$	'Low' Input threshold voltage for 'Low' input state ( $V_{out} = 2.4\text{V}$ , $I_{out} = -400\mu\text{A}$ )	0.8*	-	-	V
$V_{TH}$	'High' Input threshold voltage for 'High' input state ( $I_{out} = 16\text{mA}$ , $V_{out} = 0.4\text{V}$ )	-	-	2.0*	V
$V_{out}$	'Low' Output voltage for 'Low' output state ( $V_{in} = 2.0\text{V}$ , $I_{out} = 16\text{mA}$ )	-	0.23	0.4*	V
$V_{out}$	'High' Output voltage for 'High' output state ( $V_{in} = 0.8\text{V}$ , $I_{out} = -400\mu\text{A}$ )	2.4*	3.0	-	V
$I_{in}$	'Low' Input current for 'Low' input state ( $V_{in} = 0.4\text{V}$ , $I_{out} = 0$ )	-	-	1.6*	mA
$I_{in}$	'High' Input current for 'High' input state (each input) ( $V_{in} = 2.4\text{V}$ , $I_{out} = 0$ , other inputs = 0V)	-	-	40*	$\mu\text{A}$
$I_{out}$	'High' Leakage current into the 'High' state output ( $V_{out} = 6.7\text{V}$ ( $V_{in} = 0$ ))	-	-	300	$\mu\text{A}$
$I_{out}$	s/c 'High' Short circuit output current for 'High' output state ( $V_{in} = 0$ , o/p grounded)	18*	-	55*	mA
$t_{pd0}$	Propagation delay time to logical '0' level (Fan-out = 10, $C_L = 15\text{pF}$ )	-	8.0	15	ns
$t_{pd1}$	Propagation delay time to logical '1' level (Fan-out = 10, $C_L = 15\text{pF}$ )	-	18	29	ns

\*These are the characteristics which are recommended for acceptance testing purposes.

## NOTE

$C_L$  = Total capacitance of driven gates including wiring capacitance.



## RATINGS

Limiting values of operation according to the absolute maximum system.

### Electrical (with pin 7 earthed)

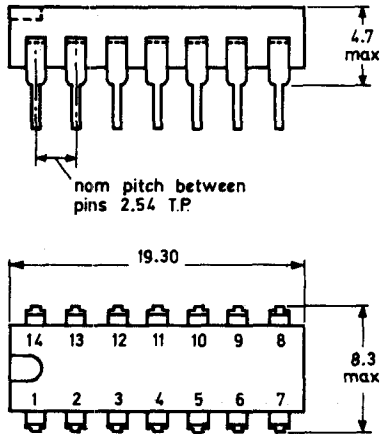
Maximum positive supply voltage (pin 14)	7.0	V
Maximum continuous input voltage (pins 1, 2, 3, 4, 5, 6, 11, 12)	5.5	V
Maximum continuous voltage applied to output (applied through $R_L \geq 270\Omega$ ) (Pin 8)	7.0	V
Maximum negative transient input voltage ( $t_p = 20\text{ns}$ , $f = 5.0\text{MHz}$ , $R_s \geq 75\Omega$ )	-2.0	V

### Temperature

$T_{stg}$ min.	-65	$^{\circ}\text{C}$
$T_{stg}$ max.	150	$^{\circ}\text{C}$
$T_{amb}$ operating range FJH101/1A	0 to +70	$^{\circ}\text{C}$
$T_{amb}$ operating range FJH106	-40 to +85	$^{\circ}\text{C}$

## OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-116



### PINNING

1.	}	Inputs
2.		
3.		
4.		
5.		
6.		
7.	Common	
8.	Output	
9.	N.C.	
10.	N.C.	
11.	}	Inputs
12.		
13.	N.C.	
14.	Supply voltage	

For detailed dimensions see General Explanatory Notes

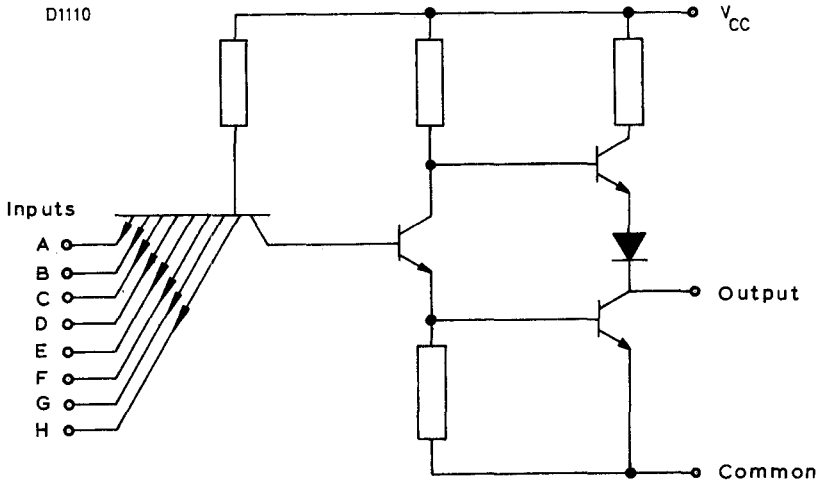
For Handling Notes see General Explanatory Notes



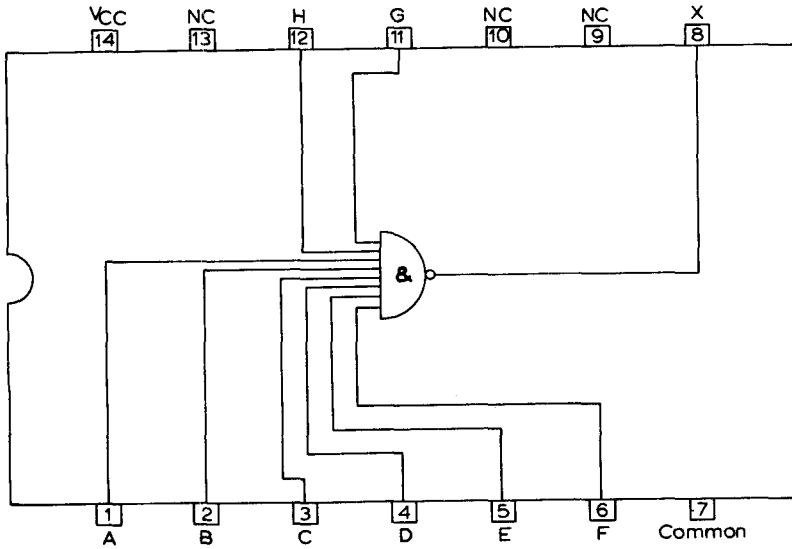
# T.T.L. SINGLE 8-INPUT NAND GATES

**FJH101  
FJH101A  
FJH106**

## EQUIVALENT CIRCUIT



## LOGIC DIAGRAM



Positive logic

$$X = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H.$$

