Pseudo Differential, 1MSPS, 12- & 10-Bit ADCs in 8-lead SOT-23

Preliminary Technical Data — AD7451/AD7441

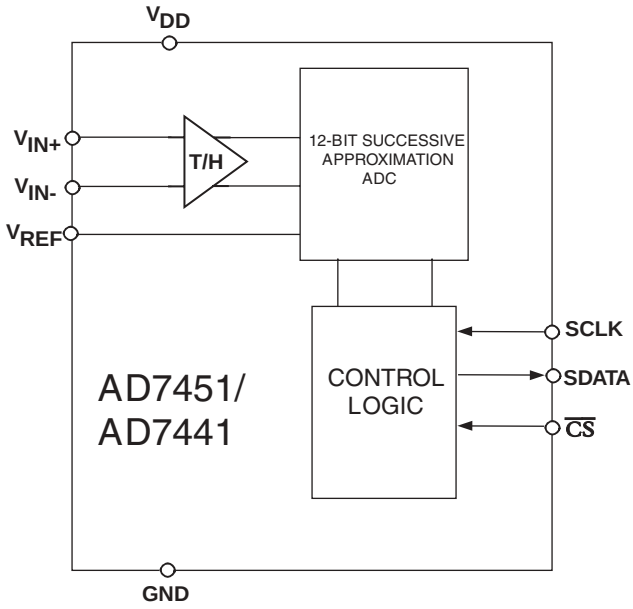
FEATURES

Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power at max Throughput Rate:
3.75 mW typ at 1MSPS with V_{DD} = 3 V
9 mW typ at 1MSPS with V_{DD} = 5 V
Pseudo Differential Analog Input
Wide Input Bandwidth:
70dB SINAD at 300kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface - SPI™/QSPI™/ MICROWIRE™/ DSP Compatible
Power-Down Mode: 1µA max
8 Pin SOT-23 and µSOIC Packages

APPLICATIONS

Transducer Interface
Battery Powered Systems
Data Acquisition Systems
Portable Instrumentation
Motor Control
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7451/AD7441 are respectively 12- and 10-bit, high speed, low power, successive-approximation (SAR) analog-to-digital converters that feature a pseudo differential analog input. These parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1MSPS.

The parts contains a low-noise, wide bandwidth, differential track and hold amplifier (T/H) which can handle input frequencies in excess of 1MHz with the -3dB point being 20MHz typically. The reference voltage is 2.5 V and is applied externally to the V_{REF} pin.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock allowing the device to interface with Microprocessors or DSPs. The input signals are sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point.

The SAR architecture of these parts ensures that there are no pipeline delays.

The AD7451/41 use advanced design techniques to achieve very low power dissipation at high throughput rates.

PRODUCT HIGHLIGHTS

1. Operation with 2.7 V to 5.25 V power supplies.
2. High Throughput with Low Power Consumption. With a 3V supply, the AD7451/41 offer 3.75mW typ power consumption for 1MSPS throughput.
3. Pseudo Differential Analog Input. The V_{IN-} input can be used as an offset from ground
4. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. These parts also feature a shutdown mode to maximize power efficiency at lower throughput rates.
5. No Pipeline Delay.
6. Accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

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AD7451 - SPECIFICATIONS[1]

(V_{DD} = 2.7V to 5.25V, f_{SCLK} = 18MHz, f_S = 1MHz, V_{REF} = 2.5 V; F_{IN} = 300kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Test Conditions/Comments	B Version[1]	Unit	
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) (SINAD)[2]		70	dB min	
Total Harmonic Distortion (THD)[2]	-80dB typ	-75	dB max	
Peak Harmonic or Spurious Noise[2]	-82dB typ	-75	dB max	
Intermodulation Distortion (IMD)[2]				
Second Order Terms		-85	dB typ	
Third Order Terms		-85	dB typ	
Aperture Delay[2]		10	ns typ	
Aperture Jitter[2]		50	ps typ	
Full Power Bandwidth[2]	@ -3 dB	20	MHz typ	
	@ -0.1 dB	2.5	MHz typ	
DC ACCURACY				
Resolution		12	Bits	
Integral Nonlinearity (INL)[2]		±1	LSB max	
Differential Nonlinearity (DNL)[2]	Guaranteed No Missed Codes to 12 Bits.	±1	LSB max	
Offset Error[2]		±3	LSB max	
Gain Error[2]		±3	LSB max	
ANALOG INPUT				
Full Scale Input Span	V_{IN+} - V_{IN-}	V_{REF}	V	
Absolute Input Voltage				
V_{IN+}		V_{REF}	V	
V_{IN-}[3]		0.1 to 1	V	
DC Leakage Current		±1	µA max	
Input Capacitance	When in Track	20	pF typ	
	When in Hold	6	pF typ	
REFERENCE INPUT				
V_{REF} Input Voltage	±1% tolerance for specified performance	2.5	V	
DC Leakage Current		±1	µA max	
V_{REF} Input Capacitance		15	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{IN}	Typically 10nA, V_{IN} = 0VorV_{DD}	±1	µA max	
Input Capacitance, C_{IN}[4]		10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} = 5V; I_{SOURCE} = 200µA	2.8	V min	
	V_{DD} = 3V; I_{SOURCE} = 200µA	2.4	V min	
Output Low Voltage, V_{OL}	I_{SINK} =200µA	0.4	V max	
Floating-State Leakage Current		±1	µA max	
Floating-State Output Capacitance[4]		10	pF max	
Output Coding		Straight (Natural) Binary		

AD7451 - SPECIFICATIONS[1]

Parameter	Test Conditions/Comments	B Version[1]	Units	
CONVERSION RATE				
Conversion Time	888ns with an 18MHz SCLK	16	SCLK cycles	
Track/Hold Acquisition Time[2]	Sine Wave Input	200	ns max	
Step Input	TBD	TBD	ns max	
Throughput Rate[6]		1	MSPS max	
POWER REQUIREMENTS				
V_{DD}		2.7/5.25	Vmin/max	
I_{DD}[5,7]				
Normal Mode(Static)	SCLK On or Off	0.5	mA typ	
Normal Mode (Operational)	V_{DD} = 5 V.	1.8	mA max	
	V_{DD} = 3 V.	1.25	mA max	
Full Power-Down Mode	SCLK On or Off	1	µA max	
Power Dissipation				
Normal Mode (Operational)	V_{DD} =5 V.	9	mW max	
	V_{DD} =3 V.	3.75	mW max	
Full Power-Down	V_{DD} =5 V. SCLK On or Off	5	µW max	
	V_{DD} =3 V. SCLK On or Off	3	µW max	

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See 'Terminology' section.
[3] A small DC input is applied to V_{IN-} to provide a pseudo ground for V_{IN+}
[4]Sample tested @ +25°C to ensure compliance.
[5]See POWER VERSUS THROUGHPUT RATE section.
[6]See 'Serial Interface Section'.
[7]Measured with a midscale DC input.
Specifications subject to change without notice.

AD7441–SPECIFICATIONS[1]

(V_{DD} = 2.7V to 5.25V, f_{SCLK} = 18MHz, f_S = 1MHz, V_{REF} = 2.5 V; F_{IN} = 300kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Test Conditions/Comments	B Version[1]	Unit	
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) (SINAD)[2]		61	dB min	
Total Harmonic Distortion (THD)[2]	-80dB typ	-73	dB max	
Peak Harmonic or Spurious Noise[2]	-82dB typ	-73	dB max	
Intermodulation Distortion (IMD)[2]				
Second Order Terms		-78	dB typ	
Third Order Terms		-78	dB typ	
Aperture Delay[2]		10	ns typ	
Aperture Jitter[2]		50	ps typ	
Full Power Bandwidth[2]	@ -3 dB	20	MHz typ	
	@ -0.1 dB	2.5	MHz typ	
DC ACCURACY				
Resolution		10	Bits	
Integral Nonlinearity (INL)[2]		±0.5	LSB max	
Differential Nonlinearity (DNL)[2]	Guaranteed No Missed Codes to 10 Bits.	±0.5	LSB max	
Offset Error[2]		±3	LSB max	
Gain Error[2]		±3	LSB max	
ANALOG INPUT				
Full Scale Input Span	V_{IN+} - V_{IN-}	V_{REF}	V	
Absolute Input Voltage				
V_{IN+}		V_{REF}	V	
V_{IN-}[3]		0.1 to 1	V	
DC Leakage Current		±1	µA max	
Input Capacitance	When in Track	20	pF typ	
	When in Hold	6	pF typ	
REFERENCE INPUT				
V_{REF} Input Voltage	±1% tolerance for specified performance	2.5	V	
DC Leakage Current		±1	µA max	
V_{REF} Input Capacitance		15	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{IN}	Typically 10nA, V_{IN} = 0VorV$_{DD}$	±1	µA max	
Input Capacitance, C_{IN}[4]		10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} = 5V; I_{SOURCE} = 200µA	2.8	V min	
	V_{DD} = 3V; I_{SOURCE} = 200µA	2.4	V min	
Output Low Voltage, V_{OL}	I_{SINK} =200µA	0.4	V max	
Floating-State Leakage Current		±1	µA max	
Floating-State Output Capacitance[4]		10	pF max	
Output Coding		Straight (Natural) Binary		

AD7441–SPECIFICATIONS[1]

Parameter	Test Conditions/Comments	B Version[1]	Units	
CONVERSION RATE				
Conversion Time	888ns with an 18MHz SCLK	16	SCLK cycles	
Track/Hold Acquisition Time[2]	Sine Wave Input	200	ns max	
	Step Input	TBD	ns max	
Throughput Rate[6]		1	MSPS max	
POWER REQUIREMENTS				
V_{DD}		2.7/5.25	Vmin/max	
I_{DD}[6,7]				
Normal Mode(Static)	SCLK On or Off	0.5	mA typ	
Normal Mode (Operational)	V_{DD} = 5 V.	1.8	mA max	
	V_{DD} = 3 V.	1.25	mA max	
Full Power-Down Mode	SCLK On or Off	1	μA max	
Power Dissipation				
Normal Mode (Operational)	V_{DD} =5 V.	9	mW max	
	V_{DD} =3 V.	3.75	mW max	
Full Power-Down	V_{DD} =5 V. SCLK On or Off	5	μW max	
	V_{DD} =3 V. SCLK On or Off	3	μW max	

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See 'Terminology' section.
[3] A small DC input is applied to V_{IN-} to provide a pseudo ground for V_{IN+}
[4]Sample tested @ +25°C to ensure compliance.
[5]See POWER VERSUS THROUGHPUT RATE section.
[6]See 'Serial Interface Section'.
[7]Measured with a midscale DC input.
Specifications subject to change without notice.

AD7451/AD7441

TIMING SPECIFICATIONS [1,2]

(V_{DD} = 2.7V to 5.25V, f_{SCLK} = 18MHz, f_S = 1MHz, V_{REF} = 2.5 V; F_{IN} = 300kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
f_{SCLK} [4]	10	kHz min	
	18	MHz max	
$t_{CONVERT}$	16 x t_{SCLK}		$t_{SCLK} = 1/f_{SCLK}$
	888	ns max	
t_{QUIET}	25	ns min	Minimum Quiet Time between the End of a Serial Read and the Next Falling Edge of $\overline{CS}$
t_1	10	ns min	Minimum $\overline{CS}$ Pulsewidth
t_2	10	ns min	$\overline{CS}$ falling Edge to SCLK Falling Edge Setup Time
t_3 [5]	20	ns max	Delay from $\overline{CS}$ Falling Edge Until SDATA 3-State Disabled
t_4 [5]	40	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_6	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_7	10	ns min	SCLK Edge to Data Valid Hold Time
t_8 [6]	10	ns min	SCLK Falling Edge to SDATA 3-State Enabled
	35	ns max	SCLK Falling Edge to SDATA 3-State Enabled
$t_{POWER-UP}$ [7]	1	µs max	Power-Up Time from Full Power-Down

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.

[2]See Figure 1, Figure 2 and the 'Serial Interface' section.

[3]Common Mode Voltage.

[4]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[5]Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V and time for an output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.

[6]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[7] See 'Power-up Time' Section.

Specifications subject to change without notice.

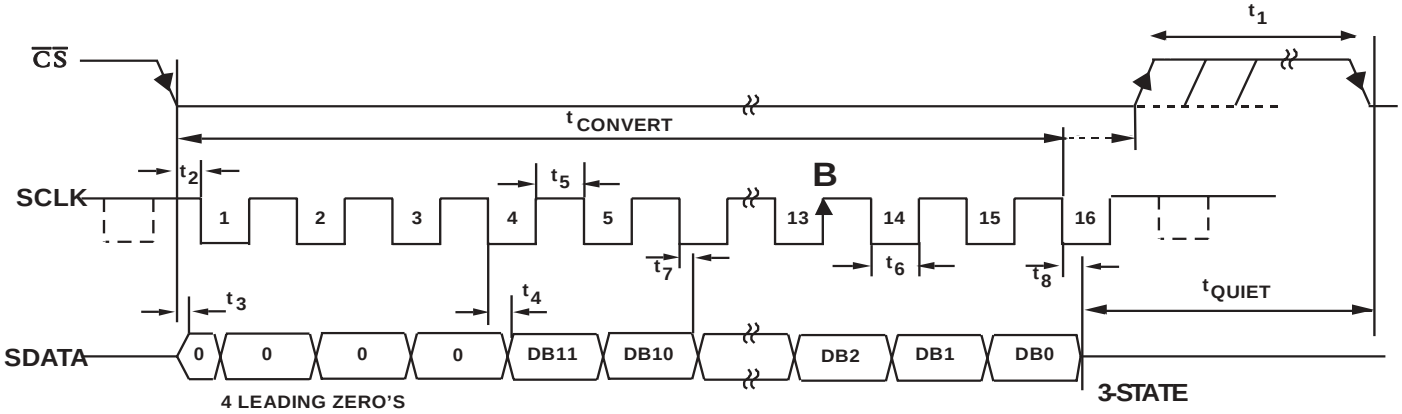


Figure 1. AD7451 Serial Interface Timing Diagram

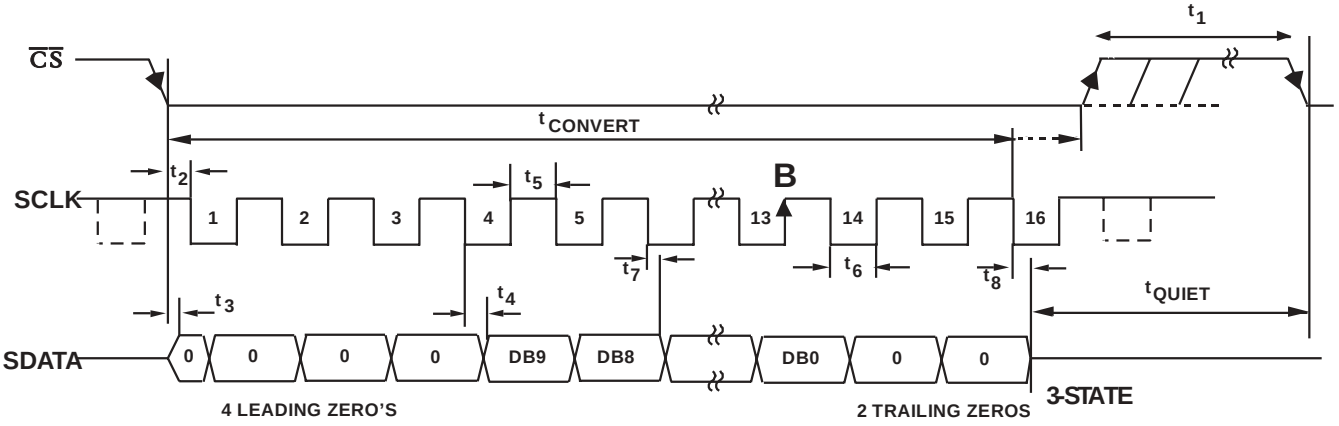


Figure 2. AD7441 Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... -0.3 V to +7 V
V_{IN+} to GND ..... –0.3 V to V_{DD} + 0.3 V
V_{IN-} to GND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND ..... -0.3 V to +7 V
Digital Output Voltage to GND . -0.3 V to V_{DD} + 0.3 V
V_{REF} to GND ..... -0.3 V to V_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2] .... ±10mA
Operating Temperature Range
Commercial (A, B Version) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
θ_{JA} Thermal Impedance .....205.9°C/W (µSOIC)
211.5°C/W (SOT-23)
θ_{JC} Thermal Impedance ..... 43.74°C/W (µSOIC)
91.99°C/W (SOT-23)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C
ESD 3.5kV

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

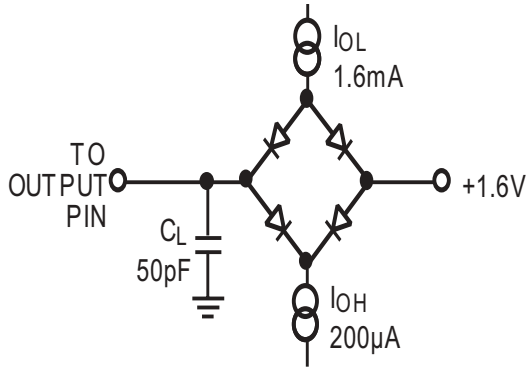


Figure 3. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[4]	Branding Information
AD7451BRT	-40°C to +85°C	±1 LSB	RT-8	TBD
AD7451BRM	-40°C to +85°C	±1 LSB	RM-8	TBD
AD7441BRT	-40°C to +85°C	±0.5 LSB	RT-8	TBD
AD7441BRM	-40°C to +85°C	±0.5 LSB	RM-8	TBD
TBD	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

NOTES
[1]Linearity error here refers to Integral Non-linearity Error.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVALUATION BOARD CONTROLLER for evaluation/demonstration purposes.
[3]EVALUATION BOARD CONTROLLER. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete Evaluation Kit, you will need to order the ADC evaluation board i.e. TBD, the EVAL-CONTROL BRD2 and a 12V AC transformer. See the TBD technote for more information.
[4]RT = SOT-23; RM = µSOIC

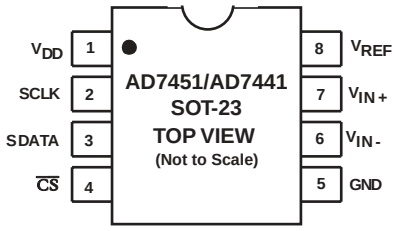
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7451/AD7441 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

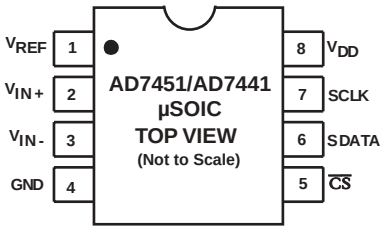
PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
V_{REF}	Reference Input for the AD7451/41. An external 2.5 V reference must be applied to this input.This pin should be decoupled to GND with a capacitor of at least 0.1µF.
V_{IN+}	Non-Inverting Input.
V_{IN-}	Inverting Input. This pin sets the ground reference point for the V_{IN+} input. Connect to Ground or to a small DC offset to provide a pseudo ground.
GND	Analog Ground. Ground reference point for all circuitry on the AD7451/41. All analog input signals and any external reference signal should be referred to this GND voltage.
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating a conversion on the AD7451/41 and framing the serial data transfer.
SDATA	Serial Data. Logic Output. The conversion result from the AD7451/41 is provided on this out put as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7451 consists of four leading zeros followed by the 12 bits of conversion data which are provided MSB first; the data stream of the AD7441 consists of four leading zeros, followed by the 10-bits of conversion data, followed by two trailing zeros. In both cases, the output coding is Straight (Natural) Binary.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process.
V_{DD}	Power Supply Input. V_{DD} is 2.7 V to 5.25 V. This supply should be decoupled to GND with a 0.1µF Capacitor and a 10µF Tantalum Capacitor.

PIN CONFIGURATION 8-LEAD SOT-23



PIN CONFIGURATION µSOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter this is 62dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7450, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7451/41 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter
This is the sample to sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth
The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1dB or 3dB for a full scale input.

Integral Nonlinearity (INL)
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (000...000 to 000...001) from the ideal (i.e. AGND + 1LSB)

Gain Error
This is the deviation of the last code transition (111...110 to 111...111) from the ideal (i.e., V_{REF} - 1LSB), after the Offset Error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode on the 13th SCLK rising edge (see the "Serial Interface Section"). The track/hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

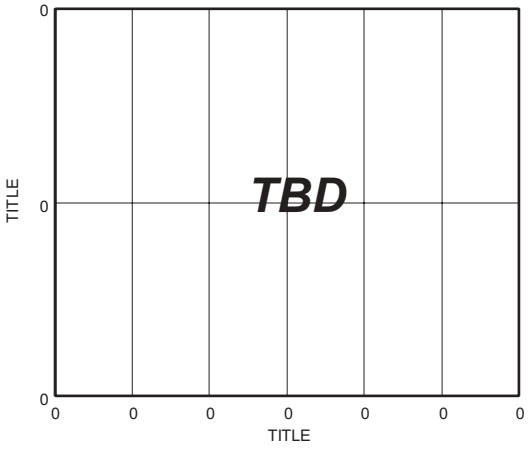
Power Supply Rejection Ratio (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of this input varies from 1kHz to 1MHz.

PSRR (dB) = 10 log (Pf/Pfs)

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

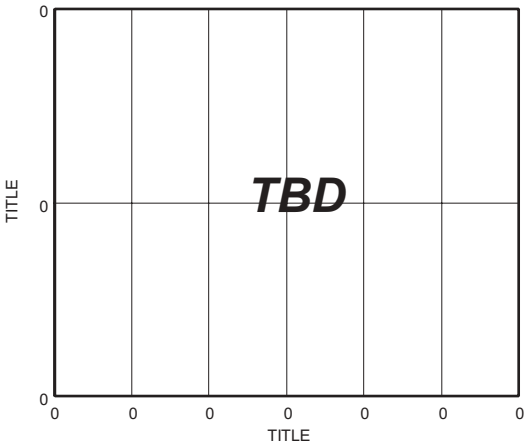
PERFORMANCE CURVES

(Default Conditions: TA = 25°C, Fs = 1MSPS, FSCLK = 18MHz, V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V)

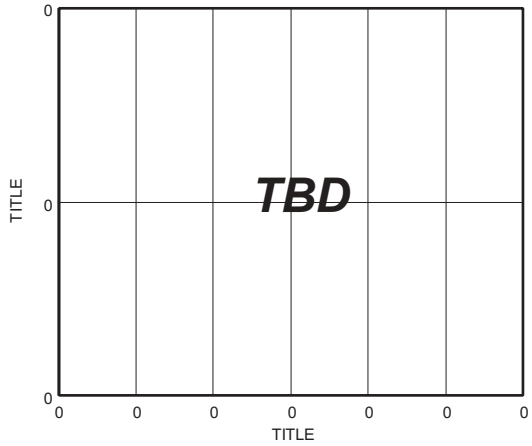


TPC 1. SINAD vs Analog Input Frequency for Various Supply Voltages

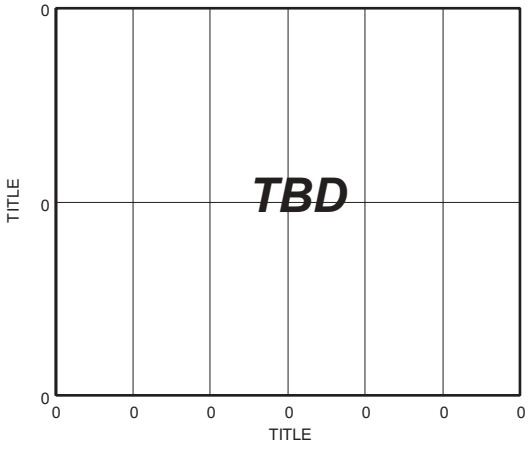
TPC 2 and TPC 3 shows the Power Supply Rejection Ratio (see Terminology) versus V_{DD} supply ripple frequency for the AD7451/41 with and without power supply decoupling respectively.



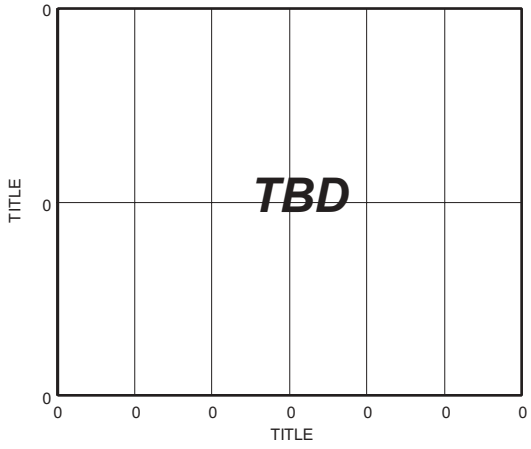
TPC 2. PSRR vs. Supply Ripple Frequency without Supply Decoupling



TPC 3. PSRR vs. Supply Ripple Frequency with Supply Decoupling of TBD

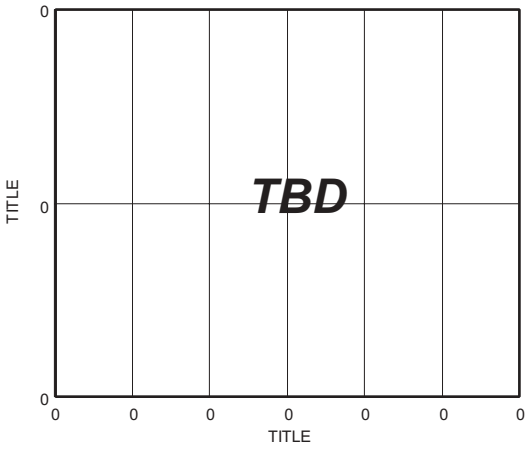


TPC 4. THD vs. Analog Input Frequency for Various Source Impedances

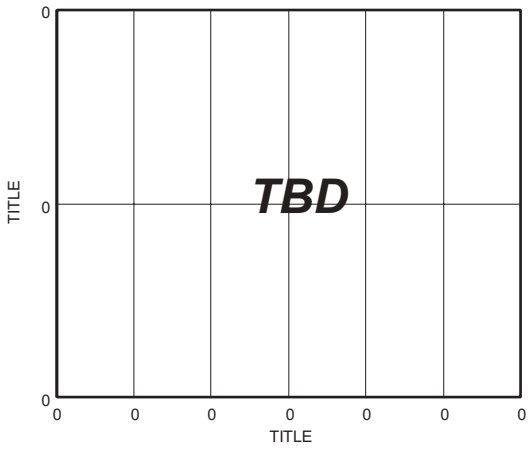


TPC 5. THD vs. Analog Input Frequency for Various Supply Voltages

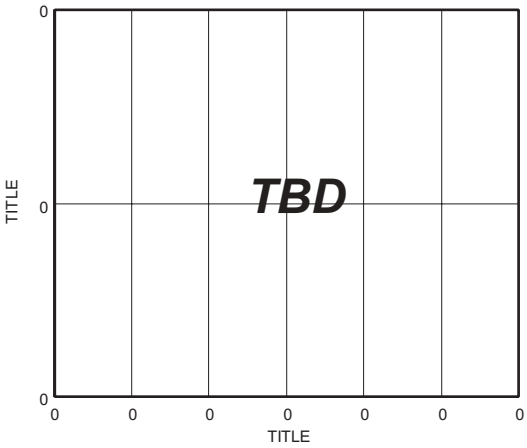
AD7451 PERFORMANCE CURVES
(Default Conditions: TA = 25°C, Fs = 1MSPS, FSCLK = 18MHz, V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V)



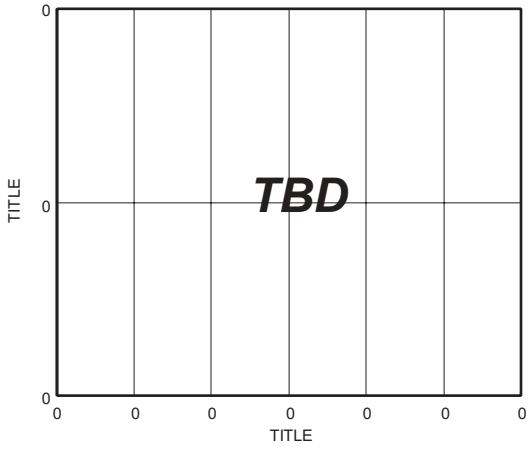
TPC 6. AD7451 Dynamic Performance



TPC 9. Histogram of 10000 conversions of a DC Input for the AD7451

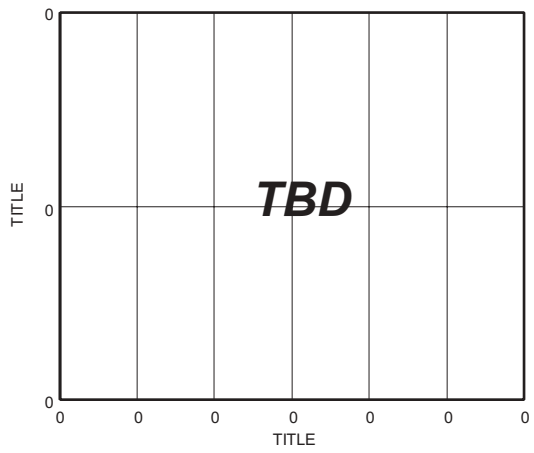


TPC 7. Typical DNL For the AD7451

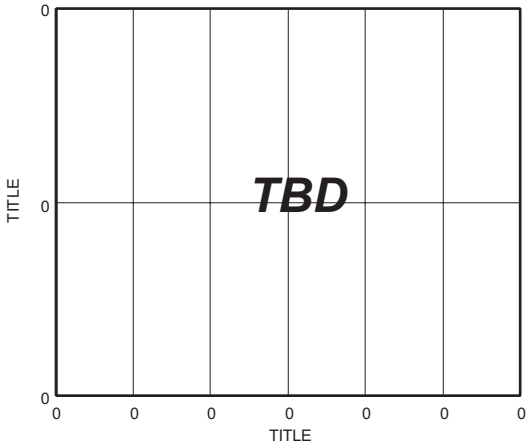


TPC 8. Typical INL For the AD7451

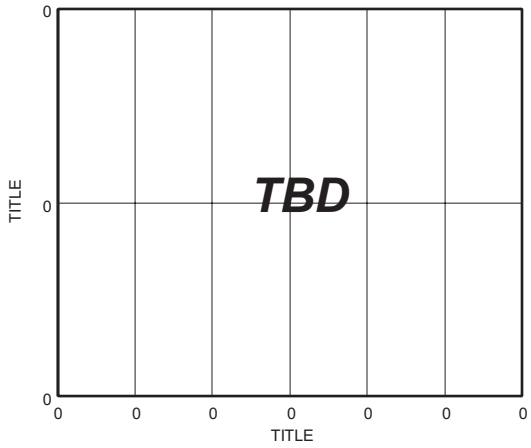
AD7441 PERFORMANCE CURVES
(Default Conditions: TA = 25°C, Fs = 1MSPS, FSCLK = 18MHz, V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V)



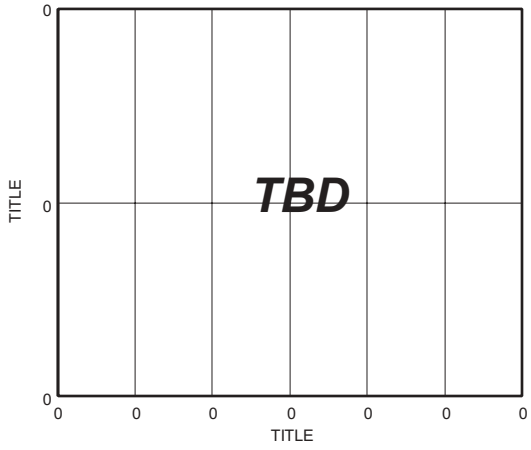
TPC 10. AD7441 Dynamic Performance



TPC 13. Histogram of 10000 conversions of a DC Input for the AD7441



TPC 11. Typical DNL For the AD7441



TPC 12. Typical INL For the AD7441

SERIAL INTERFACE

Figures 1 and 2 show detailed timing diagrams for the serial interface of the AD7451 and the AD7441 respectively. The serial clock provides the conversion clock and also controls the transfer of data from the device during conversion. $\overline{CS}$ initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$ puts the track and hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion initiated at this point. The conversion will require 16 SCLK cycles to complete.

Once 13 SCLK falling edges have occurred, the track and hold will go back into track on the next SCLK rising edge as shown at point B in Figures 1 and 2. On the 16th SCLK falling edge the SDATA line will go back into three-state.

If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state on the 16th SCLK falling edge.

The conversion result from the AD7451/41 is provided on the SDATA output as a serial data streatm. The bits are clocked out on the falling edge of the SCLK input. The data streatm of the AD7451 consists of four leading zeros, followed by 12 bits of conversion data which is provided MSB first; the data stream of the AD7441 consists of four leading zeros, followed by the 10 bits of conversion data, followed by two trailing zeros, which is also provided MSB first. In both cases, the output coding is straight (natural) binary.

16 serial clock cycles are required to perform a conversion and to access data from the AD7451/41. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges beginning with the second leading zero. Thus the first falling clock edge on the serial clock provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge. Once the conversion is complete and the data has been accessed after the 16 clock cycles, it is important to ensure that, before the next conversion is initiated, enough time is left to meet the acquisition and quiet time specifications - see the Timing Examples. To achieve 1MSPS with an 18MHz clock for V_{DD} = 3 V and 5 V, an 18 clock burst will perform the conversion and leave enough time before the next conversion for the acquisition and quiet time.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge i.e. the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the 15th SCLK edge would have DB0 provided.

Timing Example 1

Having F_{SCLK} = 18MHz and a throughput rate of 1MSPS gives a cycle time of:

1/Throughput = 1/1000000 = 1µs

A cycle consists of:

t_2 + 12.5 $(1/F_{SCLK})$ + t_{ACQ} = 1µs.

Therefore if t_2 = 10ns then:

10ns + 12.5(1/18MHz) + t_{ACQ} = 1µs

t_{ACQ} = 296ns

This 296ns satisfies the requirement of 200ns for t_{ACQ}.

From Figure 4, t_{ACQ} comprises of:

$2.5(1/F_{SCLK})$ + t_8 + t_{QUIET}

where t_8 = 35ns. This allows a value of 122ns for t_{QUIET} satisfying the minimum requirement of 25ns.

Timing Example 2

Having F_{SCLK} = 5MHz and a throughput rate of 315kSPS gives a cycle time of :

1/Throughput = 1/315000 = 3.174µs

A cycle consists of:

t_2 + 12.5 $(1/F_{SCLK})$ + t_{ACQ} = 3.174µs.

Therefore if t_2 is 10ns then:

10ns + 12.5(1/5MHz) + t_{ACQ} = 3.174µs

t_{ACQ} = 664ns

This 664ns satisfies the requirement of 200ns for t_{ACQ}.

From Figure 4, t_{ACQ} comprises of:

$2.5(1/F_{SCLK})$ + t_8 + t_{QUIET}

where t_8 = 35ns. This allows a value of 129ns for t_{QUIET} satisfying the minimum requirement of 25ns.

As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete but it is still necessary to leave 25ns minimum t_{QUIET} between conversions. In example 2 the signal should be fully acquired at approximately point C in Figure 4.

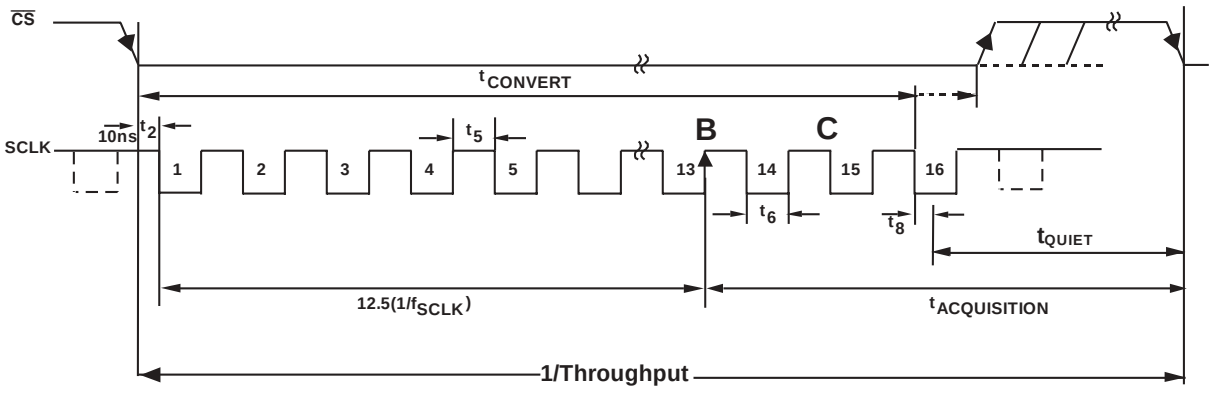


Figure 4. Serial Interface Timing Example

MODES OF OPERATION

The mode of operation of the AD7451 and the AD7441 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether or not the AD7451/41 will enter the power-down mode. Similarly, if already in power-down, $\overline{CS}$ controls whether the devices will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance. The user does not have to worry about any power-up times with the AD7451/41 remaining fully powered up all the time. Figure 5 shows the general diagram of the operation of the AD7451/41 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$ as described in the 'Serial Interface Section'. To ensure the part remains fully powered up, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$.

If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion. Once a data transfer is complete, i.e. when SDATA has returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET} has elapsed by again bringing $\overline{CS}$ low.

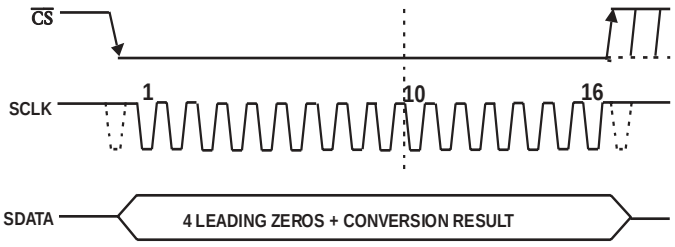


Figure 5. Normal Mode Operation

Power Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7451/AD7441 is in the power down mode, all analog circuitry is powered down. To enter power down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 6.

Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power down and the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into three-state. The time from the rising edge of $\overline{CS}$ to SDATA three-state enabled will never be greater than t_8 (see the 'Timing Specifications'). If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power-down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7451/41 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up after 1µsec has elapsed and, as shown in Figure 7, valid data will result from the next conversion.

If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7451/41 will again go back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will again power-down on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

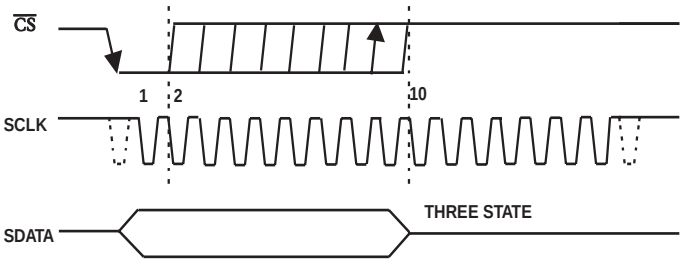


Figure 6. Entering Power Down Mode

Power up Time

The power up time of the AD7451/41 is typically 1µsec, which means that with any frequency of SCLK up to 18MHz, one dummy cycle will always be sufficient to allow the device to power-up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quiet time t_{QUIET} must still be allowed from the point at which the bus goes back into three-state after the dummy conversion, to the next falling edge of $\overline{CS}$.

When running at the maximum throughput rate of 1MSPS, the AD7451/41 will power up and acquire a signal within ±0.5LSB in one dummy cycle, i.e. 1µs. When powering up from the power-down mode with a dummy cycle, as in Figure 7, the track and hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 7.

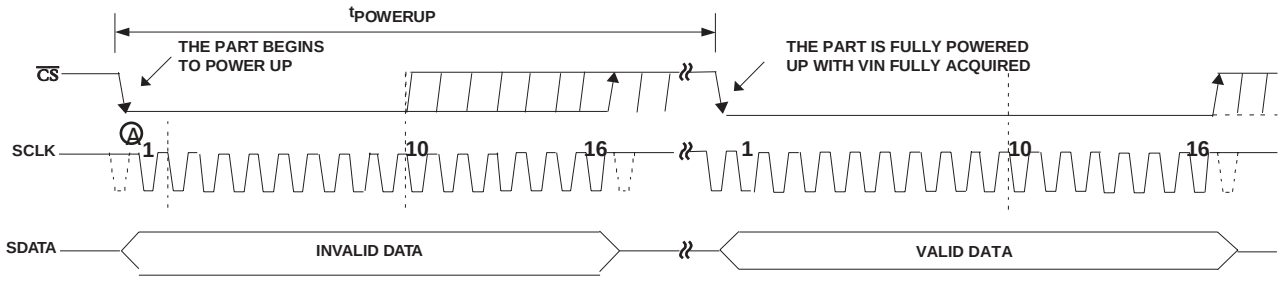


Figure 7. Exiting Power Down Mode

Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1µs will be sufficient to power the device up and acquire the input signal.

For example, if a 5MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2µs (i.e. 1/(5MHz) x 16). In one dummy cycle, 3.2µs, the part would be powered up and V_{IN} acquired fully. However after 1µs with a 5MHz SCLK only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7451/41, the ADC may either power up in the power-down mode or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if the user wishes the part to power up in power-down mode, then the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 6.

Once supplies are applied to the AD7451/41, the power up time is the same as that when powering up from the power-down mode. It takes approximately 1µs to power up fully if the part powers up in normal mode. It is not necessary to wait 1µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed.

As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track and hold will already be in track. This means if (assuming one has the facility to monitor the ADC supply current) the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track and hold into track.

POWER VERSUS THROUGHPUT RATE

By using the power-down mode on the AD7451/41 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 8 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption reduces accordingly. It shows this for both 5V and 3V power supplies.

For example, if the AD7451/41 is operated in continous sampling mode with a throughput rate of 100kSPS and an SCLK of 18MHz and the device is placed in the power down mode between conversions, then the power consumption is calculated as follows:

Power dissipation during normal operation = 9mW max (for V_{DD} = 5V).

If the power up time is 1 dummy cycle i.e. 1µsec, and the remaining conversion time is another cycle i.e. 1µsec, then the AD7451/41 can be said to dissipate 9mW for 2µsec during each conversion cycle.

If the throughput rate = 100kSPS then the cycle time = 10µsec and the average power dissipated during each cycle is:

(2/10) x 9mW = 1.8mW

For the same scenario, if V_{DD} = 3V, the power dissipation during normal operation is 3.75mW max.

The AD7450 can now be said to dissipate 3.75mW for 2µsec* during each conversion cycle.

The average power dissipated during each cycle with a throughput rate of 100kSPS is therefore:

(2/10) x 3.75mW = 0.75mW

This is how the power numbers in Figure 8 are calculated.

TBD

Figure 8. Power vs. Throughput rate for the Power Down Mode

For throughput rates above 320kSPS, it is recommended that for optimum power performance, the serial clock frequency is reduced.