



# 2.5 V/3.3 V, 10-Bit, 2-Port Level Translating, Bus Switch

## Preliminary Technical Data

## ADG3246

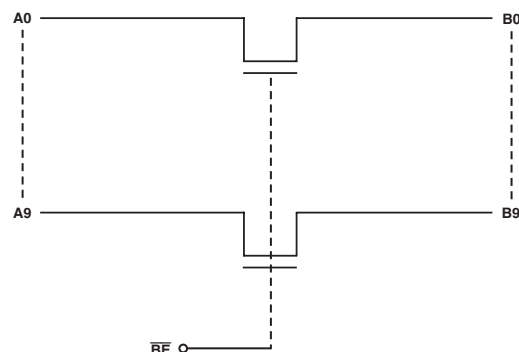
### FEATURES

225 ps Propagation Delay through the Switch  
 4.5  $\Omega$  Switch Connection between Ports  
 Data Rate 1.244 Gbps  
 2.5 V/3.3 V Supply Operation  
 Selectable Level Shifting/Translation  
 Small Signal Bandwidth 610 MHz  
 Level Translation  
   3.3 V to 2.5 V  
   3.3 V to 1.8 V  
   2.5 V to 1.8 V  
 24-Lead TSSOP and LFCSP Packages

### APPLICATIONS

3.3 V to 1.8 V Voltage Translation  
 3.3 V to 2.5 V Voltage Translation  
 2.5 V to 1.8 V Voltage Translation  
 Bus Switching  
 Bus Isolation  
 Hot Swap  
 Hot Plug  
 Analog Signal Switching

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The ADG3246 is a 2.5 V or 3.3 V, 10-bit, 2-port digital switch. It is designed on Analog Devices' low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance, allowing inputs to be connected to outputs without additional propagation delay or generating additional ground bounce noise.

The switches are enabled by means of the Bus Enable ( $\overline{BE}$ ) input signal. These digital switches allow bidirectional signals to be switched when ON. In the OFF condition, signal levels up to the supplies are blocked.

This device is ideal for applications requiring level translation. When operated from a 3.3 V supply, level translation from 3.3 V inputs to 2.5 V outputs occurs. Similarly, if the device is operated from a 2.5 V supply and 2.5 V inputs are applied, the device will translate the outputs to 1.8 V. In addition to this, the ADG3246 has a level translating select pin ( $\overline{SEL}$ ). When  $\overline{SEL}$  is low,  $V_{CC}$  is reduced internally, allowing for level translation between 3.3 V inputs and 1.8 V outputs. This makes the device suited to applications requiring level translation between different supplies, such as converter to DSP/microcontroller interfacing.

### PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation
2. Extremely low propagation delay through switch
3. 4.5  $\Omega$  switches connect inputs to outputs
4. Level/voltage translation
5. 24-lead 4 mm  $\times$  4 mm LFCSP and 24-lead TSSOP packages

REV. PrC

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# ADG3246—SPECIFICATIONS<sup>1</sup> ( $V_{CC} = 2.3 \text{ V}$ to $3.6 \text{ V}$ , $GND = 0 \text{ V}$ , all specifications $T_{MIN}$ to $T_{MAX}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	B Version			Unit
			Min	Typ <sup>2</sup>	Max	
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V <sub>INH</sub>	V <sub>CC</sub> = 2.7 V to 3.6 V	2.0			V
	V <sub>INH</sub>	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V <sub>INL</sub>	V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	V
	V <sub>INL</sub>	V <sub>CC</sub> = 2.3 V to 2.7 V			0.7	V
Input Leakage Current	I <sub>I</sub>			±0.01	±1	μA
OFF State Leakage Current	I <sub>OZ</sub>	0 ≤ A, B ≤ V <sub>CC</sub>		±0.01	±1	μA
ON State Leakage Current		0 ≤ A, B ≤ V <sub>CC</sub>		±0.01	±1	μA
Max Pass Voltage	V <sub>P</sub>	V <sub>A</sub> /V <sub>B</sub> = V <sub>CC</sub> = $\overline{\text{SEL}}$ = 3.3 V, I <sub>O</sub> = −5 μA	2.0	2.5	2.9	V
		V <sub>A</sub> /V <sub>B</sub> = V <sub>CC</sub> = $\overline{\text{SEL}}$ = 2.5 V, I <sub>O</sub> = −5 μA	1.5	1.8	2.1	V
		V <sub>A</sub> /V <sub>B</sub> = V <sub>CC</sub> = 3.3 V, $\overline{\text{SEL}}$ = 0 V, I <sub>O</sub> = −5 μA	1.5	1.8	2.1	V
CAPACITANCE <sup>3</sup>						
A Port Off Capacitance	C <sub>A</sub> OFF	f = 1 MHz		5		pF
B Port Off Capacitance	C <sub>B</sub> OFF	f = 1 MHz		5		pF
A, B Port On Capacitance	C <sub>A</sub> , C <sub>B</sub> ON	f = 1 MHz		10		pF
Control Input Capacitance	C <sub>IN</sub>	f = 1 MHz		6		pF
SWITCHING CHARACTERISTICS <sup>3</sup>						
Propagation Delay A to B or B to A, t <sub>PD</sub> <sup>4</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50 pF, V <sub>CC</sub> = $\overline{\text{SEL}}$ = 3 V			0.225	ns
Propagation Delay Matching <sup>5</sup>					22.5	ps
Bus Enable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PZH</sub> , t <sub>PZL</sub>	V <sub>CC</sub> = 3.0 V to 3.6 V; $\overline{\text{SEL}}$ = V <sub>CC</sub>	1	3.2	4.8	ns
Bus Disable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	V <sub>CC</sub> = 3.0 V to 3.6 V; $\overline{\text{SEL}}$ = V <sub>CC</sub>	1	3.2	4.8	ns
Bus Enable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PZH</sub> , t <sub>PZL</sub>	V <sub>CC</sub> = 3.0 V to 3.6 V; $\overline{\text{SEL}}$ = 0 V	0.5	2.2	3.3	ns
Bus Disable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	V <sub>CC</sub> = 3.0 V tp 3.6 V; $\overline{\text{SEL}}$ = 0 V	0.5	1.7	2.9	ns
Bus Enable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PZH</sub> , t <sub>PZL</sub>	V <sub>CC</sub> = 2.3 V to 2.7 V; $\overline{\text{SEL}}$ = V <sub>CC</sub>	0.5	2.2	3	ns
Bus Disable Time $\overline{\text{BE}}$ to A or B <sup>6</sup>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	V <sub>CC</sub> = 2.3 V to 2.7 V; $\overline{\text{SEL}}$ = V <sub>CC</sub>	0.5	1.75	2.6	ns
Max Data Rate		V <sub>CC</sub> = $\overline{\text{SEL}}$ = 3.3 V; V <sub>A</sub> /V <sub>B</sub> = 2 V		1.244		Gbps
Channel Jitter		V <sub>CC</sub> = $\overline{\text{SEL}}$ = 3.3 V; V <sub>A</sub> /V <sub>B</sub> = 2 V		50		ps p-p
Operating Frequency—Bus Enable	f <sub><math>\overline{\text{BE}}</math></sub>				10	MHz
DIGITAL SWITCH						
On Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA		4.5	8	Ω
		V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 1.7 V, I <sub>BA</sub> = 8 mA		15	28	Ω
		V <sub>CC</sub> = 2.3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA		5	9	Ω
		V <sub>CC</sub> = 2.3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 1 V, I <sub>BA</sub> = 8 mA		11	18	Ω
		V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = 0 V, V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA		5	8	Ω
		V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = 0 V, V <sub>A</sub> = 1 V, I <sub>BA</sub> = 8 mA		14		Ω
On Resistance Matching	ΔR <sub>ON</sub>	V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 0 V, I <sub>BA</sub> = 8 mA		0.45		Ω
		V <sub>CC</sub> = 3 V, $\overline{\text{SEL}}$ = V <sub>CC</sub> , V <sub>A</sub> = 1 V, I <sub>BA</sub> = 8 mA		0.65		Ω
POWER REQUIREMENTS						
V <sub>CC</sub>			2.3		3.6	V
Quiescent Power Supply Current	I <sub>CC</sub>	Digital Inputs = 0 V or V <sub>CC</sub> ; $\overline{\text{SEL}}$ = V <sub>CC</sub>		0.001	1	μA
	I <sub>CC</sub>	Digital Inputs = 0 V or V <sub>CC</sub> ; $\overline{\text{SEL}}$ = 0 V		0.65	1.2	mA
Increase in I <sub>CC</sub> per Input <sup>7</sup>	ΔI <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, $\overline{\text{BE}}$ = 3.0 V; $\overline{\text{SEL}}$ = V <sub>CC</sub>			130	μA

**NOTES**<sup>1</sup>Temperature range is as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .<sup>2</sup>Typical values are at  $25^\circ\text{C}$  unless otherwise stated.<sup>3</sup>Guaranteed by design, not subject to production test.<sup>4</sup>The digital switch contributes no propagation delay other than the RC delay of the typical  $R_{ON}$  of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.<sup>5</sup>Propagation delay matching between channels is calculated from the on resistance matching and load capacitance of  $50 \text{ pF}$ .<sup>6</sup>See Timing Measurement Information.<sup>7</sup>This current applies to the control pin ( $\overline{BE}$ ) only. The A and B ports contribute no significant ac or dc currents as they transition.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>CC</sub> to GND	−0.5 V to +4.6 V
Digital Inputs to GND	−0.5 V to +4.6 V
DC Input Voltage	−0.5 V to +4.6 V
DC Output Current	120 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

**LFCSP Package** $\theta_{JA}$  Thermal Impedance ..... 35°C/W**TSSOP Package** $\theta_{JA}$  Thermal Impedance ..... 128°C/W

Lead Temperature, Soldering (10 seconds) ..... 300°C

IR Reflow, Peak Temperature (&lt;20 seconds) ..... 235°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

**ORDERING GUIDE**

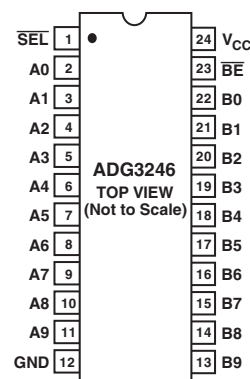
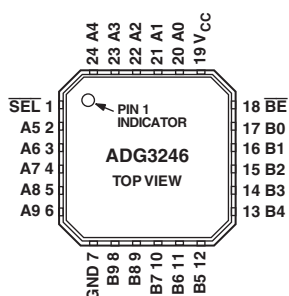
Model	Temperature Range	Package Description	Package Option
ADG3246BCP	−40°C to +85°C	Chip Scale Package (LFCSP)	CP-24
ADG3246BRU	−40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-24

**Table I. Pin Description**

Pin Mnemonic	Description
$\overline{BE}$	Bus Enable (Active Low)
$\overline{SEL}$	Level Translation Select
Ax	Port A, Inputs or Outputs
Bx	Port B, Inputs or Outputs

**Table II. Truth Table**

$\overline{BE}$	$\overline{SEL}^*$	Function
L	L	A = B, 3.3 V to 1.8 V Level Shifting
L	H	A = B, 3.3 V to 2.5 V/2.5 V to 1.8 V Level Shifting
H	X	Disconnect

\* $\overline{SEL}$  = 0 only when V<sub>DD</sub> = 3.3 V ± 10%**PIN CONFIGURATION**  
**24-Lead LFCSP and 24-Lead TSSOP****CAUTION**

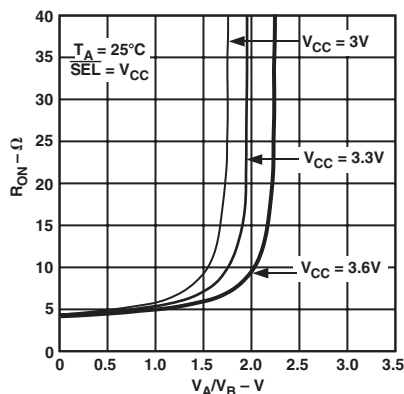
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3246 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



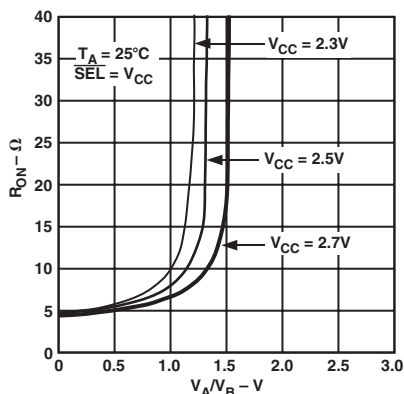
## TERMINOLOGY

$V_{CC}$	Positive Power Supply Voltage
GND	Ground (0 V) Reference
$V_{INH}$	Minimum Input Voltage for Logic 1
$V_{INL}$	Maximum Input Voltage for Logic 0
$I_I$	Input Leakage Current at the Control Inputs
$I_{OZ}$	OFF State Leakage Current. It is the maximum leakage current at the switch pin in the OFF state.
$I_{OL}$	ON State Leakage Current. It is the maximum leakage current at the switch pin in the ON state.
$V_P$	Max Pass Voltage. The max pass voltage relates to the clipped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.
$R_{ON}$	Ohmic Resistance Offered by a Switch in the ON State. It is measured at a given voltage by forcing a specified amount of current through the switch.
$\Delta R_{ON}$	On Resistance Match between Any Two Channels, i.e., $R_{ON} \text{ Max} - R_{ON} \text{ Min}$
$C_X \text{ OFF}$	OFF Switch Capacitance
$C_X \text{ ON}$	ON Switch Capacitance
$C_{IN}$	Control Input Capacitance. This consists of $\overline{BE}$ and $\overline{SEL}$ .
$I_{CC}$	Quiescent Power Supply Current. It is measured when all control inputs are at a logic HIGH or LOW level and the switches are OFF.
$\Delta I_{CC}$	Extra Power Supply Current Component for the $\overline{BE}$ Control Input when the Input is not Driven at the Supplies
$t_{PLH}, t_{PHL}$	Data Propagation Delay through the Switch in the ON State. Propagation delay is related to the RC time constant $R_{ON} \times C_L$ , where $C_L$ is the load capacitance.
$t_{PZH}, t_{PZL}$	Bus Enable Times. These are times taken to cross the $V_T$ voltage at the switch output when the switch turns on in response to the control signal, $\overline{BE}$ .
$t_{PHZ}, t_{PLZ}$	Bus Disable Times. This is the time taken to place the switch in the high impedance OFF state in response to the control signal. It is measured as the time taken for the output voltage to change by $V_{\Delta}$ from the original quiescent level, with reference to the logic level transition at the control input. (Refer to Figure 3 for enable and disable times.)
Max Data Rate	Maximum Rate at which Data Can Be Passed through the Switch
Channel Jitter	Peak-to-Peak Value of the Sum of the Deterministic and Random Jitter of the Switch Channel
$f_{\overline{BE}x}$	Operating Frequency of Bus Enable. This is the maximum frequency at which Bus Enable ( $\overline{BE}$ ) can be toggled.

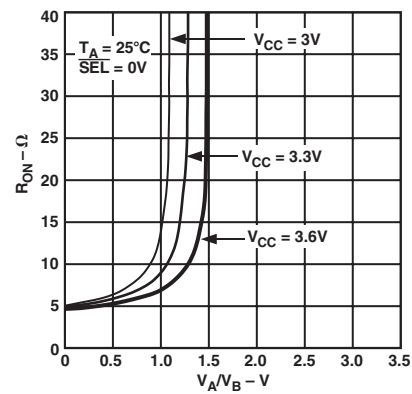
## Typical Performance Characteristics—ADG3246



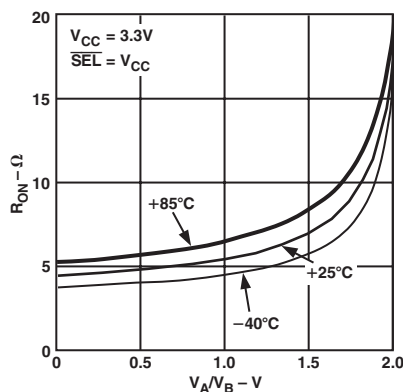
TPC 1. On Resistance vs. Input Voltage



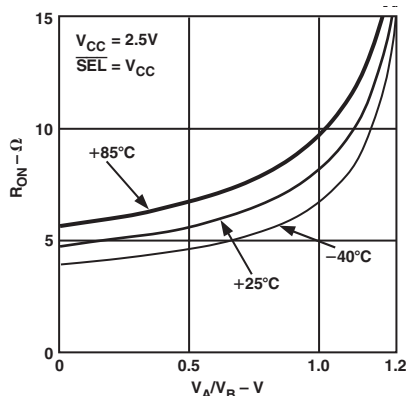
TPC 2. On Resistance vs. Input Voltage



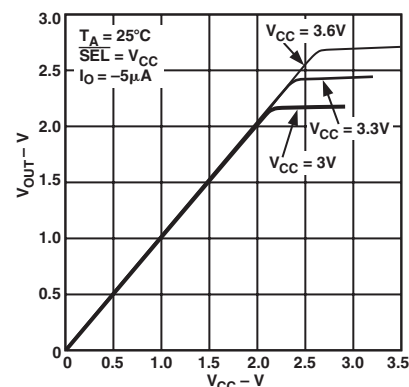
TPC 3. On Resistance vs. Input Voltage



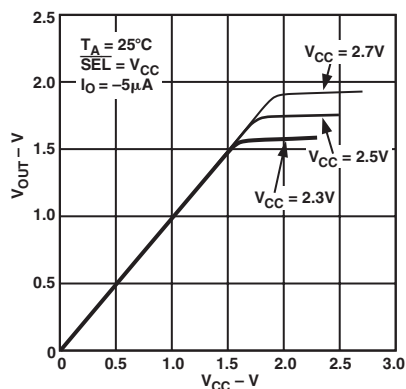
TPC 4. On Resistance vs. Input Voltage for Different Temperatures



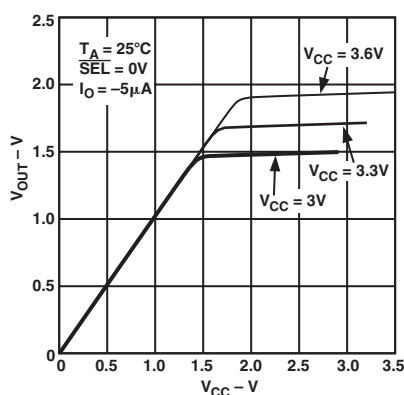
TPC 5. On Resistance vs. Input Voltage for Different Temperatures



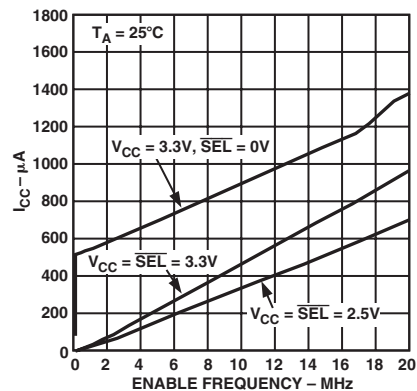
TPC 6. Pass Voltage vs.  $V_{CC}$



TPC 7. Pass Voltage vs.  $V_{CC}$

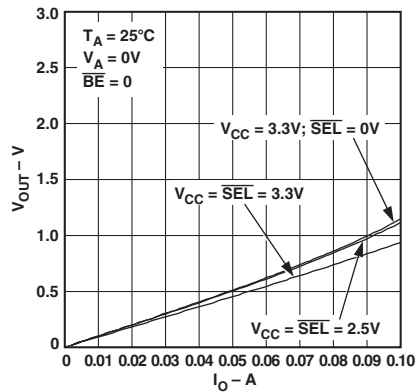


TPC 8. Pass Voltage vs.  $V_{CC}$

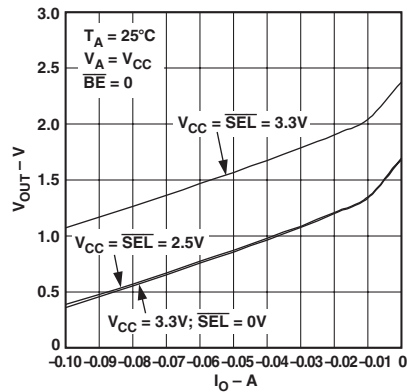


TPC 9.  $I_{CC}$  vs. Enable Frequency

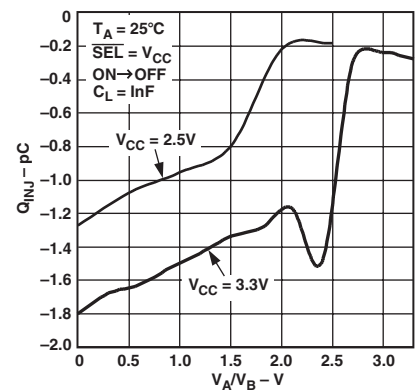
## ADG3246



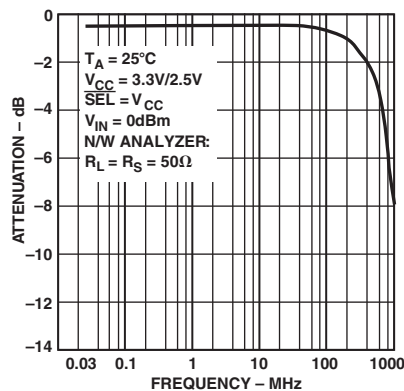
TPC 10. Output Low Characteristic



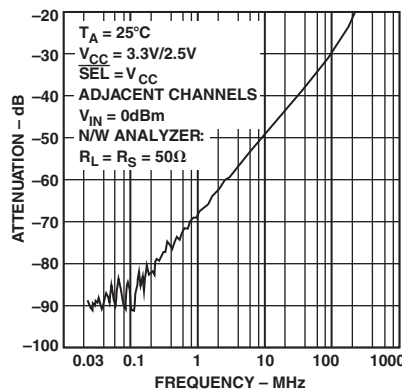
TPC 11. Output High Characteristic



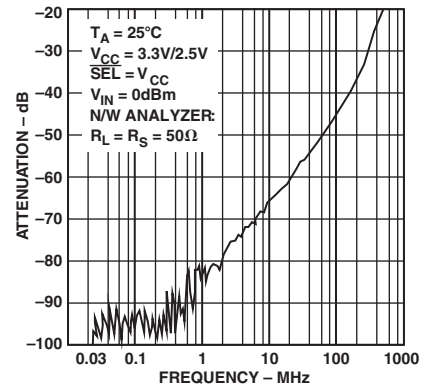
TPC 12. Charge Injection vs. Source Voltage



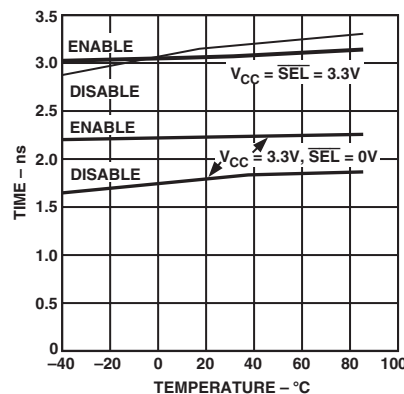
TPC 13. Bandwidth vs. Frequency



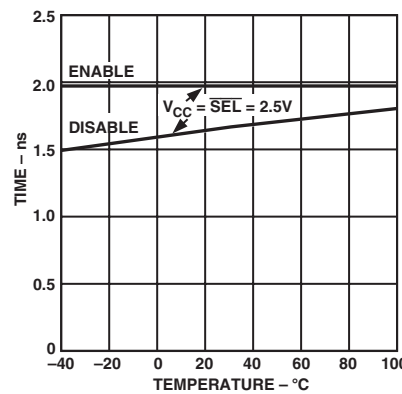
TPC 14. Crosstalk vs. Frequency



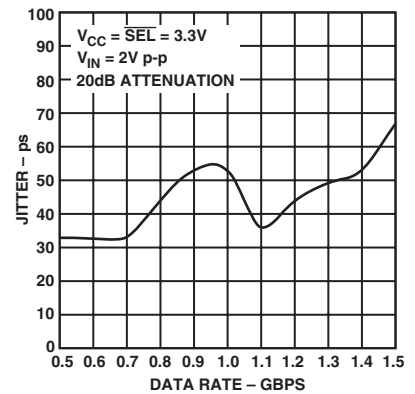
TPC 15. Off Isolation vs. Frequency



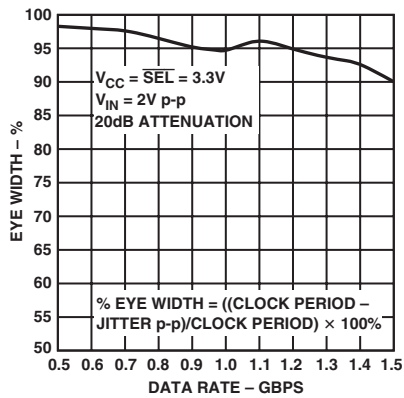
TPC 16. Enable/Disable Time vs. Temperature



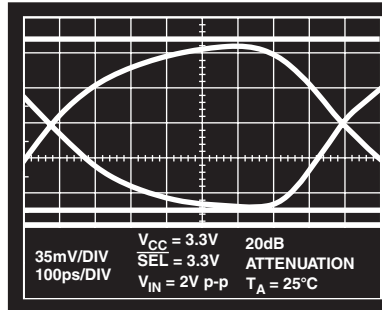
TPC 17. Enable/Disable Time vs. Temperature



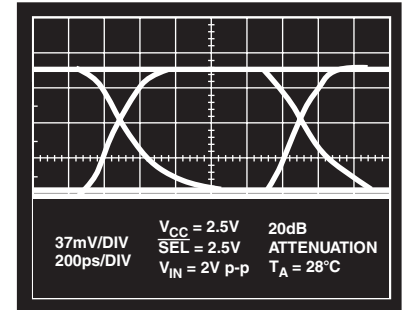
TPC 18. Jitter vs. Data Rate; PRBS 31



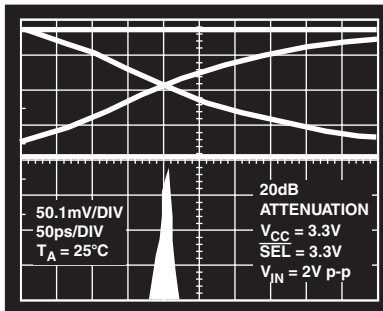
TPC 19. Eye Width vs. Data Rate; PRBS 31



TPC 20. Eye Pattern; 1.244 GBPS,  $V_{CC} = 3.3V$ , PRBS 31



TPC 21. Eye Pattern; 1 GBPS,  $V_{CC} = 2.5V$ , PRBS 31



TPC 22. Jitter @ 1.244 GBPS, PRBS 31

## ADG3246

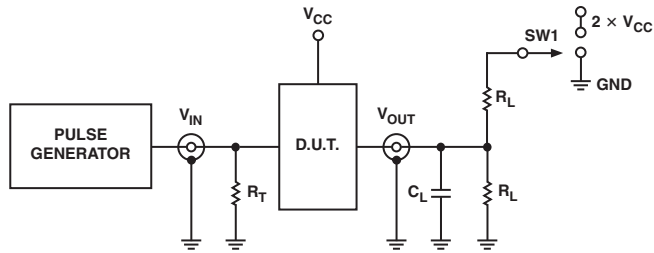
### TIMING MEASUREMENT INFORMATION

For the following load circuit and waveforms, the notation that is used is  $V_{IN}$  and  $V_{OUT}$  where:

$$V_{IN} = V_A \text{ and } V_{OUT} = V_B$$

or

$$V_{IN} = V_B \text{ and } V_{OUT} = V_A$$



**NOTES**  
PULSE GENERATOR FOR ALL PULSES:  $t_R \leq 2.5\text{ns}$ ,  $t_F \leq 2.5\text{ns}$ ,  
FREQUENCY  $\leq 10\text{MHz}$   
 $C_L$  INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES  
 $R_T$  IS THE TERMINATION RESISTOR, SHOULD BE EQUAL TO  $Z_{OUT}$   
OF THE PULSE GENERATOR.

Figure 1. Load Circuit

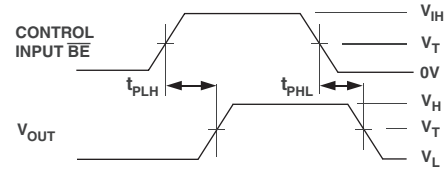


Figure 2. Propagation Delay

### Test Conditions

Symbol	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ( $\overline{\text{SEL}} = V_{CC}$ )	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ( $\overline{\text{SEL}} = V_{CC}$ )	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ( $\overline{\text{SEL}} = 0\text{ V}$ )	Unit
$R_L$	500	500	500	$\Omega$
$V_{\Delta}$	300	150	150	mV
$C_L$	50	30	30	pF
$V_T$	1.5	0.9	0.9	V

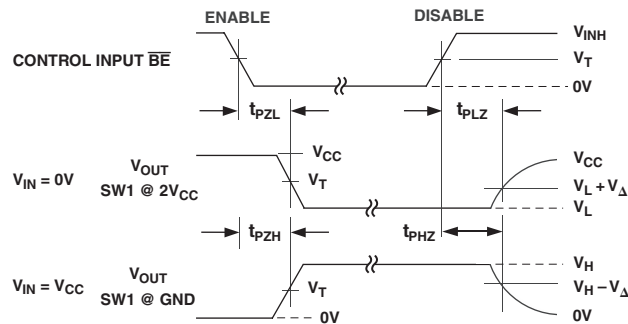


Figure 3. Enable and Disable Times

Table III. Switch Position

TEST	S1
$t_{PLZ}$ , $t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}$ , $t_{PZH}$	GND



**BUS SWITCH APPLICATIONS****Mixed Voltage Operation, Level Translation**

Bus switches can be used to provide an ideal solution for interfacing between mixed voltage systems. The ADG3246 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 3.3 V to 1.8 V, from 2.5 V to 1.8 V, or bidirectionally from 3.3 V directly to 2.5 V.

Figure 4 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs, therefore placing the ADG3246 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

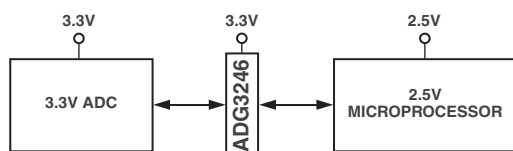


Figure 4. Level Translation between a 3.3 V ADC and a 2.5 V Microprocessor

**3.3 V to 2.5 V Translation**

When  $V_{CC}$  is 3.3 V ( $\overline{SEL} = V_{CC}$ ) and the input signal range is 0 V to  $V_{CC}$ , the max output signal will be clamped to within a voltage threshold below the  $V_{CC}$  supply.

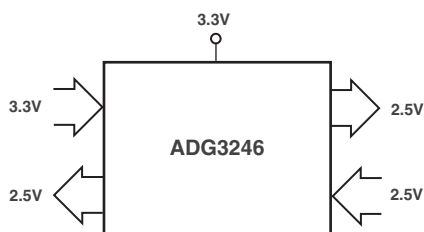


Figure 5. 3.3 V to 2.5 V Voltage Translation,  $\overline{SEL} = V_{CC}$

In this case, the output will be limited to 2.5 V, as shown in Figure 6.

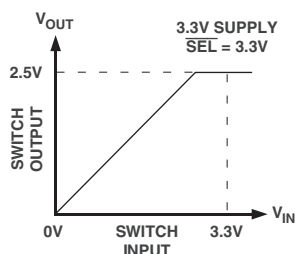


Figure 6. 3.3 V to 2.5 V Voltage Translation,  $\overline{SEL} = V_{CC}$

This device can be used for translation from 2.5 V to 3.3 V devices, and also between two 3.3 V devices.

**2.5 V to 1.8 V Translation**

When  $V_{CC}$  is 2.5 V ( $\overline{SEL} = V_{CC}$ ) and the input signal range is 0 V to  $V_{CC}$ , the max output signal will, as before, be clamped to within a voltage threshold below the  $V_{CC}$  supply.

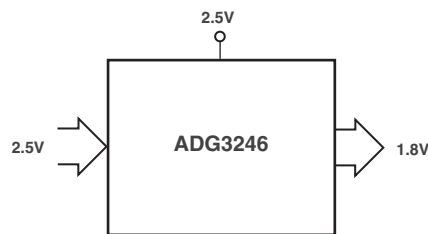


Figure 7. 2.5 V to 1.8 V Voltage Translation,  $\overline{SEL} = V_{CC}$

In this case, the output will be limited to approximately 1.8 V, as shown in Figure 7.

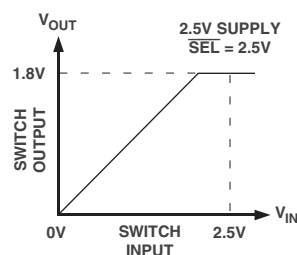


Figure 8. 2.5 V to 1.8 V Voltage Translation,  $\overline{SEL} = V_{CC}$

**3.3 V to 1.8 V Translation**

The ADG3246 offers the option of interfacing between a 3.3 V device and a 1.8 V device. This is possible through use of the  $\overline{SEL}$  pin.

$\overline{SEL}$  pin: An active low control pin.  $\overline{SEL}$  activates internal circuitry in the ADG3246 that allows voltage translation between 3.3 V devices and 1.8 V devices.

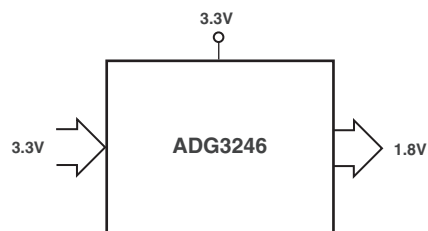


Figure 9. 3.3 V to 1.8 V Voltage Translation,  $\overline{SEL} = 0 V$

When  $V_{CC}$  is 3.3 V and the input signal range is 0 V to  $V_{CC}$ , the max output signal will be clamped to 1.8 V, as shown in Figure 9. To do this, the  $\overline{SEL}$  pin must be tied to Logic 0. If  $\overline{SEL}$  is unused, it should be tied directly to  $V_{CC}$ .

## ADG3246

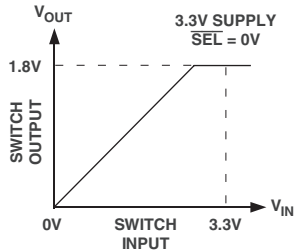


Figure 10. 3.3 V to 1.8 V Voltage Translation,  $\overline{SEL} = 0\text{ V}$

### Bus Isolation

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus bridge devices that extend the number of loads on the bus without exceeding the specifications. Because the ADG3246 is designed specifically for applications that do not need drive yet require simple logic functions, it solves this requirement. The device isolates access to the bus, thus minimizing capacitance loading.

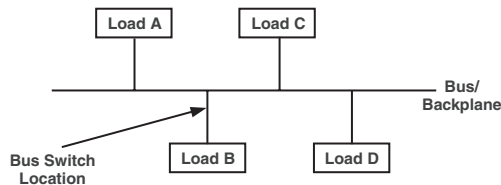


Figure 11. Location of Bus Switched in a Bus Isolation Application

### Hot Plug and Hot Swap Isolation

The ADG3246 is suitable for hot swap and hot plug applications. The output signal of the ADG3246 is limited to a voltage that is below the  $V_{CC}$  supply, as shown in Figures 6, 8, and 10. Therefore the switch acts like a buffer to take the impact from hot insertion, protecting vital and expensive chipsets from damage.

In hot-plug applications, the system cannot be shutdown when new hardware is being added. To overcome this, a bus switch can be positioned on the backplane between the bus devices and the hot plug connectors. The bus switch is turned off during hot plug. Figure 12 shows a typical example of this type of application.

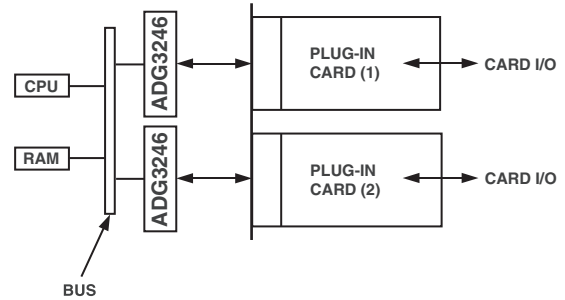


Figure 12. ADG3246 in a Hot Plug Application

There are many systems that require the ability to handle hot swapping, such as docking stations, PCI boards for servers, and line cards for telecommunications switches. If the bus can be isolated prior to insertion or removal, then there is more control over the hot swap event. This isolation can be achieved using a bus switch. The bus switches are positioned on the hot swap card between the connector and the devices. During hot swap, the ground pin of the hot swap card must connect to the ground pin of the back plane before any other signal or power pins.

### Analog Switching

Bus switches can be used in many analog switching applications; for example, video graphics. Bus switches can have lower on resistance, smaller ON and OFF channel capacitance and thus improved frequency performance than their analog counterparts. The bus switch channel itself consisting solely of an NMOS switch limits the operating voltage (see TPC 1 for a typical plot), but in many cases this does not present an issue.

### High Impedance During Power-Up/Power-Down

To ensure the high impedance state during power-up or power-down,  $\overline{BE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### PACKAGE AND PINOUT

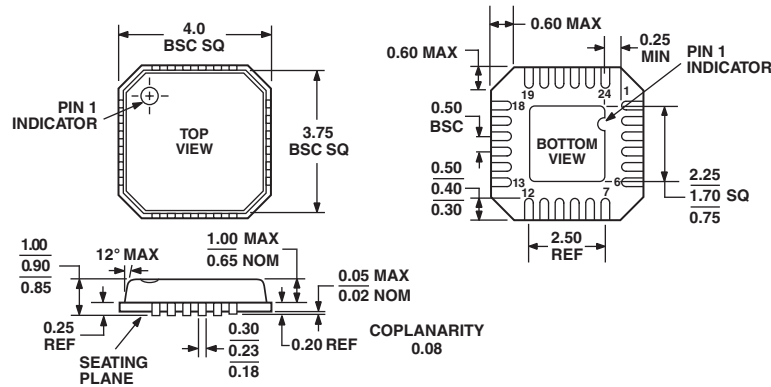
The ADG3246 is packaged in both a small 24-lead TSSOP or a tiny 24-lead LFCSP package. The area of the TSSOP option is  $49.375\text{ mm}^2$ , while the area of the LFCSP option is  $16\text{ mm}^2$ . This leads to a 67% savings in board space when using the LFCSP package compared with the TSSOP package. This makes the LFCSP option an excellent choice for space-constrained applications.

The ADG3246 in the TSSOP package offers a flowthrough pinout. The term *flowthrough* signifies that all the inputs are on opposite sides from the outputs. A flowthrough pinout simplifies the PCB layout.

## OUTLINE DIMENSIONS

**24-Lead Lead Frame Chip Scale Package [LFCSP]**  
**4 × 4 mm Body**  
**(CP-24)**

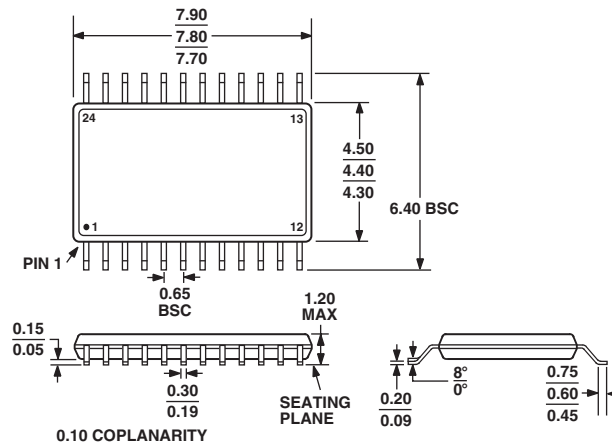
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

**24-Lead Thin Shrink Small Outline Package [TSSOP]**  
**(RU-24)**

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AD

