

T8300/T8300U Phone-On-A-Chip™ IP Solution

Application

- Voice over Internet Protocol (VoIP) telephone.

Solution Features

- Complete VoIP telephone solution:
 - No dependency on external processor.
 - All of the required software components provided in the form of binary and/or source code.
 - Development board with integrated demo voice application using H.323 and session initiation protocol (SIP) protocols.
 - Complete system solution includes *Wind River Systems VxWorks*® real-time operating system (RTOS), *Trillium Digital Systems*® H.323 and SIP, Agere's G.7XX voice codecs.
- High integration requires fewer external components:
 - Integrated Ethernet switch, MACs, PHYs, and codecs.
 - Integrated differential inputs provide high noise immunity for analog signals.
 - Integrated reset control circuit reduces design complexity and board space.

T8300/T8300U Feature Summary

- T8300/T8300U features include:
 - 3.3 V device in 272-pin PBGA package.
 - ARM®940T and DSP1600 cores running at 100 MHz clock speed.
 - 3-port Ethernet switch with integrated dual 10/100 MACs and PHYs.
 - USB 1.1 host controller (T8300U only).
 - IrDA, UART, external memory interface (EMI), SSI, and 16-bit parallel I/O.
 - Two 16-bit DACs; one 16-bit ADC.
 - GCI+ interface, bit I/O, and serial I/O.
 - Three-way hybrid conferencing.
 - G.711 appendices I & II, G.723.1, G.726, G.729A, G.729B, and wideband G.722.
 - Voice activity detection and comfort noise generation.
 - DTMF generation.
 - Acoustic echo cancellation for full-duplex speakerphone.
 - Open listening support.
 - Two differential analog inputs and one single-ended analog input.
 - Two differential analog outputs and one single-ended analog output.

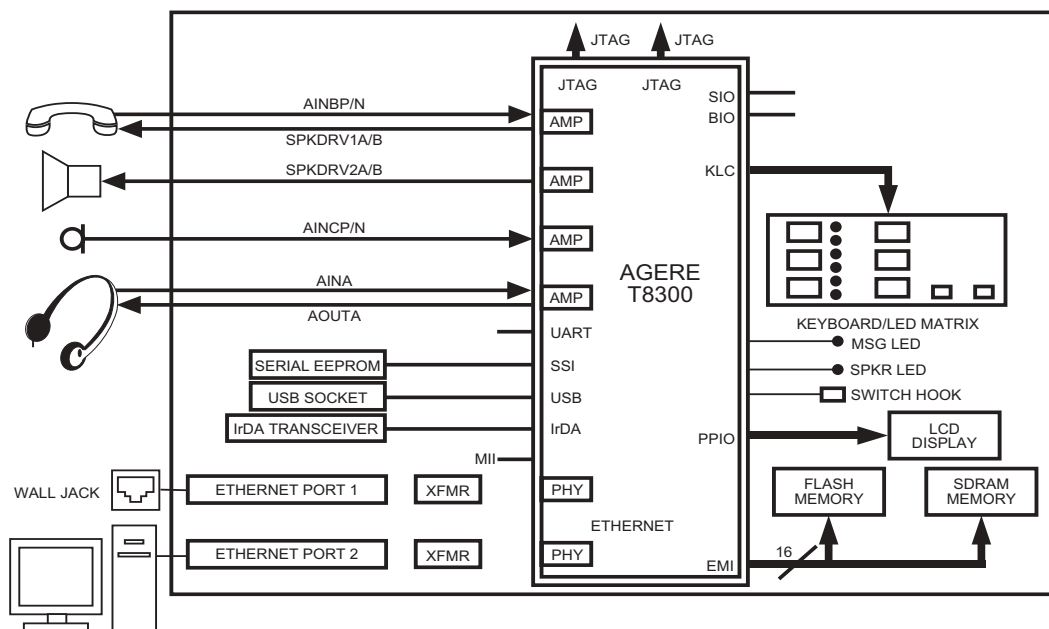


Figure 1. Phone-On-A-Chip Development Board Block Diagram

Description

The *Phone-On-A-Chip* is a complete VoIP single-chip solution. The T8300, along with minimal additional components, provides all the active functions required to implement a complete VoIP based telephone. As shown in Figure 1, chip interfaces have been provided to allow direct integration into a system design; reducing time to market, implementation risk, and component cost. The network interface is implemented as an autonegotiating 10/100 Mbits/s Ethernet based LAN. The chip includes a complete three-port Ethernet subsystem implemented as a three-port switch (two external, one internal) with priority queuing running at 10/100 Mbits/s. A fully functional MII interface facilitates other external PHYs compatible with 802.3 MAC.

T8300/T8300U Detailed Features

Microprocessor Features

- Core:
 - ARM940T core with 4 Kbyte instruction cache and 4 Kbyte data cache.
 - Clock speed of 100 MHz (110 MIPS).
 - System memory interface to ARM with support for SDRAM, Flash, and SRAM.
 - 1 K x 32 on-chip SRAM.
- Peripherals:
 - Ethernet:
 - 3-port Ethernet switch.
 - Three integrated 802.3 MAC controllers.
 - Two integrated 10/100 Mbits/s PHYs.
 - Two hardware queues per Ethernet port for handling priority processing of voice traffic per IEEE[®] 802.1p and 802.1q.
 - VLAN support with tag insertion, tag deletion, tag modification.
 - Hardware support for network management (SNMP/RMON).
 - USB 1.1 host controller (available in T8300U).
 - IrDA infrared communication interface.
 - UART interface.
 - Synchronous serial communications controller and interface.
 - 16-bit parallel I/O.
 - LED control interface for 72 LEDs.
 - Keyboard scan circuitry with support for 72 keys.
 - Four general-purpose timers.
 - Real-time clock.
 - JTAG support for ARM development tools.
- Software:
 - Objects:
 - ITU-T H.323 and IETF SIP protocol stacks.

- RTP/RTCP.
- Sample source code:
 - H.323 and SIP phone sample application.
 - API wrapper to interface with the *Trillium* H.323 and SIP protocol stacks.
 - Board support package (BSP) for *Phone-On-A-Chip* development board.
 - Complete set of device drivers.
 - Source code for DSP API and sample jitter buffer management.
- Target license for *VxWorks* RTOS along with TCP, UDP, and IP.

Digital Signal Processor Features

- Core:
 - DSP1600 core with 48 K x 16 ROM and 16 K x 16 RAM (zero wait-state, DPRAM); 12 K SRAM (single wait state) data.
 - DSP clock speed of 100 MHz.
 - GCI interface.
 - Two timed DMA outputs for simultaneous handset and speaker audio output.
 - Two serial I/O interfaces.
 - Bit I/O interface.
 - General-purpose timer counter.
- Peripherals:
 - Low-pass filtering on audio inputs and outputs.
 - 16-bit analog-to-digital converter.
 - Two 16-bit digital-to-analog converters.
 - Programmable gain amplifier on audio input.
 - Two differential and one single-ended audio input for use with speakerphone, handset, and/or headphone.
 - Fixed gain amplifier for differential inputs.
 - One single-ended audio output to drive a standard 150 Ω handset speaker.
 - Two sets of differential audio outputs to drive 125 mW into 16 Ω speakers.
- Software:
 - G.711 Appendices I & II, G.723.1, G.726, and G.729A, G.729B, wideband G.722.
 - Voice activity detection.
 - Local loop support, dial tone, busy tone, call waiting tone, ring-back tone, and network busy tone.
 - Comfort noise generation.
 - Acoustic echo cancellation for full-duplex speakerphone.

General Features

- Additional features include:
 - 3.3 V device in 272-pin PBGA package.
 - JTAG boundary-scan capability.
 - JTAG tools (debug) capability.
 - Only two external crystals required.

The Chip Set Functions

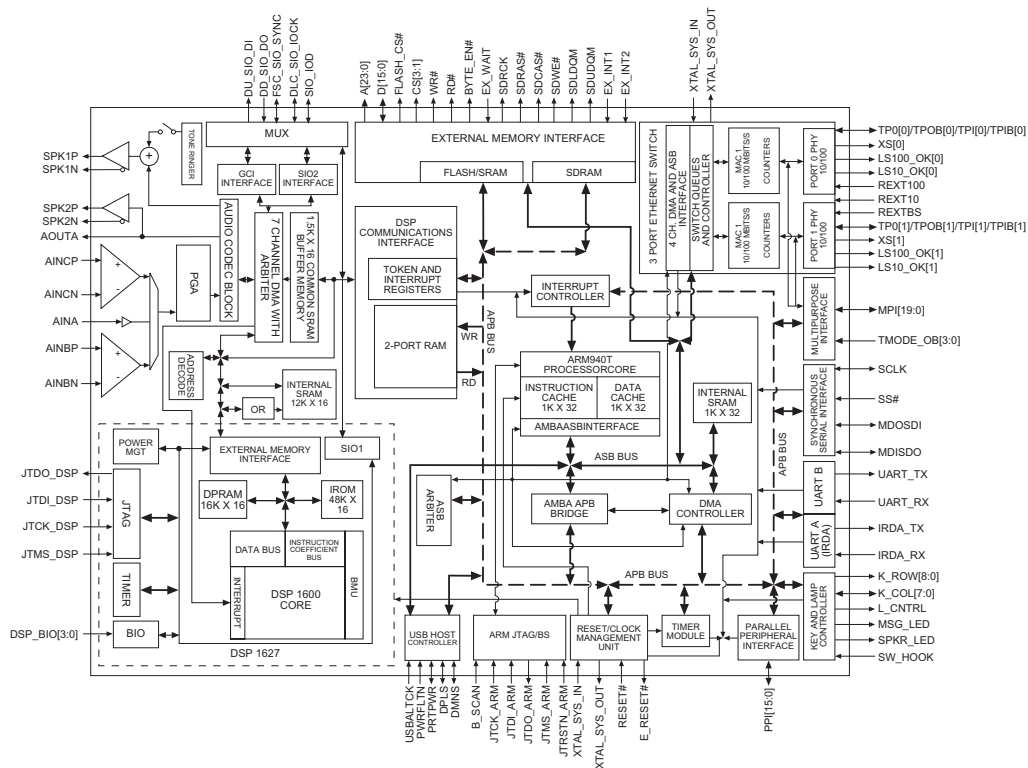


Figure 2. T8300/T8300U Block Diagram

The chip functions are depicted in the *Phone-On-A-Chip* block diagram above. Some of the key functions included in this chip are described in the following two sections.

Integrated Amplifiers

All the gain amplifiers are integrated on the T8300, eliminating the need for external amplification.

Adaptable Acoustic Echo Cancellation

The adaptable acoustic echo cancellation algorithm automatically adjusts the AEC for the environment (room size, telephone housing, etc.).

Tone Generation

DTMF, ringing, and call progress tones are generated by the T8300. The particular tone is selected via an API command.

Integrated PHY

The two external ports from the Ethernet switch are integrated with 802.3 MACs and PHYs configurable for 10/100 Mbps/s, full-/half-duplex. This eliminates the need for external PHYs and allows the board to have a

smaller footprint. A second Ethernet port provides the ability to connect a PC to the network through the *Phone-On-A-Chip* based telephone. Transfer of data between the IP telephone, PC, and the network is possible.

Prioritization of Real-Time Data

QoS support is provided in accordance with *IEEE* 802.1p and 802.1q.

Data and Instruction Cache

The ARM940T processor core offers the benefit of 4 Kbytes instruction cache and 4 Kbytes data cache.

Advantages of *Phone-On-A-Chip*

Lower Total System Cost

Phone-On-A-Chip eliminates the need for expensive glue logic. All the required interfaces such as keypad, LED, amplifiers, and PHYs are integrated within the device. The bundled target license fee for *Trillium Digital Systems* H.323, SIP, RTP/RTCP protocol stack, and *Wind River Systems VxWorks* RTOS reduces cost.

Advantages of *Phone-On-A-Chip*

(continued)

High Sound Quality

The differential amplifiers for the speaker and the microphone are integrated into the chip, providing very high sound quality at low cost.

Reduced Development Time

A development kit bundled with the required sample source code and binaries gives a jump start for the development of application code that can easily be migrated to target products. This development board can be easily shrunk into a cost-effective solution.

High Performance and QoS

QoS support is provided in accordance with *IEEE* 802.1p and 802.1q. A four-channel DMA ensures fast data transfers between user interfaces and memories to supplement the performance.

Extended Alliance Programs

Agere has formed alliances with industry leaders to ease product development enabling fast time to market. Relationships with *Wind River Systems* and *Trillium Digital Systems* provide value pricing for integration of hardware and software. Agere has qualified RealTime Digital Inc. as a third-party vendor to customize the DSP code parameters.

Industry Proven Functionality

The T8300 mitigates development risk by integrating the proven functionality of Agere's T8301/T8302 VoIP phone chip set into a single chip solution. The T8301/T8302 has been successfully deployed by VoIP phone manufacturers. Therefore, the T8300 incorporates a

proven design with field tested software.

Building a System with *Phone-On-A-Chip*

A development kit has been designed to help customers expedite their product launch by reducing the development cycle significantly. The development kit provides a turnkey demo solution to plug and play with the H.323 and SIP protocol stack based applications. The development design kit includes the following:

- Welcome letter and a getting started guide.
- Two complete IP telephone development boards.
- Integrated solution including H.323 and SIP based sample application to allow quick evaluation.
- CD including all the binaries, sample source code, all necessary documentation, and tools.
- Schematic diagrams, PCB layout source files, and bill of materials.
- Development board layout files.
- *Phone-On-A-Chip* device datasheets.
- Application notes.
- FAE regional customer support for one year.

This integrated solution approach provides a self-contained VoIP telephone solution, allowing our customers to concentrate on system-related issues. The development kit reference design can easily be adapted to provide a commercial product.

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For additional information, contact your Agere Systems Account Manager or the following:

INTERNET: <http://www.agere.com>

E-MAIL: docmaster@agere.com

N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286

1-800-372-2447, FAX 610-712-4106 (In CANADA: 1-800-553-2448, FAX 610-712-4106)

ASIA: Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon

Tel. (852) 3129-2000, FAX (852) 3129-2020

CHINA: (86) 21-5047-1212 (Shanghai), (86) 10-6522-5566 (Beijing), (86) 755-695-7224 (Shenzhen)

JAPAN: (81) 3-5421-1600 (Tokyo), KOREA: (82) 2-767-1850 (Seoul), SINGAPORE: (65) 778-8833, TAIWAN: (886) 2-2725-5858 (Taipei)

EUROPE: Tel. (44) 1344 296 400

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