

# 74FR245

## Octal Bidirectional Transceiver with 3-STATE Outputs

### General Description

The 74FR245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B Ports. The Transmit/Receive ( $\overline{T/R}$ ) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a High Z condition.

### Features

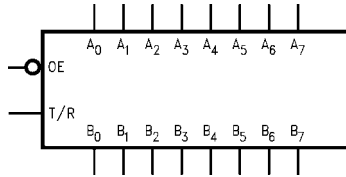
- Non-inverting buffers
- Bidirectional data path
- A and B output sink capability of 64 mA, source capability of 15 mA
- Guaranteed pin-to-pin skew

### Ordering Code:

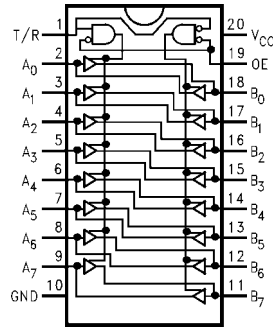
Order Number	Package Number	Package Description
74FR245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74FR245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active-LOW)
$\overline{T/R}$	Transmit/Receive Input
$A_0$ - $A_7$	Side A Inputs or 3-STATE Outputs
$B_0$ - $B_7$	Side B Inputs or 3-STATE Outputs

### Truth Table

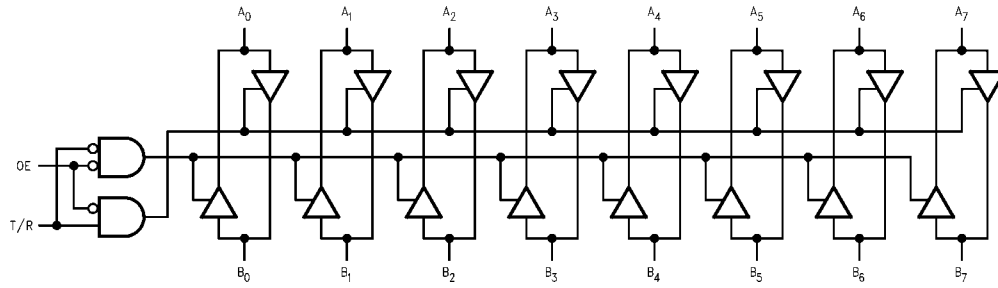
Inputs		Output
$\overline{OE}$	$\overline{T/R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

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### Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

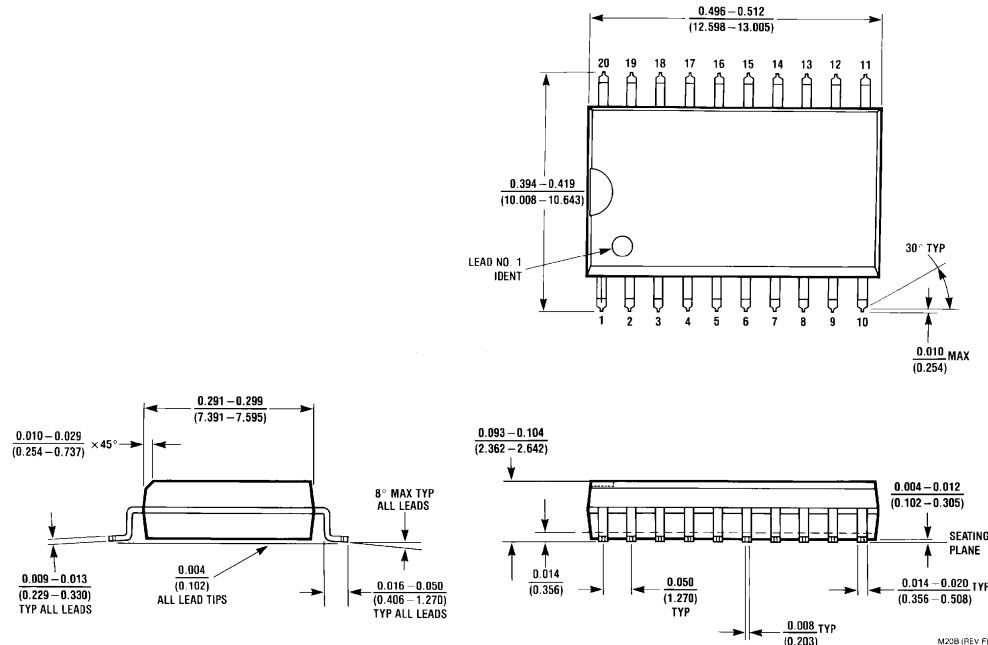
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

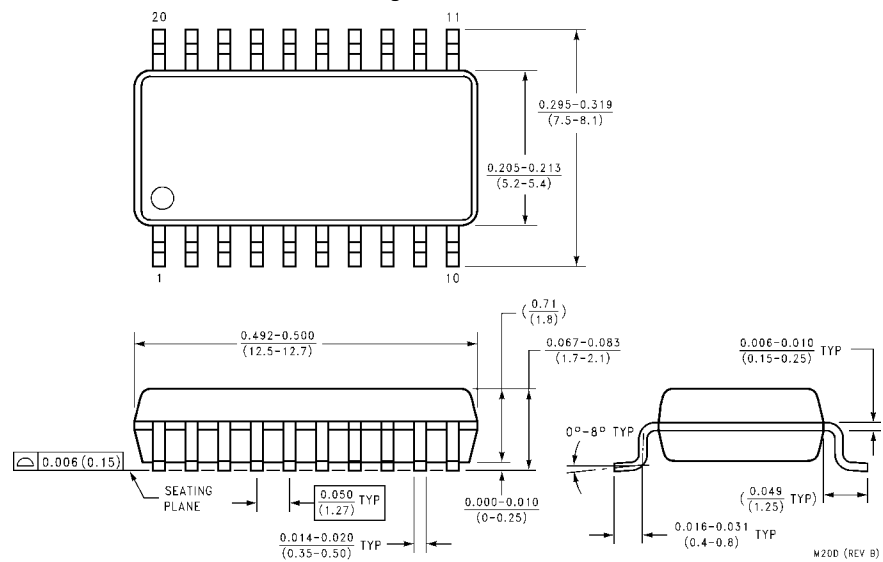
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	Min	I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		2.0			V	Min	I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V ( $\overline{OE}$ , $\overline{T/R}$ )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE}$ , $\overline{T/R}$ )
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			-250	μA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , $\overline{T/R}$ )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			25	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-150	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0.0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		55	75	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current		75	110	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current		55	75	mA	Max	Outputs 3-STATE
C <sub>IN</sub>	Input Capacitance		8.0		pF	5.0	$\overline{OE}$ , $\overline{T/R}$
			17.0		pF	5.0	A <sub>n</sub> , B <sub>n</sub>

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.0	2.6	3.9	1.0	3.9	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.0	1.7	3.9	1.0	3.9	
t <sub>PZH</sub>	Output Enable Time	2.5	5.0	7.0	2.5	7.0	ns
t <sub>PZL</sub>		2.5	4.3	7.0	2.5	7.0	
t <sub>PHZ</sub>	Output Disable Time	1.7	3.7	6.5	1.7	6.5	ns
t <sub>PLZ</sub>		1.7	3.6	6.5	1.7	6.5	
Extended AC Characteristics							
Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF Eight Outputs Switching (Note 3)		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 250 pF (Note 4)		Units	
		Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	1.0	5.9	2.5	7.5	ns	
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.0	5.9	2.5	7.5		
t <sub>PZH</sub>	Output Enable Time	2.5	11.9			ns	
t <sub>PZL</sub>		2.5	11.9				
t <sub>PHZ</sub>	Output Disable Time	1.3	6.5			ns	
t <sub>PLZ</sub>		1.3	6.5				
t <sub>OSSL</sub> (Note 5)	Pin to Pin Skew for HL Transitions		1.7			ns	
t <sub>OSLH</sub> (Note 5)	Pin to Pin Skew for LH Transitions		1.0			ns	
t <sub>OSt</sub> (Note 5)	Pin to Pin Skew for HL/LH Transitions		3.3			ns	
<p><b>Note 3:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.</p> <p><b>Note 4:</b> These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p><b>Note 5:</b> Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t<sub>OSSL</sub>), LOW-to-HIGH (t<sub>OSLH</sub>), or HIGH-to-LOW and/or LOW-to-HIGH (t<sub>OSt</sub>). Specifications guaranteed with all outputs switching in phase.</p>							

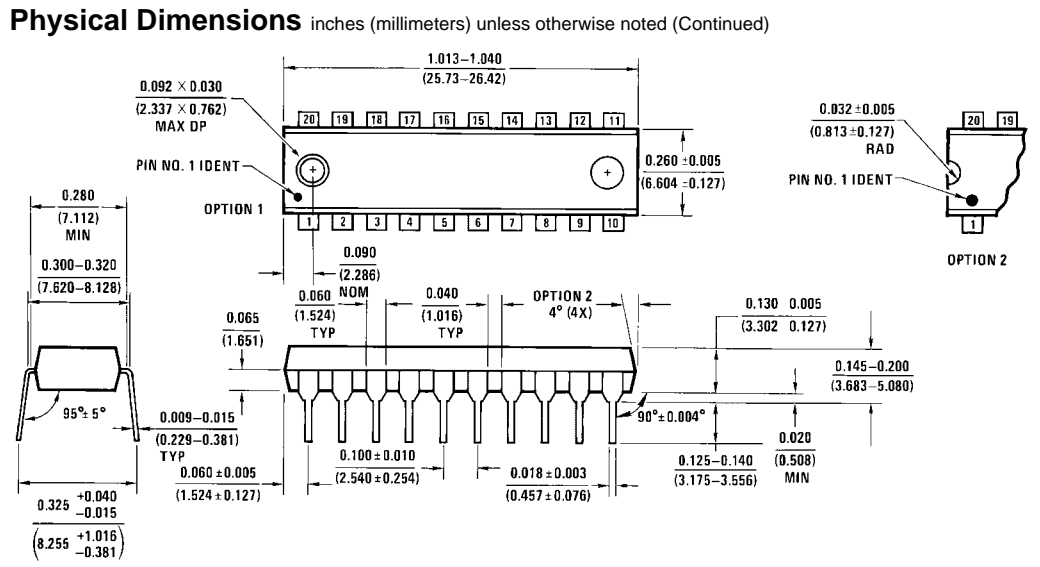
**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A**

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