

# 74LVX541

## Low Voltage Octal Buffer/Line Driver with 3-STATE Outputs

### General Description

The LVX541 is an octal non-inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

### Features

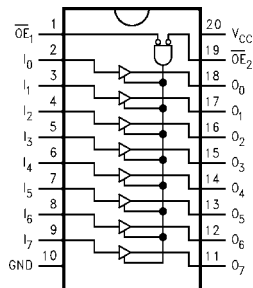
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

### Ordering Code:

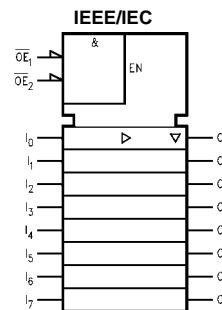
Order Number	Package Number	Package Description
74LVX541M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Logic Symbol



### Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0 - I_7$	Inputs
$O_0 - O_7$	3-STATE Outputs

### Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

74LVX541 Low Voltage Octal Buffer/Line Driver with 3-STATE Outputs

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to +3.6V
Input Voltage ( $V_I$ )	0V to +5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	2.0	1.5			1.5		V	
		3.0	2.0			2.0			
		3.6	2.4			2.4			
$V_{IL}$	LOW Level Input Voltage	2.0		0.5			0.5	V	
		3.0		0.8			0.8		
		3.6		0.8			0.8		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$
		3.0	2.9	3.0		2.9			
		3.0	2.58			2.48			
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$
		3.0		0.0	0.1		0.1		
		3.0			0.36		0.44		
$I_{OZ}$	3-STATE Output OFF-State Current	3.6			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND
$I_{IN}$	Input Leakage Current	3.6			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND
$I_{CC}$	Quiescent Supply Current	3.6			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND

**Noise Characteristics** (Note 3)

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.5	0.8	V	$C_L = 50 \text{ pF}$
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.5	-0.8	V	$C_L = 50 \text{ pF}$
$V_{IHD}$	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	$C_L = 50 \text{ pF}$
$V_{ILD}$	Maximum HIGH Level Dynamic Input Voltage	3.3		0.8	V	$C_L = 50 \text{ pF}$

**Note 3:** Input  $t_r = t_f = 3 \text{ ns}$ .

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time	2.7	6.1	11.3	1.0	13.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PHL</sub>			8.6	14.9	1.0	17.0		C <sub>L</sub> = 50 pF	
		3.3 ± 0.3	4.7	7.0	1.0	8.5		C <sub>L</sub> = 15 pF	
			7.2	10.5	1.0	12.0		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub>	3-STATE Output Enable Time	2.7	7.1	13.8	1.0	16.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PZH</sub>			9.6	17.3	1.0	20.0		R <sub>L</sub> = 1 kΩ	
		3.3 ± 0.3	6.8	10.5	1.0	12.5		C <sub>L</sub> = 50 pF	
			9.3	14.0	1.0	16.0		R <sub>L</sub> = 1 kΩ	
t <sub>PLZ</sub>	3-STATE Output	2.7	11.6	17.9	1.0	20.0	ns	C <sub>L</sub> = 50 pF	
t <sub>PHZ</sub>	Disable Time	3.3 ± 0.3	10.7	15.4	1.0	17.5		R <sub>L</sub> = 1 kΩ	
t <sub>OSLH</sub>	Output to Output	2.7		1.5		1.5	ns	C <sub>L</sub> = 50 pF	
t <sub>OSSL</sub>	Skew (Note 4)	3.3		1.5		1.5			

**Note 4:** Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PHLn}|$ ;  $t_{OSSL} = |t_{PHLm} - t_{PLLn}|$ .

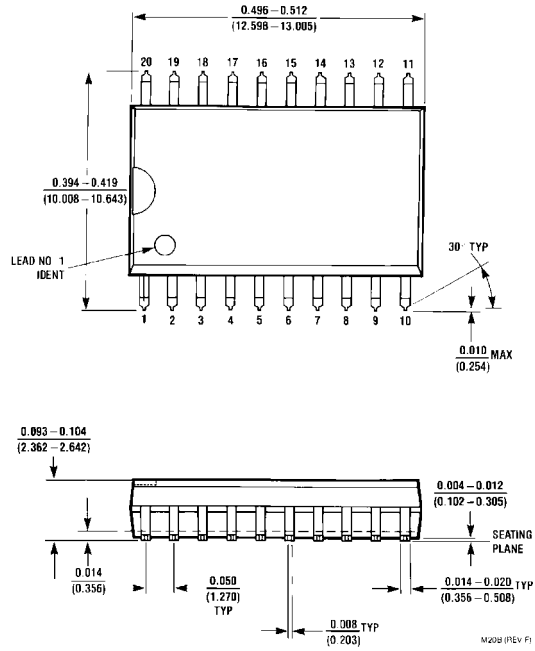
## Capacitance

Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)		19				pF

**Note 5:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr.})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$$

**Physical Dimensions** inches (millimeters) unless otherwise noted

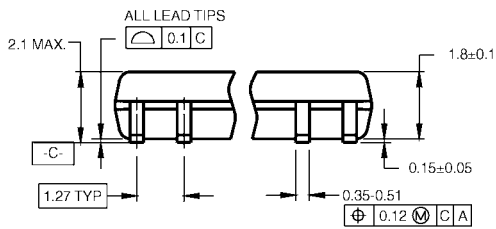


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B**

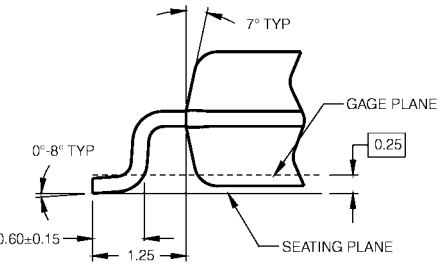
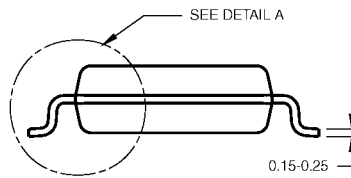
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



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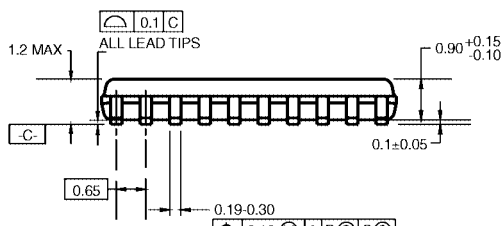
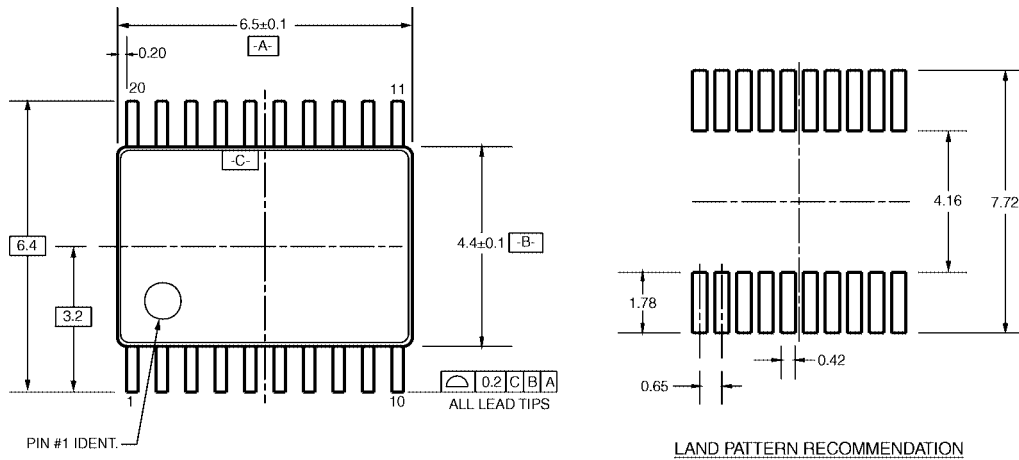
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

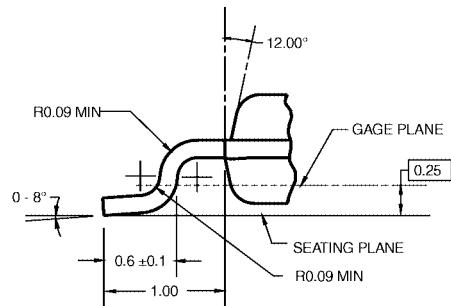
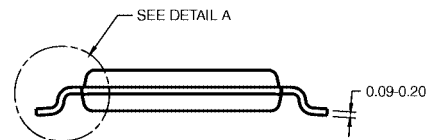


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

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