TC8250P TC8250AP

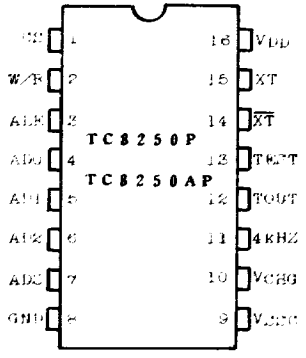
REAL TIME CLOCK

1. INTRODUCTION

The TC8250P or TC8250AP is a single chip C-MOS LSI for real time clock, which is composed as a peripheral LSI of a microcomputer.

The RTC has a 32768Hz X'tal oscillation circuit, counter group for clocking, control circuit for read/write from CPU, and battery backup terminal. The package is a 16 pin DIP, and a non-power interruption type clock system can be realized with I/O ports, X'tal and battery.

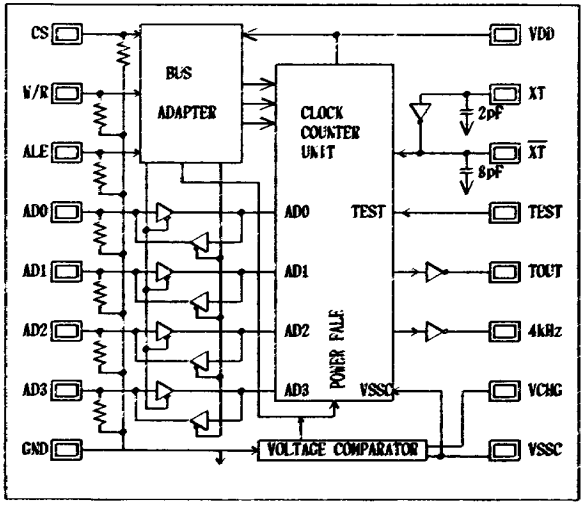
The input terminals for the CPU have pull-down registers in the TC8250P. The TC8250AP has no pull-down registers.



PIN ASSIGNMENT (Top View)

2. FEATURES

- o Low Power Consumption
- o 32,768Hz X'tal Oscillation Circuit
- o Counts Seconds, Minutes, and Hours
- o Counts Days of the Week, Date, Month, and Year.
- o Automatic Leap Year Compensation
- o Battery Back-up function with Low Voltage Detector
- o Battery Charge Control Terminal (VCHG)
- o Signal output (2048Hz - 1Hz, 1 minute, 10 minutes. programmable)
- o Write Protect Key for sure operation
- o 4 bit Multiplexed Bus
- o 16-pin DIP



BLOCK DIAGRAM (TC8250P)

3. Description of Pin Function

o VDD +5V Volt supply.

o GND Ground

o VSSC -3V to VDD terminal supplies for clock logic.

o VCHG The battery charging terminal. Connect this terminal to the minus terminal of the battery via the current limit resister. A built-in transistor is cut off, when the system supply voltage (supplied to VDD) is below battery voltage.

o 4KHz (Signal output)
4KHz signal obtained by dividing a clock from the X'tal (32768Hz) is outputted by the 5V circuit Duty: 50% - 50%

o TOUT (Signal output)
The terminal for outputting 2KHz to 1Hz, 1 minute and 10 minutes outputs by the internal program.

o CS (Chip select)
When this signal is High, Read or Write operation (by W/R terminal) is executed for address pointed to by the internal address latch.

o W/R (Read/Write control)

CS	W/R	AD0 to AD3
0	x	Hi-Z, input mode
1	0	Counter -> Data Bus
1	1	Data Bus -> Counter

When both CS and W/R are High, the write operation to the clock chip is executed. When cs is High and W/R is Low, the read operation from the clock chip is executed.

o ALE (Address latch enable)
When this signal is placed at High level, contents of AD0 to AD3 are taken into the internal address latch of the clock chip.

o AD0 to AD3 (Address data bus)
The bidirectional data bus (4 bits) is used to exchange data and address with CPU side.

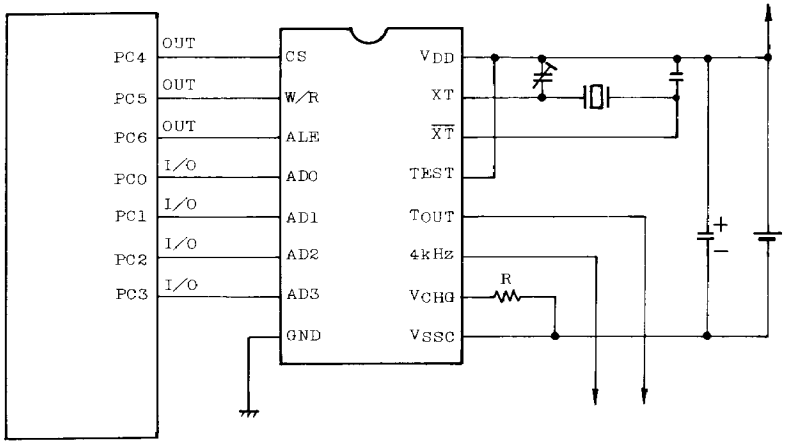
4. System Configuration

The RTC can be used in two connecting method of VCHG. Shown in system configuration (1) is a case in which a private battery is provided to the RTC with +5V used as the common terminal. System Configuration (2) shows a case in which GND side is used commonly and 5 to 3V is applied depending upon availability of main power.
Two kinds of connecting methods are selected according to the configuration of the entire system. Both system configurations are as follows.

System Configuration (1)

When no device is backed up besides RTC, the control circuit for back-up can be omitted.

As 3V from the battery is fixedly supplied to the clock counter unit, the accuracy of clocking operation can be improved.

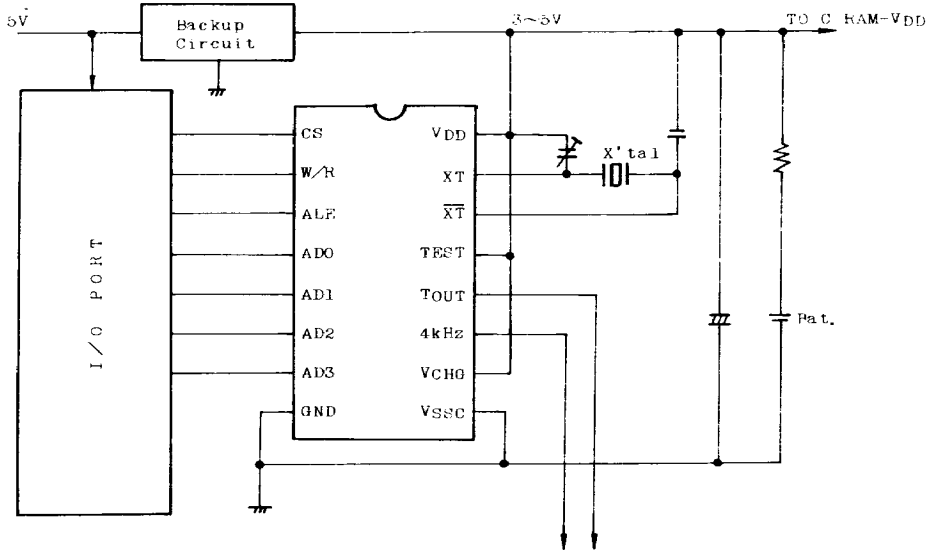


System Configuration (1)

System Configuration (2)

The RTC can be connected in parallel to such back up devices as C-RAM, etc.

(Note) When the VCHG level is lower than VSSC, the battery backup function by VCHG is active. (System Configuration (1))
When the VCHG terminal is connected to VDD, VSSC and GND must be connected. (System Configuration (2))



System Configuration (2)

5. Functional Description

5.1 Data I/O Method

There are 16 kinds of addresses inside the RTC, which are controlled by the 4 bit address line. These addresses are shown in the following table.

Content of Adrs.latch A3 A2 A1 A0	Hex.	Write Data D3	D2	D1	D0	Read Data D3	D2	D1	D0	Remarks
0 0 0 0	0	8(s)	4(s)	2(s)	1(s)	<-	<-	<-	<-	1 sec. digit
0 0 0 1	1	- (*)	40(s)	20(s)	10(s)	0	<-	<-	<-	10 secs. digit
0 0 1 0	2	8(m)	4(m)	2(m)	1(m)	<-	<-	<-	<-	1 min. digit
0 0 1 1	3	-	40(m)	20(m)	10(m)	0	<-	<-	<-	10 mins. digit
0 1 0 0	4	8(h)	4(h)	2(h)	1(h)	<-	<-	<-	<-	1 hour digit
0 1 0 1	5	-	40(h)	20(h)	10(h)	0	0	<-	<-	10 hours digit
0 1 1 0	6	8(d)	4(d)	2(d)	1(d)	<-	<-	<-	<-	1 day digit
0 1 1 1	7	-	40(d)	20(d)	10(d)	0	0	<-	<-	10 days digit
1 0 0 0	8	8(M)	4(M)	2(M)	1(M)	<-	<-	<-	<-	1 month digit
1 0 0 1	9	L1 (**)	L0 (**)	-	10(M)	<-	<-	LY (**)	<-	10 months digit
1 0 1 0	A	8(Y)	4(Y)	2(Y)	1(Y)	<-	<-	<-	<-	1 year digit
1 0 1 1	B	80(Y)	40(Y)	20(Y)	10(Y)	<-	<-	<-	<-	10 years digit (***)
1 1 0 0	C	-	W2	W1	W0	0	<-	<-	<-	Day of the week
1 1 0 1	D	T3	T2	T1	T0	<-	<-	<-	<-	TOUT Control
1 1 1 0	E	X3	X2	X1	X0					KEY (****)
1 1 1 1	F	-	1 <- sec. reset>					busy	Xbusy	Status (*****)

(*) : "-" is ignored at write operation.
(**) : Leap-year control bit.
(***) : Day of the week is a numeral 0 to 6.
(****) : PROTECTION KEY
(*****) : Internal state check bit

[Note] The meaning of abbreviated letter in the above table are as below.

(s): second (m): minute (h): hour
(d): day (M): month (Y): year

5.2 WRITE operation

At first, data on AD0 to AD3 is set into address latch by ALE strobe. When both CS and W/R are High, data on AD0 to AD3 is written to a internal register (counter) pointed to by the address latch.
In this case, "5" must have been written into "PROTECT KEY" (address OE_{16}) in advance.

The means of PROTECT KEY will be as follows:
KEY = 5 : All registers are writable.
KEY ≠ 5 : No writable except PROTECT KEY.

Further, System Configuration (1), if GND-VSSC > 0.5, it is regarded as the power failure state and the content of PROTECT KEY is automatically reset.

5.3 READ operation

Set register address to read out in the same manner as in WRITE operation. Then, when CS is put at High level at W/R=Low, the register content is outputted to AD0 to AD3.

5.4 Usage

It is necessary to control READ/WRITE operation so that it does not compete with the counting operation of the clock counter. To sense the counting operation of RTC from the host machine side, status is used. Status is read out by setting 15 (OF_{16}) in the address register. Low order 2 bits of the content of the status register shown in the following figure are significant.

D3	D2	D1	D0
-	-	busy	Xbusy

busy : busy denotes the sectional pulse itself, which synchronizes with one second clock in RTC. The relation between this pulse and the internal pulse is illustrated in Fig. 5.1.

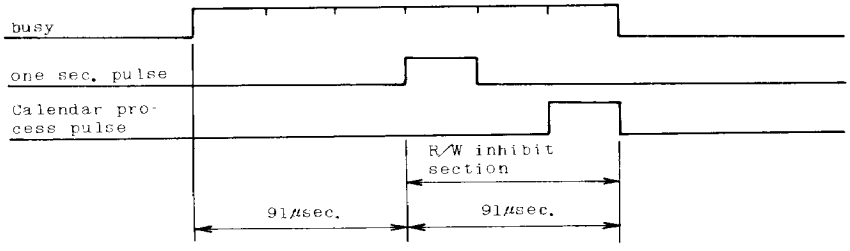


Fig. 5.1 Relation between Internal Pulse and Busy

Xbusy : Xbusy is able to read output of F.F. which is set by the busy signal and reset by the status read strobe treading edge. It's internal circuit and waveform timing are shown in Fig. 5.2.

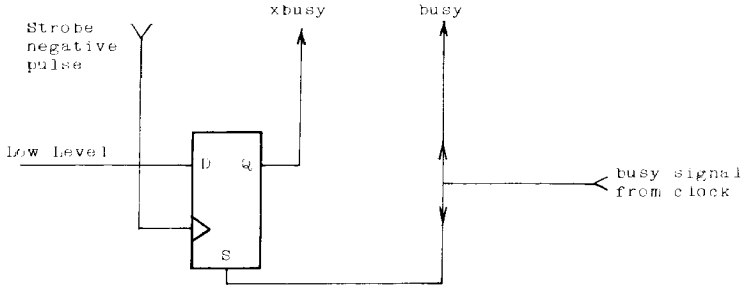


Fig. 5.2(a) Xbusy Circuit

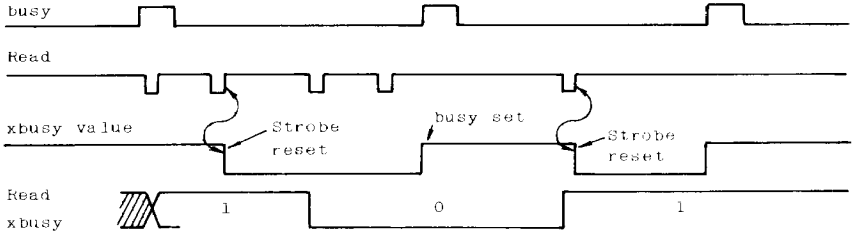


Fig. 5.2(b) Timing of Xbusy

From Xbusy value it can be seen if there is one second count between the read timing of this time and that of the last time.

(1) When it is clear that a series of counter reads or writes completes within 91 usec [for instance, read of second only, write of hour only (time difference correction)], the "busy" flag is used.
The program flow in this case is shown in Fig. 5.3.

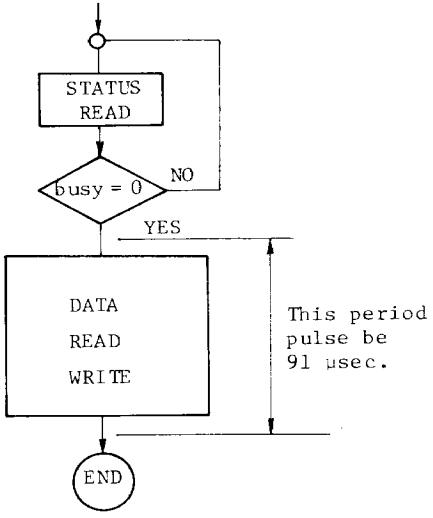


Fig. 5.3 Program Flow (1)

(2) When a series of counter reads requires more than 91 usec, the "xbusy" flag is used. This is such an occasion, for instance, where time data such as year, month, day, day of week, hour, min., sec., are all taken in. At this time, if clock count pulses are inserted during read, data before and after the pulse insertion may become wrong. The way of checking "xbusy" flag to detection the clock count pulse is effective. As the clock count is occured once per second, even if the first trial is not good, next trial is surely successful. (Note : It is assumed that a time for a series of reads is sufficiently shorter than one second.) The program flow at this time is shown in Fig. 5.4.

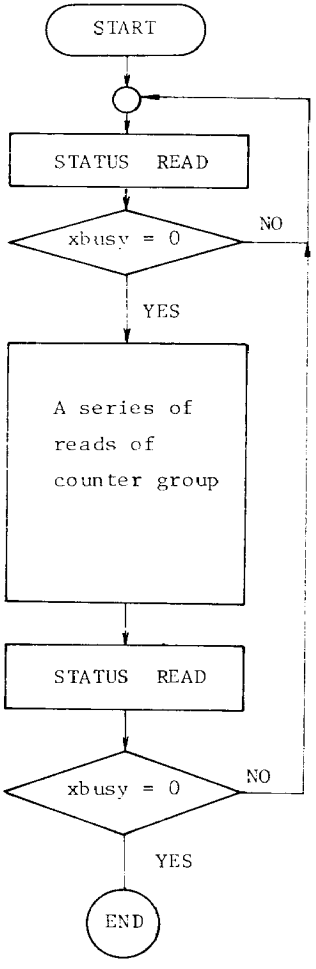


Fig. 5.4 Program Flow (2)

(3) Use of Second Reset

WRITE operation of ADR="OF_{16}" resets the second counter to zero. When the second counter is above 30, carry to the minutes counter is generated. In the inside of RTC "busy" signal is once ON to perform the same process as in the normal second carry. This can be used as the beginning of a series of counter write operations like the initializing sequence of the clock counter. The program flow in this case is shown in Fig. 5.5.

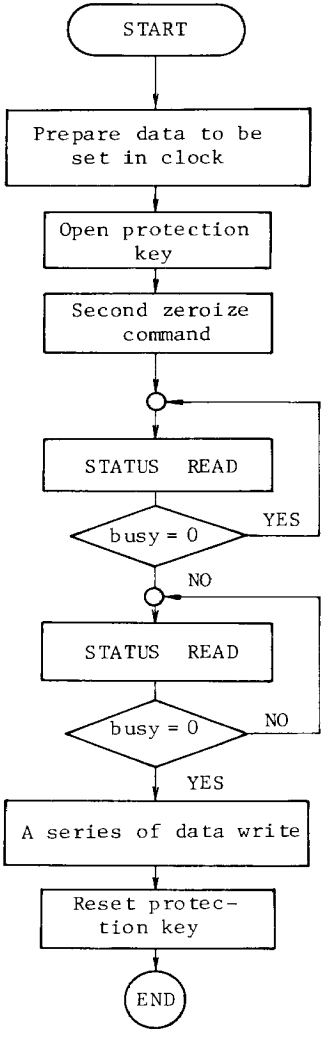


Fig. 5.5 Program Flow (3)

5.5 Leap-year control

The year counter (address OA_{16}, OB_{16}) is a 00 to 99 year counter by decimal (BCD) 2 digits.
A leap-year is designated by values of L1 and L0 at the high order of the ten-month digit counter.

L1	L0	Leap-year
0	0	Year when the remainder of the year counter is 0.
0	1	Year when the remainder of the year counter is 1.
1	0	Year when the remainder of the year counter is 2.
1	1	Year when the remainder of the year counter is 3.

That is, when the 2 digit year counter is treated as low order 2 digits of A.D., L1=L0=0 is set.

Note) At present, the leap-years are defined to be those years out of A.D. years that can be divided by 4, except those years that can be divided by 100 but cannot be divided by 400. Therefore, there are leap-year every 4 years during the period from 1901 to 2099.

In this connection, when a year number of Showa is set, years with the remainder of Showa of 3 [the 55th (1980), 59th (1984) ... year of Showa] are the leap-years and therefore, L1=1, L0=1 are set. In the leap-year, 29th February is indicated following 28th February. In the other year, 1st March is indicated. Further, when the year is the leap-year, D1=1 is read if the ten-month digit is read.

5.6 TOUT signal program

It is possible to program TOUT signal according to the value to be set in address OD_{16}.

Set Value	TOUT Output	Duty ratio
0	1 Hz pulse	50%
1	2 Hz pulse	"
2	4 Hz pulse	"
3	8 Hz pulse	"
4	16 Hz pulse	"
5	32 Hz pulse	"
6	64 Hz pulse	"
7	128 Hz pulse	"
8	256 Hz pulse	"
9	512 Hz pulse	"
10	1024 Hz pulse	"
11	2048 Hz pulse	"
12	1 min. pulse	Pulse width 30.5us positive pulse
13	10 mins.pulse	"
14	TOUT=VDD fixed	-
15	TOUT=VSS fixed	-

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATINGS	UNITS
Supply Voltage (1)	VDD	-0.5 to +7.0	V
Supply Voltage (2)	VDD-VSSC	-0.5 to +7.0	V
Input Voltage	VI	VSS(C)-0.5 to VDD+0.5	V
Operating Temperature	Topr	-40 to 85	^{o}C
Storage Temperature	Tstg	-65 to +125	^{o}C

6.2 D.C. CHARACTERISTICS

(Ta=-40~85^{o}C, VDD=+5V, VDD-VSSC=+3V)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS MIN.	RATINGS MAX.	UNITS
Input Low Voltage	VIL		-0.3	0.8	V
Input High Voltage	VIH		2.0	VDD+0.3	V
Input Low Current	IIL	VIL=0v	-1		uA
Input High Current (1) (AD0 to 3)	IIH1	VIH=VDD	0.15	0.5 (note)	mA
Input High Current (2) (CS, W/R, ALE)	IIH2	VIH=VDD	0.45	0.8 (note)	mA
Output Low Current(1)-1 (AD0 to 3)	IOL1-1	VOL=0.4V	0.75		mA
Output Low Current(2)-1 (Tout,4kHz)	IOL2-1	VOL=0.4V	0.45		mA
Output Low Current-2 (Room Temp.)	IOL-2	VOL=0.4V,Ta=25^{o}C	0.75		mA
Output High Current-1 (all output)	IOH-1	VOH=4.6V		-0.2	mA
Output High Current-2 (Room Temp.)	IOH-2	VOH=4.6V,Ta=25^{o}C		-0.35	mA
Supply Current (1)	IDD			1	mA
Supply Current (2)-1	ISSC-1	fo=32768Hz Cg=10pF		40	uA
Supply Current (2)-2	ISSC-2	fo=32768Hz Cg=10pF,Ta=25^{o}C		20	uA
Test Terminal Pull-up Resistance	Rpull		4	6	kohm
Clock Section Operating Minimum Voltage	Vc min	VDD-VSSC	1.8	-	V

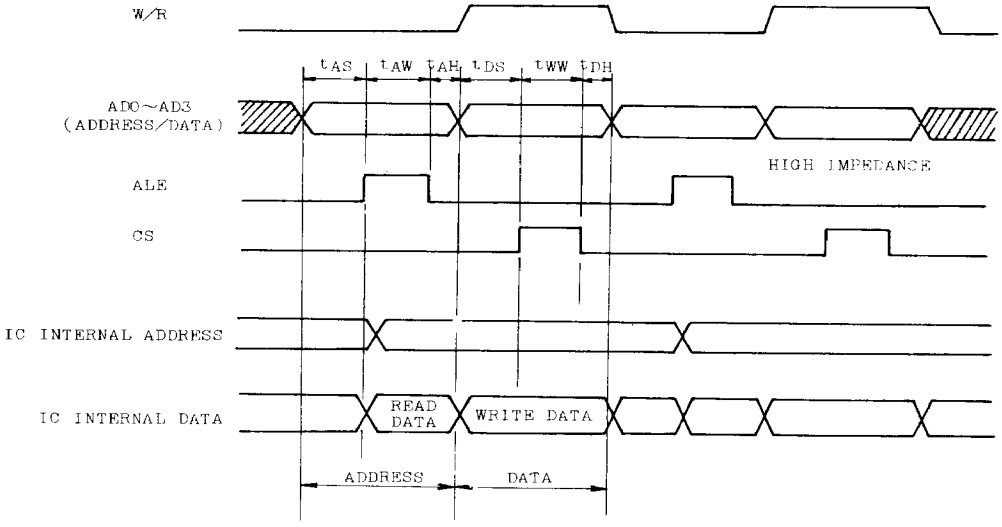
Note) The maximum IIH (Input High Current) is 1uA on the TC8250AP.

6.3 AC CHARACTERISTIC

(1) WRITE Mode

(VDD=5V±5%, VDD-VSSC=3V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	tAS		0	-	-	us
Address Write Pulse Width	tAW		0.4	-	-	us
Address Hold Time	tAH		0.1	-	-	us
Data Setup Time	tDS		0	-	-	us
Write Pulse Width	tWW		1	-	-	us
Data Hold Time	tDH		0	-	-	us

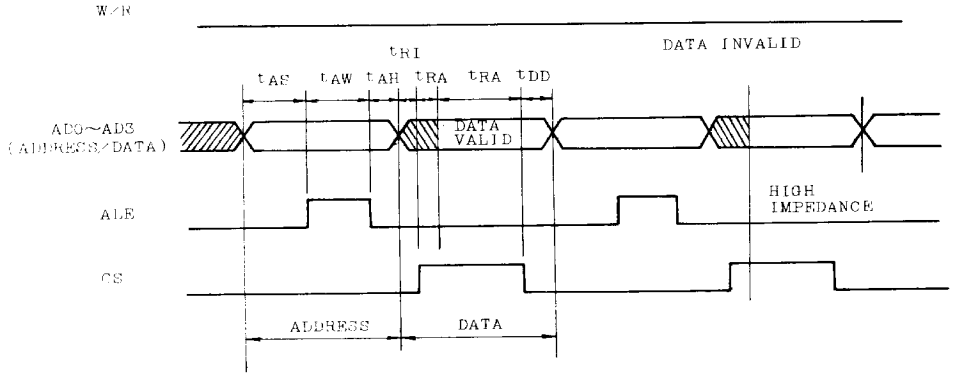


(2) READ Mode

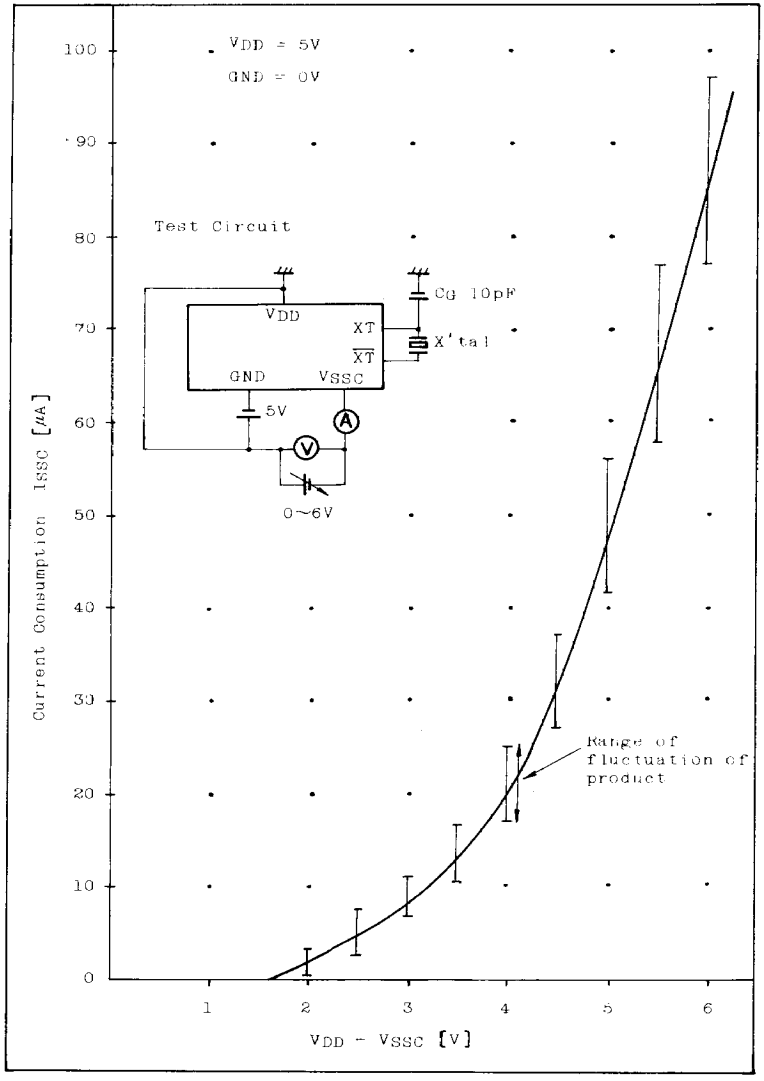
(VDD=5V±5%, VDD-VSSC=3V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	tAS		0	-	-	us
Address Write Pulse Width	tAW		0.4	-	-	us
Address Hold Time	tAH		0.1	-	-	us
Read Access Time	tRA		-	-	0.7	us
Read Delay Time	tDD		-	-	0.3	us
Read Inhibit Time	tRI		0.1	-	-	us

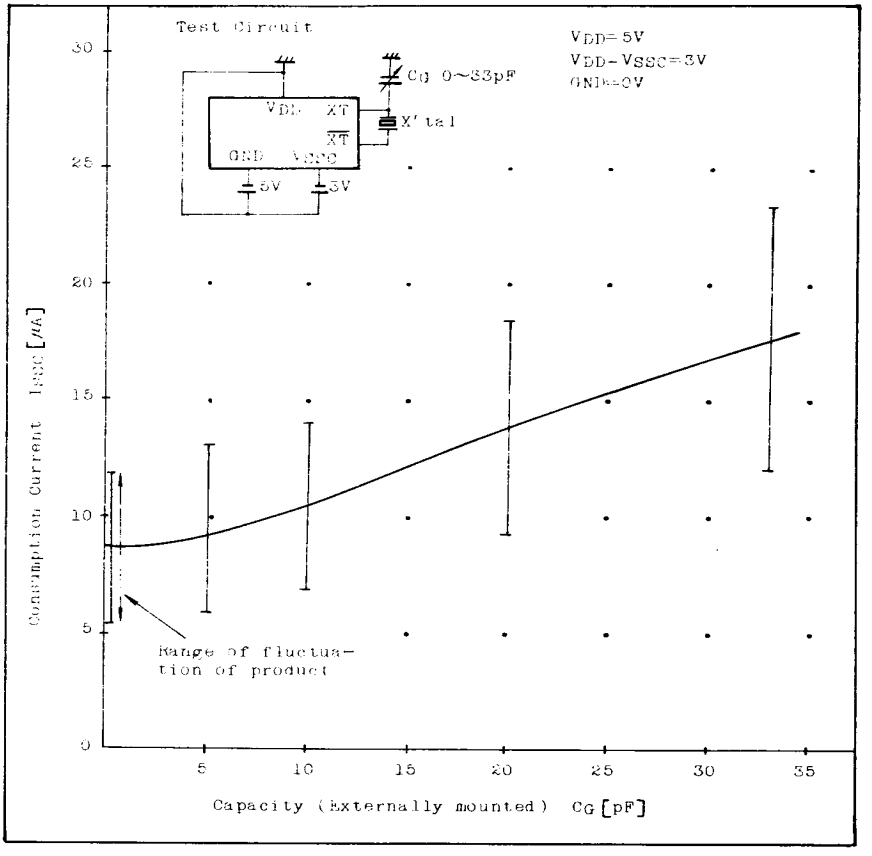
Note) ALE and READ input become active at level, not at edge.



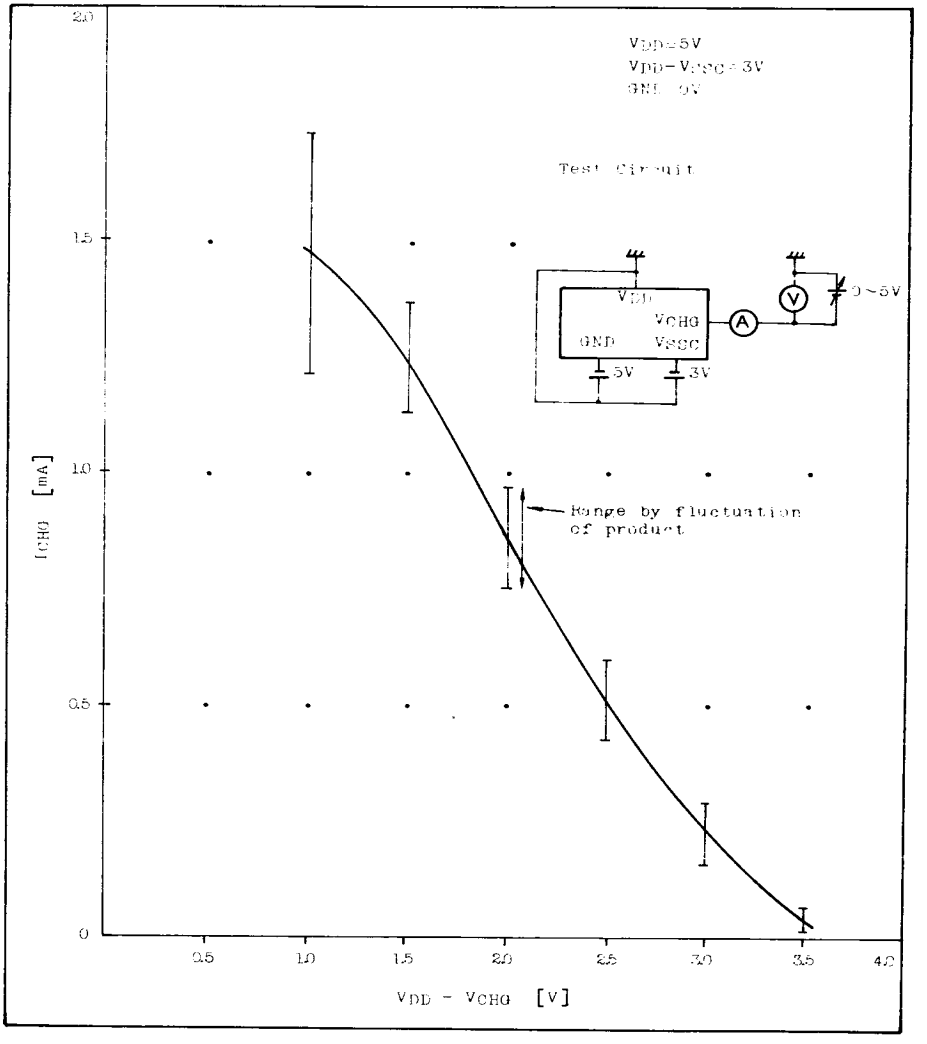
Relation between Current Consumption and VDD-VSSC



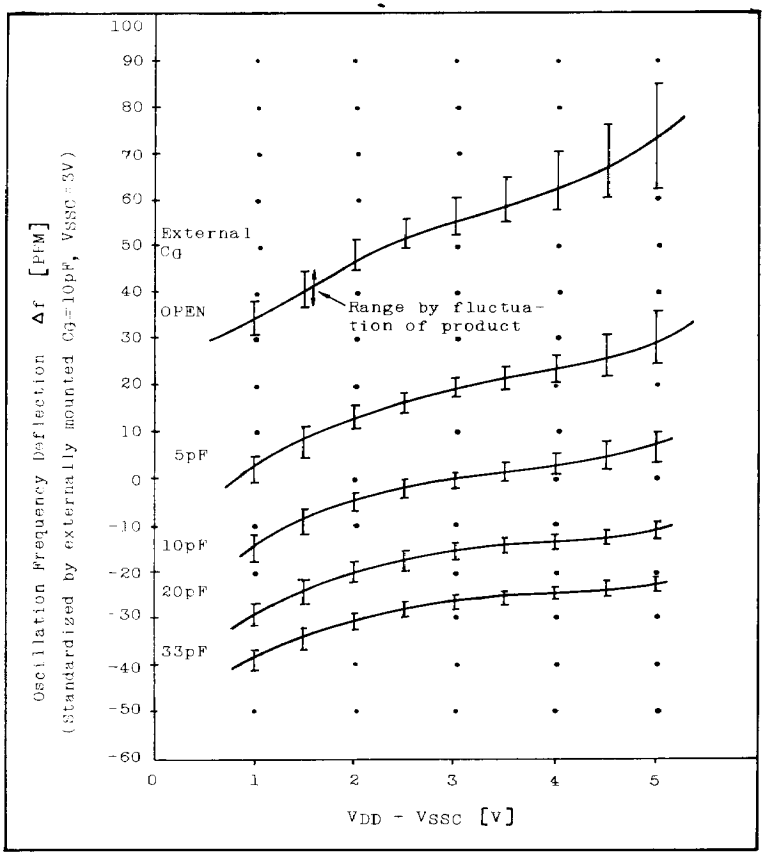
Relation between Current Consumption and External CG



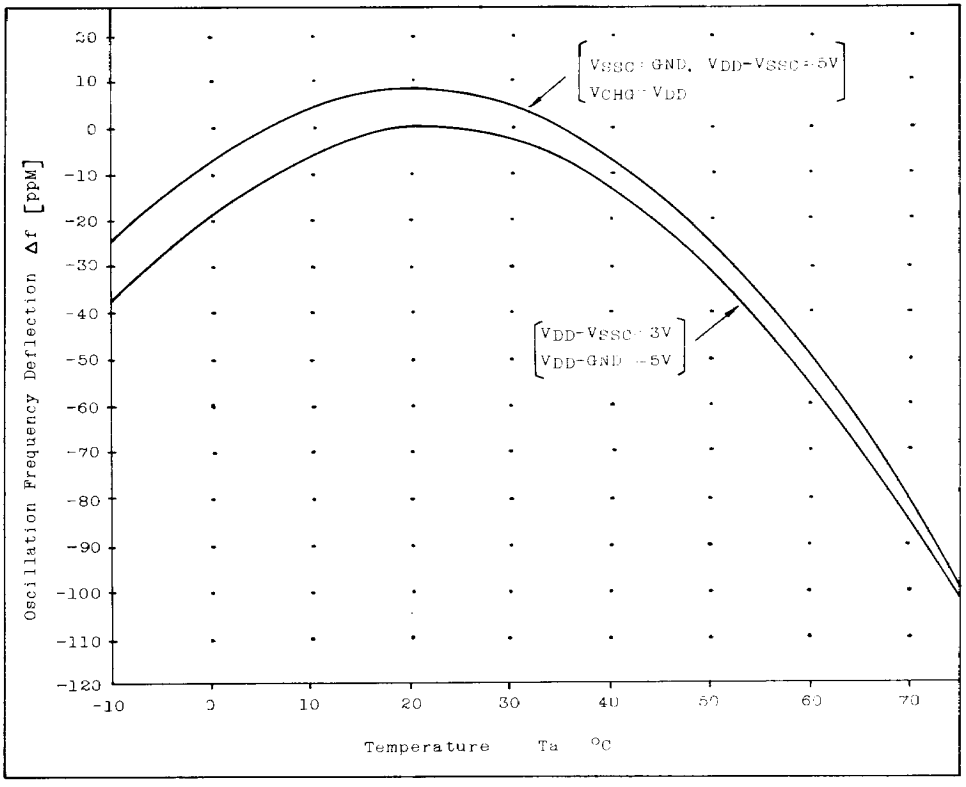
ICHG - VCHG CHARACTERISTIC



Supply Voltage Dependence of Oscillation Frequency

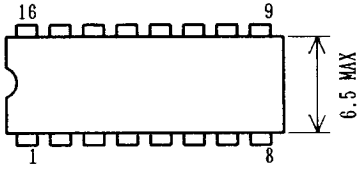


Temperature Characteristic of Oscillation Frequency
(Standardized by externally mounted CG=10pF, VDD-VSSC = 3V, 25°C)



7. PACKAGE OUTLINE

16PIN DIP(Plastic Package)



Unit in mm