[1] General

The C^2MOS voice synthesizing LSI systems T6721A, T6772 and T6684 are the easy-to-control voice synthesizing LOW POWER LSI systems with the following features.

T6721A C^2MOS Voice Synthesizing LSI

T6772 C^2MOS Mask ROM dedicated for Voice Data (64K bit)
T6684 C^2MOS Mask ROM dedicated for Voice Data (128K bit)

(1) The voce synthesizing system is of PARCOR type*. 8 kHz sampling voice output.

(2) C^2MOS +5V single power supply with low power consumption. (T6721A 2.5mW TYP., T6772 0.2mW TYP, T6684 0.3mW TYP.)

(3) Easy connection to a microcomputer. 12 kinds of command write, 4 kinds of synthesizing system status read, voice data ROM data read, and genration of BUSY signal and END OF SPEECH signal are possible.

(4) It is possible to make power down of the entire synthesizing system and to output signals for power down of the externally mounted audio circuit by means of commands from a microcomputer. The latter only is also possible.

(5) The manual use without a microcomputer connected is also possible. In this case, the sequential speech for every phrase (HALT/START) or ENDLESS LOOP speech is possible.

(6) Synthesizing conditions can be selected and speed of speech is changeable. (bit rate: 2.4, 4.8 and 9.6 kbps; sound source: 2; number of filter stages: 8 or 10; speed of speech: 10 stages)

(7) It is possible to store data other than voice data in the voice data ROM and use them by CPU.

(8) Max. capacity of voice data is 8M bit Max. at time of Mask ROM.

(9) The ceramic oscillator used for oscillation provides stable speech.

(10) The built-in voltage type DA converter (9 bits) improves accuracy of voice output.

* PARCOR is the voice analyzing and synthesizing method developed by Nippon Telegraph and Telephone Public Corporation, and our voice synthesizing LSIs have been developed under the guidance of Nippon Telegraph and Telephone Public Corporation.

[2] Configuration of Voice Synthesizing System LSI

When a voice synthesizing system is composed using the voice synthesizing LSI systems.

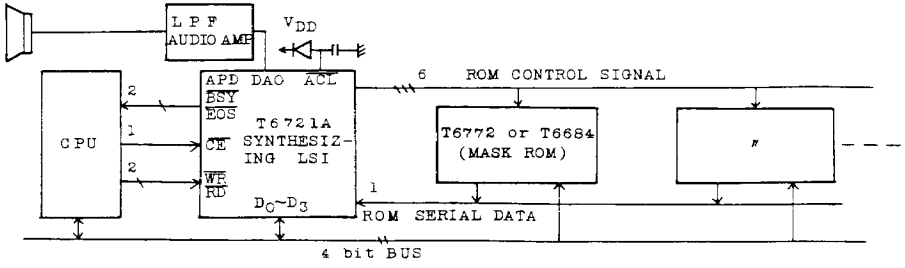
T6721A Voice Synthesizing LSI

T6772, T6684 Dedicated Mask ROM

there are tow types of configuration: CPU control type by means of a microcomputer and other CPU and manual control type using no CPU.

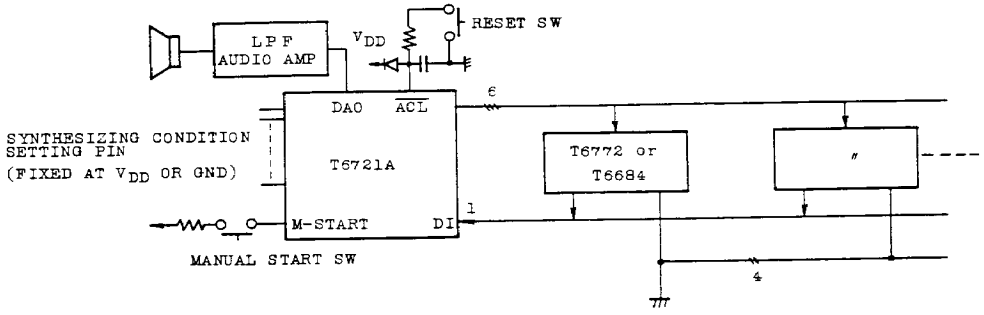
(1) CPU control type

The basic configuration of the system of this type is the 3 chip configuration composed of CPU, T6721A and (a) dedicated mask ROM (s). If ROM capacity is insufficient, multiple ROMs can be parallelly connected. (Refer to P29.)



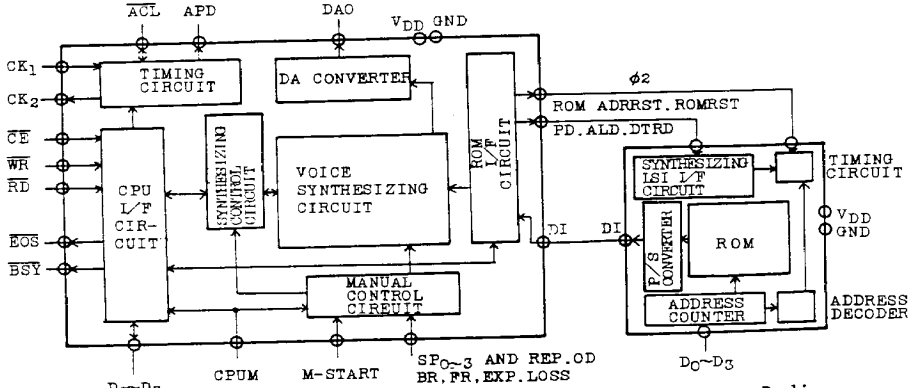
DAO : DA Converter Output APD : Audio Power Down

(2) Manual control type



As T6721A LSI has a built-in voltage type DA converter, it is necessary to externally provide LPF (low-pass filter) and AUDIO AMP as shown in the above diagram.

(3) Block diagram of each LSI



Synthesizing LSI T6721A

Voice Data Dedicated Mask ROM T6772, T6684

[3] Specifications for Voice Synthesizing Section

(1) Operation unit

Type	PARCOR type
No. of operation bits	15 bits
No. of digital filter stages	8 and 10 states are selectable
Clock frequency	160 kHz
Sampling frequency	8 kHz
Loss effect in digital filter	Available and non-available are selectable
Interpolating calculation	Available

(2) Others

Sound source	One of 2 voice sources is selectable. Unvoice source : white noise
Non-linear conversion	Available for 48 bits/frame
Total speech time	Systematically, possible to expand the voice ROM capacity up to 8 M bits. In the case of 2.4 kbps, the total speech time is about 1 hour.
Repeat bit	Available and non-available are selectable.

(3) Changeability of synthesizing conditions and speech length

Selection shown in the following table is possible for 6 synthesizing conditions. This selection, however, is made at time of voice analysis and selected conditions are set through the dedicated PINs when the manual control mode is used or by the CPU when the CPU is used.

Type of sound source	Loss effect	Bit/ frame	Frame length	Repeat	Number of filter stages
Pitch	None	48	20mS	Available	10
Triangle wave	Available	96	10mS	None	8

Selection of magnifications shown in the following table is possible for speech length assuming that length of original sound is x 1.0.

CODE (HEX)	1	2	3	4	5	6	7	8	9	A
(*)	x0.7	x0.8	x0.9	x1.0	x1.1	x1.2	x1.3	x1.4	x1.5	x1.55

(*): Magnification of speech length

This selection can be made by a command from CPU or through the decicated PIN when the manual control system is used. Differing from the above selection of synthesizing conditions, however, this selection is independent of the voice analysis.

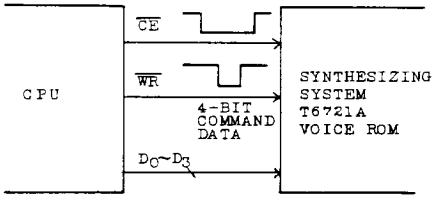
[4] Operation under CPU Control

Any control concerning synthesizing operation itself of the synthesizing system is not required for CPU. Controls required for CPU are (1) instruction for speech start and stop, (2) assignment of phrases to be spoken, and (3) others.

Flows of control signals and data between CPU and the voice synthesizing system may be classified into the follow 4 flows. Further, CPU M PIN of T6721A must be connected to V_{DD} when the CPU control.

(1) General

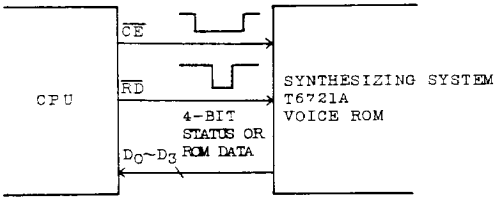
① Write operation from CPU to voice synthesizer system



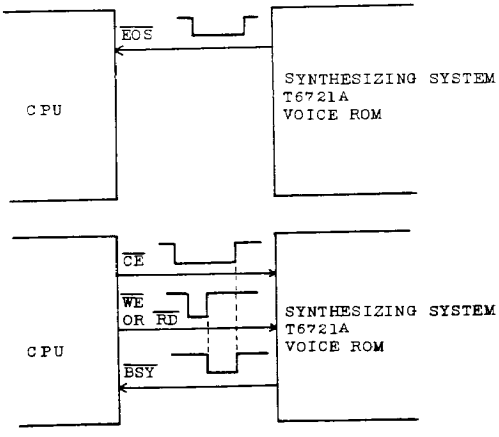
The synthesizing system is selected by $\overline{CE}$ and a 4 bit code on $D_0 \sim D_3$ is written by $\overline{WR}$. This 4 bit code coresponds to 12 types of commands which specify operation of the synthesizing system, and to parameter data for incidental synthesizing conditions and speech length or to the start address data specifying the phrases in the voice ROM.

② Read operation from voice synthesizing system to CPU

The synthesizing system is selected by $\overline{CE}$ and a 4 bit data is read on $D_0 \sim D_3$ from the synthesizing system by $\overline{RD}$. Content of this 4 bit data is 4 types of internal status of the synthesizing system or data in the voice ROM.



③ $\overline{EOS}$ (END OF SPEECH) and $\overline{BSY}$ (BUSY) signals from voice synthesizing system to CPU



$\overline{EOS}$ is the signal that is generated from the synthesizing system for about 20ms when the speech ended to inform CPU of the end of speech. $\overline{BSY}$ is generated for a period during which control by CPU is undesirable for the synthesizing system. That is, this is the period of data transfer in T6721A during power on Auto Clear or immediately after $\overline{WR}$ and $\overline{RD}$ are accepted.

However, no output is provided as long as $\overline{CE}$ is at "H" as output is resulted from AND with CE in T6721A. (Refer to Page 23)
$\overline{EOS}$ has no relation with $\overline{CE}$.

④ Generation of code data showing end of selected pharase from voice ROM to T6721A.
The synthesizing system stops speech by this END code (END ①) and generates the above-mentioned $\overline{EOS}$. When the synthesizing system is forced to stop speech by STOP command or power down command, $\overline{EOS}$ is not generated.
END ① code is added at time of voice analysis and ROM data preparation.

(2) Types of commands and operation of the synthesizing system

① SPDN (SYSTEM POWER DOWN)

- o Stops oscillation of T6721A and reduces power to the entire synthesizing system.
- o Places AUTIO POWER DOWN OUTPUT APD at "H" level.
- o Places $\overline{ACL}$ at "L" level and fixes the synthesizing system at the reset status. (Synthesizing conditions and speech length are also cleared, accordingly and reset is required when power is ON.)

② SAGN (SYSTEM ASGIN)

- o Releases SYSTEM POWER DOWN status.
- o After the release, there is the power on transient status for about average 30ms. $\overline{BSY}$ is generated during this trqnsient status.
- o APD is kept at "H" level. Therefore, prior to starting speech, it is necessary to make AAGN shown below.
- o It is necessary to take a time of more than 30ms before SAGN is made after SPDN.

③ APDN (AUDIO POWER DOWN)

o Places AUDIO POWER DOWN OUTPUT APD at "H" level.

④ AAGN (AUDIO ASGIN)

o Places APD at "L" level.

* APDN and AAGN are available during speech, so suited to the speaker ON/OFF key (SW) by use of the touch key provided to CPU.

⑤ SPLD (SPEED LOAD)

o Speed of speech (slow, fast) is set by this command and 1 nibble (4 bits) data that successively writes.

⑥ CNDT① (CONDITION ①)

o Type of sound source and availability of loss effect calculation are set by this command and succeeding 1 nibble data.

⑦ CNDT ② (CONDITION ②)

o Similar to CNDT ①, this command sets bit/frame, frame length, availability of repeat and number of filter states.

* Parameters that are set in ⑤, ⑥ and ⑦, above, are kept till they are reset or cleared by SPDN.

⑧ ADLD (ADDRESS LOAD)

o The start address of the voice data ROM corresponding to the phrase to be spoken or to the data in the voice data ROM to be read is set by this command and succeeding 5 nibbles (20 bits) data.

⑨ RRDM (ROM READ MODE)

o This is a command for setting a mode to read data in the voice data ROM. Under the normal mode other than this mode, the status is read by $\overline{RD}$.

o This mode is released when another command is written.

- The low order 4 bits of 8 bits of ROM data coresponding to the ROM address that have been set by ADLD in ⑧ are taken into T6721A by this command. These 4 bits are output to the bus lines $D_0 \sim D_3$ by next $\overline{RD}$ and at the same time, the high order 4 bits are taken into T6721A. Address is advanced in order by the succeeding read and data is read every 4 bits.
- This function makes it possible to take other data than voice analysis data into the voice data ROM and use it (particularly effective for phrase start address labelling that is described later).

⑩ STRT (START)

- This command starts the speech.
- Releases the status "ROM DATA ERROR".

⑪ STOP (STOP)

- This command forces the speech to stop and resets the synthesizing system.
- Synthesizing conditions, speech length and APD status are held by this command.

⑫ NOP (NO OPERATION)

- No OPERATION. ROM READ MODE is, however, released by this command.

⑬ Redundant Command

- 4 types of redundant codes are available. Although there is no effect even when these redundant codes are read, the status "COMMAND ERROR" becomes "H" level.

LIST OF COMMANDS, $\overline{RD}$

	Name, code D_3 D_2 D_1 D_0	$\overline{BSY}$ generating length (Tϕ =6.25μs TYP)	Cautions for generation			Operation	
1 Nibble Instruction	SPDN 1001	4 Tϕ MAX.		Invalid during POWER DOWN	Should not be performed when $\overline{BSY}$ is being generated ($\overline{BSY}$="L")	o Power down of the entire synthesizing system o Reset	Releases ROM READ MODE and changes the mode to STATUS READ MODE.
	SAGN 1011	"	APD remains at "H" level			o Release of power down	
	APDN 1010	"				o Brings APD to "H" level	
	AAGN 0100	"				o Brings APD to "L" level	
	RRDM 1000 Note 1	11 Tϕ MAX.	ROM start address must have been set	Should not be performed during the speech		o Sets ROM READ MODE	
	STRT 0001 Note 1	4 Tϕ MAX.	ROM start address must have been set. Synthesizing conditions must have been set.			o Starts the speech o If the succeeding ROM data is not at "H" level for 1 frame, status ROM DATA Err is released.	Release ROM READ MODE and changes the mode to STATUS READ MODE.
	STOP 0010	"				o Speech stop and reset (synthesizing conditions and APD are held)	
	NOP 0000	"				o NO OPERATION	
	REDUNDANT COMMAND 11xx	"				o Status COMMAND Err becomes 1.	

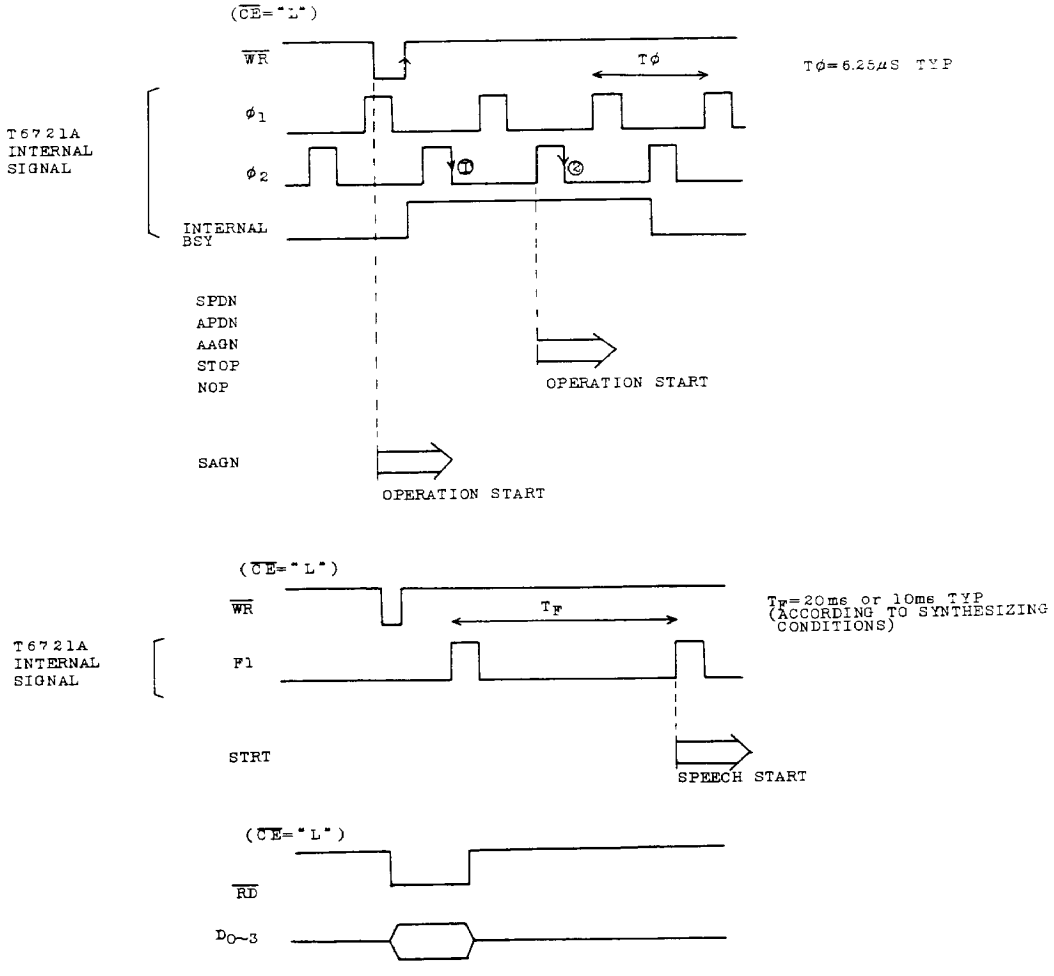
*: ($\overline{BSY}$="L")

	Name, code D_3 D_2 D_1 D_0	$\overline{BSY}$ generating length (Tϕ =6.25μs TYP)	Cautions for generating				Operation	
2 Nibble Instruction	SPLD 0101 XXXX	4 Tϕ MAX. "		Should not be performed during the speech (status EOS = 0).	Invalid during POWER DOWN	Should not be performed when $\overline{BSY}$ is being generated*	o Sets speech length (speed)	Release ROM READ MODE and change the mode to STATUS READ MODE.
	CNDT① 0110 XX00	" "	D_0,D_1 must be "0".				o Sets synthesizing conditions ①	
	CNDT② 0111 XXXX	" "					o Sets synthesizing conditions ②	
6 Nibble Instruction	A D L D 0 0 1 1 $X_1X_1X_1X_1$ $X_2X_2X_2X_2$ $X_3X_3X_3X_3$ $X_4X_4X_4X_4$ $X_5X_5X_5X_5$	" " " " " "	Data of all 20 bits must be set.				o Sets ROM start address 20 bits.	

	$\overline{BSY}$ generating length (Tϕ = 6.25μs TYP)	Cautions for generating	Operations other than principal operations
$\overline{RD}$	Status read 4 Tϕ MAX. ROM Data read 11 Tϕ MAX.	Should not be performed when $\overline{BSY}$ is being generated. Note 1.	o Status or ROM data read. o Release of 2 nibble and 6 nibble modes.

Note 1. 120μs TYP. is required for a period from setting of ROM address by 6 nibble instruction to RRDM or STRT command write. Similarly, 120μs TYP. is also required for a period from RRDM to $\overline{RD}$ and succeeding each $\overline{RD}$.

The timing that the operation of each command starts after each WR is in some point of time in a period from the edge of $\overline{WR}$ to end of BSY. The timing chart is shown below.



(3) Setting of parameters for synthesizing conditions and speech length

Parameters for synthesizing conditions will be determined separately upon consultation with customers at the initial stage of the development on the basis of their requirements for speech quality, ROM capacity, etc. These parameters are set by the above-mentioned commands CNDT ①, CNDT ② and SPLD and the succeeding 1 nibble data on the bus lines $D_0 \sim D_3$. These parameters must have been properly set prior to the speech and also, must not be reset during the speech.

Synthesizing Conditions and Bus Line Data

Bus Line Data \ Condition / Command		Synthesizing conditions ①	Synthesizing conditions ②
		CNDT ①	CNDT ②
D_3	0	Sound source shape pitch	48 bits/frame
	1	Sound source shape triangle wave	96 bits/frame
D_2	0	Loss effect calculation None	20 ms/frame
	1	" Available	10 ms/frame
D_1	0	Must be set at 0	Repeat available
	1		Repeat None
D_0	0	Must be set at 0	Filter 10 stages
	1		Filter 8 stages

Magnification of Speech Length and Bus Line Data

Bus line data	1	2	3	4	5	6	7	8	9	A
Magnification of speech length	x0.7	x0.8	x0.9	x1.0	x1.1	x1.2	x1.3	x1.4	x1.5	x1.55

When the redundant codes 0,B,C,D,E and F are set, the magnification becomes x1.0.

Voice synthesizing bit rate is selected through the combinaiton of D_3 and D_2 of the synthesizing conditions ② in the above table.

2.4 kbps 48 bits/frame and 20 ms/frame
4.8 kbps 48 bits/frame and 10 ms/frame
9.6 kbps 96 bits/frame and 10 ms/frame

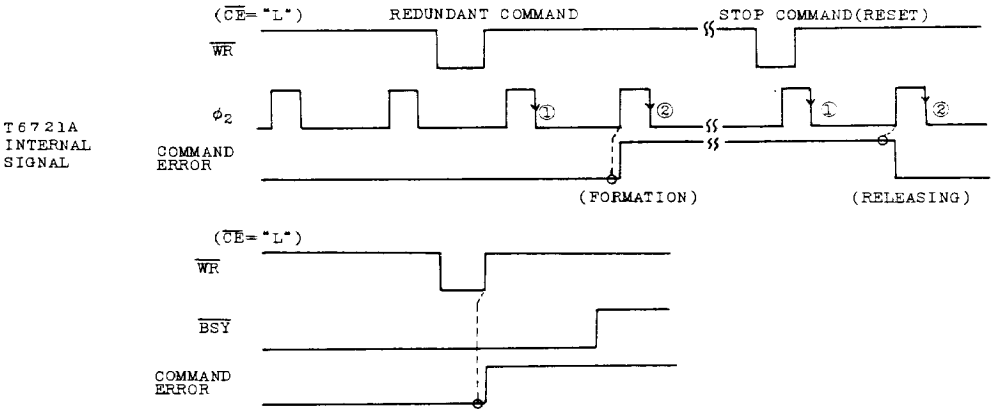
(4) Synthesizing system status output (status)

Unless the system has been placed in ROM READ MODE by Coomand RRDM, when the read is performed from CPU, a 4 bit status is read out and the status of the synthesizing system can be known. To release this mode, execute commands (NOP, etc.) other than RRDM. Names of status and corresponding bus lines, and conditions for formation and releasing are shown in the following table.

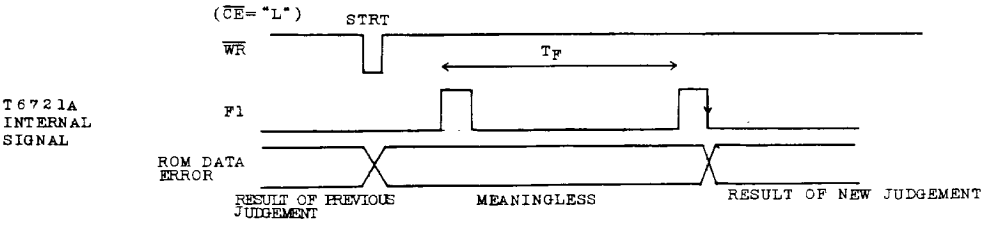
Corresponding bus line	Status name	Conditions for formation ("H")	Conditions for releasing
D_3	COMMAND ERROR	(1) When a redundant command is written. (2) When write/read is made during BSY is being generated.	STOP When POWER ON CLEAR. During POWER DOWN
D_2	ROM DATA ERROR	When the speech has started and all voice data in the first frame are at "H" level. That is,when ROM CHIP that did not exist has been selected or when it has started from address in which any data did not exist.	Same as above, and when normal data has been obtained by next start.
D_1	POWER DOWN	When the synthesizing system is in POWER DOWN status.	At time of POWER ON.
D_0	EOS (END OF SPEECH)	When no voice is synthesized.	During voice is being synthesized.

The timing chart for formation and releasing of each status is shown below.

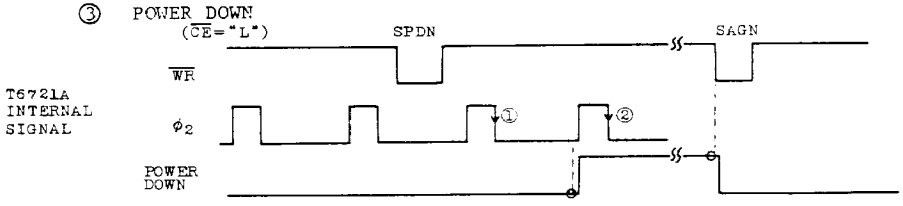
① COMMAND ERROR



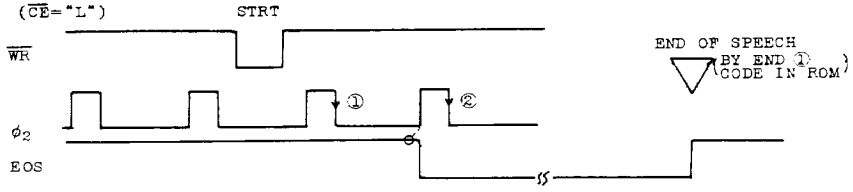
② ROM DATA ERROR



③ POWER DOWN

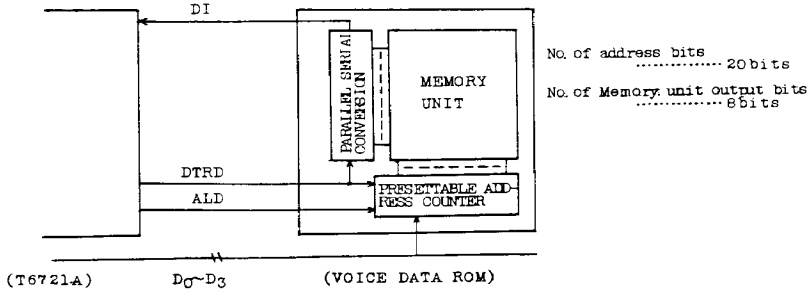


④ EOS (END OF SPEECH)



(5) Setting of ROM start address

① Voice data ROM structure and ROM data output



The structure of Voice Data ROM and principal interface signals with T6721A are shown above.

The voice data output operation is executed as shown below:

(i) Selection of phrase to be spoken

ROM start address 20 bits for the phrase are set from CPU by ADLD command and succeeding 5 nibble (20 bits) data to be output to the bus lines. At this time, load pulse ALD is once generated from T6721A to the presettable address counter every 1 nibble.

(ii) Start of speech

When STRT command is written from CPU, the address counter starts to count from the start address, and counted data are converted to serial data DI through the parallel serial conversion and transfered to T6721A. The transfer timing of this parallel serial conversion and this address count are controlled by DTRD pulse.

At this time, a waiting time of TYP 120 μs is required for the systematic reason from completion of address setting in (i) to STRT command write.

(iii) Stop of speech

Unless the speech is forced to stop by STOP command, SPDN command, etc., the count in (ii) is continued until END ① code comes appear in voice data.

② Definite setting method of ROM start address

The setting sequence of the above ① - (i) is as follows.

CPU Operation	Data from CPU to bus line D_3 D_2 D_1 D_0	(MSB) A_{19}	A_{15}	A_{11}	A_7	A_3 (LSB) A_0	
Command	ADLD 0 0 1 1	Y_{19} Y_{18} Y_{17} Y_{16}	Y_{15} Y_{14} Y_{13} Y_{12}	Y_{11} Y_{10} Y_9 Y_8	Y_7 Y_6 Y_5 Y_4	Y_3 Y_2 Y_1 Y_0	(Old address)
1st data	X_3 X_2 X_1 X_0	* * * *	* * * *	* * * *	* * * *	X_3 X_2 X_1 X_0	
2nd data	X_7 X_6 X_5 X_4	* * * *	* * * *	* * * *	X_7 X_6 X_5 X_4	X_3 X_2 X_1 X_0	
3rd data	X_{11} X_{10} X_9 X_8	* * * *	* * * *	X_{11} X_{10} X_9 X_8	X_7 X_6 X_5 X_4	X_3 X_2 X_1 X_0	
4th data	X_{15} X_{14} X_{13} X_{12}	* * * *	X_{15} X_{14} X_{13} X_{12}	X_{11} X_{10} X_9 X_8	X_7 X_6 X_5 X_4	X_3 X_2 X_1 X_0	
5th data	X_{19} X_{18} X_{17} X_{16}	X_{19} X_{18} X_{17} X_{16}	X_{15} X_{14} X_{13} X_{12}	X_{11} X_{10} X_9 X_8	X_7 X_6 X_5 X_4	X_3 X_2 X_1 X_0	

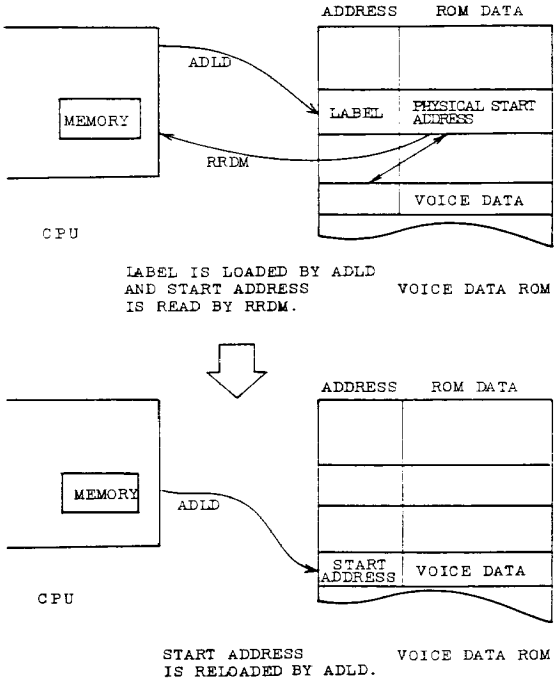
* denotes indefinite values.

* Use of Labeled Start Address

When the above start address $X_0 \sim X_{19}$ is generated each time a phrase is assigned by CPU, load applied on CPU software will increase in proportion to increase in kinds of phrases. In addition, if it becomes necessary to change contents of phrases, not only the voice data ROM but also CPU side software must be changed.

Therefore, when serial numbers (labels) are assigned to phrases and labels are generated at CPU software side without generating physical addresses of these phrases, load at CPU side can be reduced.

For this purpose it is possible to use a method in which physical address of each phrase is stored in a part of the voice data ROM address space, that ROM address is used as a lable, which is then address loaded (ADLD) by CPU, and physical start address is read by RRDM and reloaded to select a phrase.

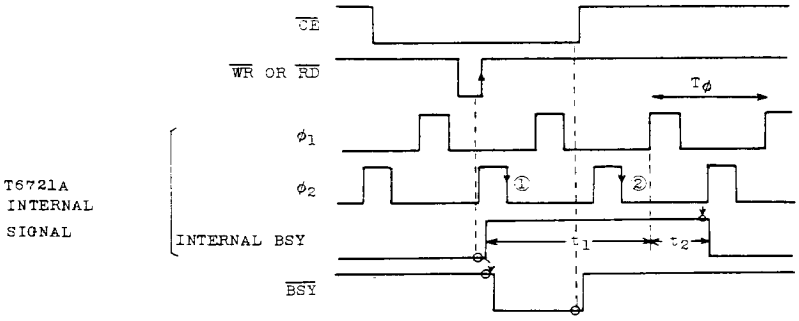


(6) $\overline{BSY}$ Output

The period in which $\overline{BSY}$ signal is generated from T6721A is that period during which $\overline{WR}$ and $\overline{RD}$ from CPU must not be accepted by the synthesizing system. If $\overline{WR}$ or $\overline{RD}$ is performed disregarding this period, the synthesizing system does not accept $\overline{WR}$ or $\overline{RD}$ at all or operates uncertainly and the internal status may possibly becomes uncertain. In this case, however, status COMMAND ERROR is formed to give a warming.

When $\overline{BSY}$ signal is generated, length of the period of $\overline{BSY}$ signal generation is either ① or ②, below.

① Period from rise of $\overline{WR}$ or $\overline{RD}$ pulse from CPU to completion of command data transfer process in the synthesizing system.



* $\overline{BSY} = \overline{CE \cdot \text{internal BSY}}$
* TØ = 6.25us TYP.
* When rise of $\overline{WR}$ or $\overline{RD}$ and ① of ϕ_2 fall in the diagram are close together, $t_1 + t_2$ may be further lengthened 1 Tφ length in some cases due to delay of signal transmission in LSI.

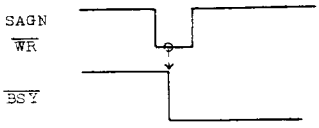
	Internal BSY generating period ($t_1 + t_2$)	Synthesizing system operation by $\overline{WR}$ or $\overline{RD}$ during internal BSY generating period	
		$\overline{WR}$ or $\overline{RD}$ in t_1 term	$\overline{WR}$ or $\overline{RD}$ in t_2 term
Command RRDM and succeeding $\overline{RD}$	From rise of $\overline{WR}$ to rise of next $\Phi 2$ after 9 falls of $\Phi 2$ are counted. 11 TΦ Max. including characteristic consideration.	$\overline{WR}$ or $\overline{RD}$ is inhibited and COMMAND ERROR of the status is formed.	$\overline{WR}$ or $\overline{RD}$ is accepted uncertainly, and uncertain operation and status are resulted. Length of internal BSY signal may be extended in some cases. COMMAND ERROR is formed.
$\overline{WR}$ or $\overline{RD}$ other than above (excluding command STOP)	From rise of $\overline{WR}$ to rise of next $\Phi 2$ after 2 falls of $\Phi 2$ are counted. 4 TΦ Max. including characteristic consideration.		
Command $\overline{WR}$ or $\overline{RD}$ during BSY by command STOP.	——	Ditto. However, previously written STOP command (RESET) may be executed and ERROR released immediately in some cases.	
$\overline{WR}$ or $\overline{RD}$ of command STOP	4 TΦ Max. including characteristic consideration.	WR or RD is inhibited and COMMAND ERROR is formed	Ditto. However, COMMAND ERROR may be released in some cases.

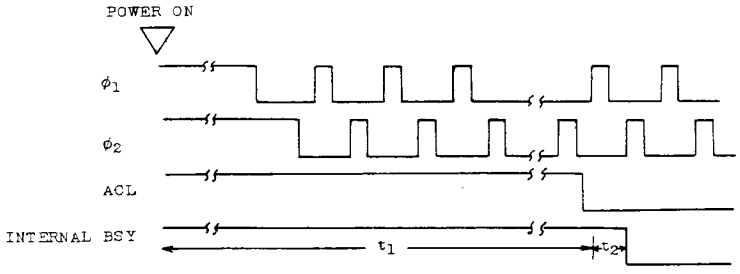
Therefore, it is necessary for CPU to perform write or read after checking $\overline{BSY}$ signal or to take a sufficient interval between each write or read.

② Power ON transient status period

When the synthesizing system is placed in On status by turning the power switch ON or by SAGN command, AUTO CLEAR (ACL) is generated for a fixed time (about 30 ms) by the capacitor which has been externally mounted on T6721A $\overline{ACL}$ terminal and the synthesizing system is initialized. This period is power ON transient status and $\overline{BSY}$ will generate during its length.

When the power on is made by SAGN command, differing from the normal case, fall of $\overline{BSY}$ signal begins to generate during $\overline{WR}$ is at low level, not from rise of $\overline{WR}$.

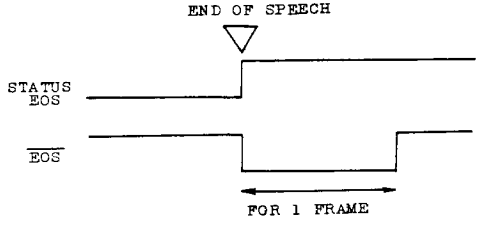




(7) $\overline{EOS}$ Output

AT the end of speech, the speech is stopped by END ① code that has been set at the end of a phrase in the voice data ROM and the $\overline{EOS}$ output is placed at low level for about 1 frame (20 or 10ms TYP). When the speech is forced to stop by STOP or SPDN command, no $\overline{EOS}$ output is generated. Further, if the speech is restarted when $\overline{EOS}$ is at LOW level, the $\overline{EOS}$ output is placed at high level.

The relationship with status EOS is shown below.



(8) Summary of principal precautions under CPU control

① Connect T6721A CPUM PIN to "H". (Page 8.)

② $\overline{BSY}$ output is the output from AND of T6721A internal BSY signal and CE. Therefore, when $\overline{CE}$ is at "H" level, there is no $\overline{BSY}$ output. (Page 23.)

③ In [4]-(2) "Types of commands and operation of synthesizing system" (Pages 10 to 15), the following instructions should be particularly observed:

(i) $\overline{WR}$ or $\overline{RD}$ must not be performed when internal BSY signal is being generated. (Pages 13, 14, 22, 23 and 24.)

(ii) APD output is placed at "H" level by command SPDN and is also placed at "H" by next command SAGN. It should be made ot "L" level by AAGN command. (Page 10, 11.)

(iii) In RD operation, the status is normally read out. (Pages 11 and 17.) To read ROM data, it is necessary to set mode by command RRDM.

(iv) It is necessary to take 120 μs TYP for a period from ROM data start address setting to next RRDM or START command write. In the similar manner, 120 μs TYP is also required from read after RRDM to RRDM and each interval of subsequent reads. (Pages 13, 14 and 20.)

(v) RRDM, STRT, 2 nibble and 6 nibble commands must not be executed during the speech. (Pages 13, 14.)

(vi) It is necessary to take a time more than 30 ms before command SAGN is executed after SPDN command. (Page 10.)

(vii) Time required for each command to start to operate after write. (Page 15.)

④ Timing for formation and release of each status. (Pages 17 to 19.)

[5] Operation under Manual Control

The operation under manual control is performed by M·START PIN, the switch externally mounted on $\overline{ACL}$ PIN and control code END ① and END ② generated from the voice data ROM of T6721. Connect CPUM PIN of T6721A to "L".

(1) General

① Reset of synthesizing system	$\overline{ACL}$ SW ON
② Speech start	M·START SW ON
③ Stop by end of speech	END ① Code
④ Repeat of a series of speeches	END ② Code
⑤ Set of synthesizing conditions and speech length	Set of T6721 dedicated PIN level

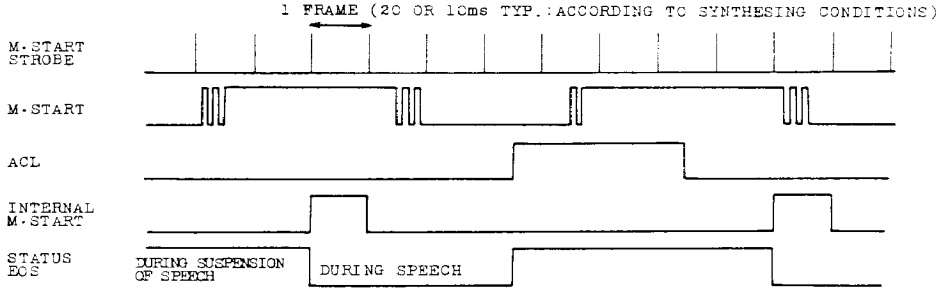
(2) Reset operation

- After $\overline{ACL}$ switch is turned from ON to OFF, AUTO CLEAR (ACL) is generated for a fixed time (about 30ms) by the capacitor externally mounted on PIN, and the synthesizing system is initialized. During this period, the M·START switch is not accepted. This reset operation is used when the speech is forced to stop or the system is initialized.
- When the power switch (Pages 41~40) in the configuration circuit is turned from the OFF position to the ON position, ACL is generated as in the above case. If the power ON status is once turned to the OFF status and then, to the ON status again, a time of more than 100ms is required for turning OFF the power supply.

(3) Start operation

The start operation is initiated by the M·START switch.

When M·START switch is normally depressed, T6721A will start the speech after the chattering preventive time (about 20ms) has passed.



M·START switch must have been steadily depressed for more than 2 frame length.

Chattering of M·START switch must be less than 20ms at both ON and OFF sides.

(4) Setting of parameters for synthesizing conditions and speech length

These parameters are set by connecting the T6721A synthesizing condition setting pins (6 pins) for the manual control to "H" or "L". These synthesizing conditions have been already selected at time of the analysis.

Pin / Level	EXP	LOSS	BR	FR
L	Sound source shape pitch	Loss effect calculation - None	48 bits/frame	20ms/frame
H	" triangle wave	" Available	96 bits/frame	10ms/frame

Pin / Level	REP	OD
L	Repeat - Available	Filter - 10 stages
H	Repeat - None	Filter - 8 stages

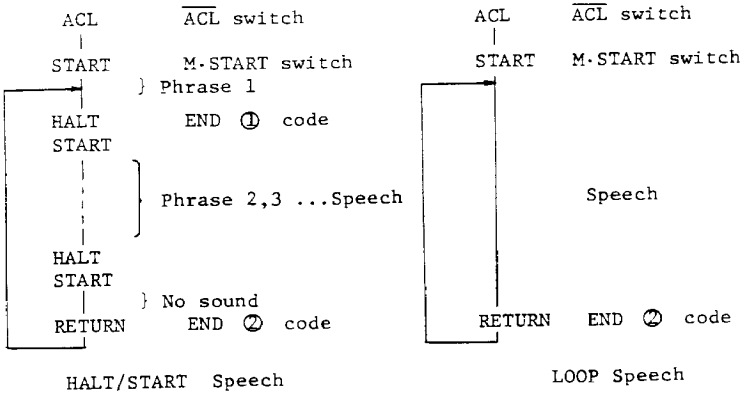
Set the T6721A speech length setting pins($SP_3 \sim SP_0$) for the manual control to the codes shown in the following table.

SP_3, SP_2, SP_1 and SP_0 Code	1	2	3	4	5	6	7	8	9	A
Magnification of speech length	x0.7	x0.8	x0.9	x1.0	x1.1	x1.2	x1.3	x1.4	x1.5	x1.55

When 0, B, C, D, E and F are set, the magnification becomes x1.0.

(5) HALT/START and ENDLESS LOOP speech

2 types of speeches are possible by the stop code END ① and the ROM address initialize code END ② arranged in the voice data ROM. Select either one of these codes.



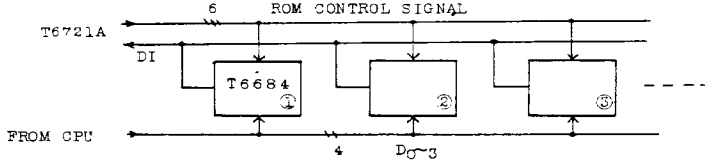
[6] Dedicated Mask ROM

(1) Use of multiple dedicated mask ROMs

On T6684 128K ROM, the speechable times without using repeat bits are as follows:

2.4 kbps	53 sec.
4.8 kbps	26 sec.
9.6 kbps	13 sec.

If time is insufficient, multiple mask ROMs can be used when they are parallelly connected. The connection in this case is as shown below:



All address counters that have been built in ROMs always perform the same count and each ROM selects itself by its built-in chip selecter according to address. Therefore, the individual chip select signal to each ROM from CPU or T6721A is not required as shown in the figure. In this case, current consumption of unselected ROM is TYP. 20μA/ROM. (Refer to electrical characteristics.)

Max. Connectable ROMs

				Total speech time (sec.)		
		No.of connectable ROMs	Total No. of bits	2.4 kbps	4.8 kbps	9.6 kbps
T6772	64 kbits	8	512K	210	105	50
T6684	128 kbits	16	2M	850	425	210

[7] PIN DESCRIPTION & PIN CONNECTIONS

(1) PIN Description

(1)-1 T6721A(Voice synthesizing LSI)

PIN Name	PIN NO. FP ( ):DIP	Structure I/O	Structure Pull-up/down	Functional Explanation
W	1 (5)	Output	-	Output for test.
TDAI	3 (6)	Input	Pull-down	Input for test. To be connected to GND.
TFIO	4 (7)	Output	-	Output for test.
DAO	6 (8)	DAC Output	-	DA CONVERTER Output. Output of V_{SS} during power down.
APD	7 (9)	Output	-	Power down output for external audio circuit.
ϕ_2	8 (10)			Clock pulse to ROM or P-ROM I/F LSI.
PD	9 (11)			Power down to ROM or P-ROM I/F LSI.
ROM ADR RST	11 (12)			Address reset to ROM or P-ROM I/F LSI.
ROM RST	12 (13)			Initialize to ROM or P-ROM I/F LSI.
ALD	13 (14)			Sart address set pulse to ROM or P-ROM I/F LSI.
DI	14 (15)	Input	500kΩ Pull-up	Data input from ROM or P-ROM I/F LSI.
DTRD	15 (16)	Output	-	Data read pulse to ROM or P-ROM I/F LSI.
D3	18 (17)	3-state bi-directional bus	-	4-bit bus line Input during $\overline{WR}$ is "L". Output during $\overline{RD}$ is "L". Hi-Z at other occasions
D2	19 (18)			
D1	21 (19)			
D0	22 (20)			

PIN Name	PIN NO. FP ( ):DIP	Structure I/O	Structure Pull-up/down	Functional Explanation
GND	23 (21)	Power supply	—	0V
VDD	24 51 (42)			+5V
$\overline{WR}$	25 (22)	Input	500kΩ Pull-up	Write pulse input of command, data, etc. under CPU control.
$\overline{RD}$	26 (23)			Read pulse input of status, ROM data, etc. under CPU control.
$\overline{CE}$	27 (24)			Chip enable pulse input under CPU control.
$\overline{BSY}$	28 (25)	Output	-	BSY Output
$\overline{EOS}$	29 (26)			Output at end of speech
CPUM	31 (27)	Input	None	Fixed to high level under CPU control. Fixed to low level under CPU control.
$\overline{ACL}$	32 (28)	I/O	-	Power ON auto clear pin. Schmitt input
TPN	33 (29)	Input	Pull-down	Input for test. To be connected to GND.
M·START	35 (30)		10mΩ ∿ 50mΩ Pull-down	Start switch under manual control.
CK1	36 (31)		None	Connection pin for ceramic oscillator (Murata Ceralock)
CK2	38 (32)	Output	-	Connection pin for ceramic oscillator (Murata Ceralock)
EXP	39 (33)	Input	None	Connected to high or low level under of manual control according to fixed synthesizing conditions.

PIN Name	PIN NO. FP ( ):DIP	Structure I/O	Structure Pull-up/down	Functional Explanation
REP	40 (34)	Input	None	Connected to high or low level under of manual control according to fixed synthesizing conditions.
OD	41 (35)			
BR	43 (36)			
FR	44 (37)			
TEM	45 (38)			Input for test. To be connected to GND.
SP0	46 (39)			Speech length can be set up by connecting this input pin to high or low level under manual control.
SP1	47 (40)			
SP2	49 (41)			
SP3	52 (1)			
LOSS	53 (2)			Same as EXP ∿ FR.
TS	54 (3)		Pull-down	Input for test. To be connected to GND
TSN	56 (4)			

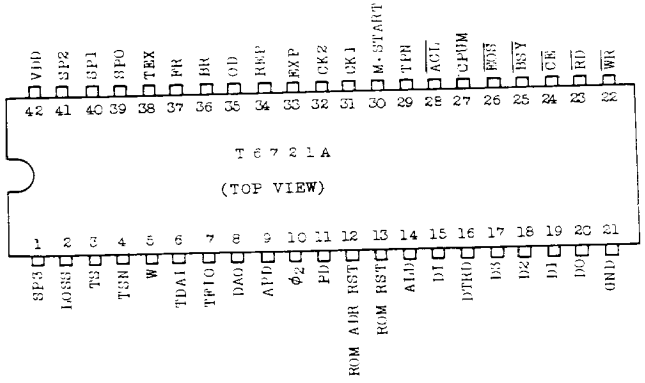
(1)-2 T6772, T6684 (Mask ROM)

PIN Name	PIN NO. FP ( ):DIP	Structure		Functional Explanation
		I/O	Pull-up/down	
D0	1 (17)	Input	None	4-bit bus line Address data input at setting of start address.
D1	2 (18)			
D2	4 (19)			
D3	5 (20)			
DTRD	6 (21)			Data read pulse from synthesizing LSI.
DI	7 (22)	3-state output	-	Serial data output to synthesizing LSI. Hz during nonselection and power down.
ALD	8 (23)	Input	None	Start address set pulse from synthesizing LSI.
ROM RST	9 (24)			Initialize from synthesizing LSI.
ROM ADR RST	11 (25)			Address reset from synthesizing LSI.
PD	13 (26)			Power down from synthesizing LSI.
ϕ_2	14 (27)			Clock pulse from synthesizing LSI.
V_{DD}	18 39 (28)	Power supply	-	+5V
GND	42 (15)			0V
TS	43 (16)	Input	500kΩ Pull-down	Input for test.
TSO	29 (17)	Output	-	Output for test. (N.C. for T6772)

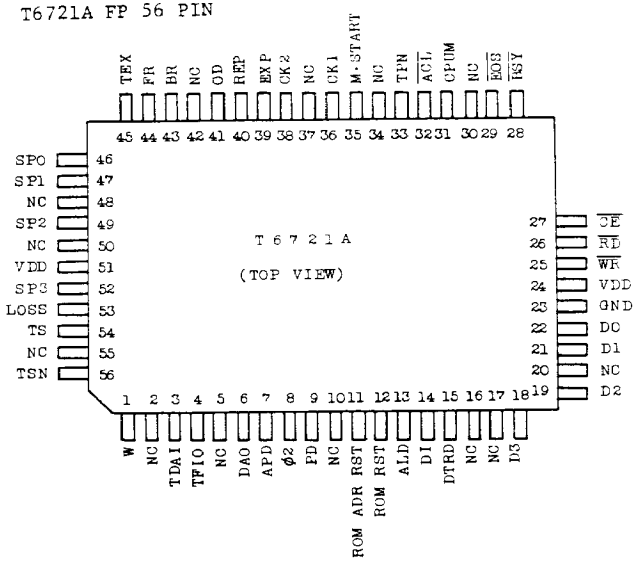
* T6684

(2) PIN CONNECTIONS

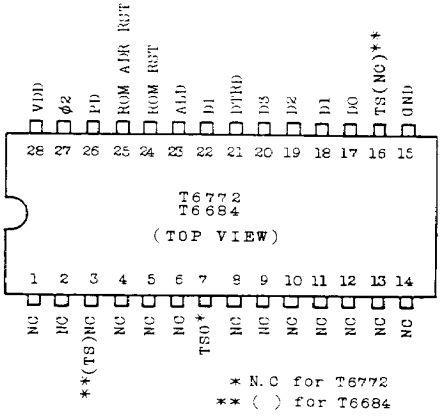
(2)-1. T6721A DIP 42PIN



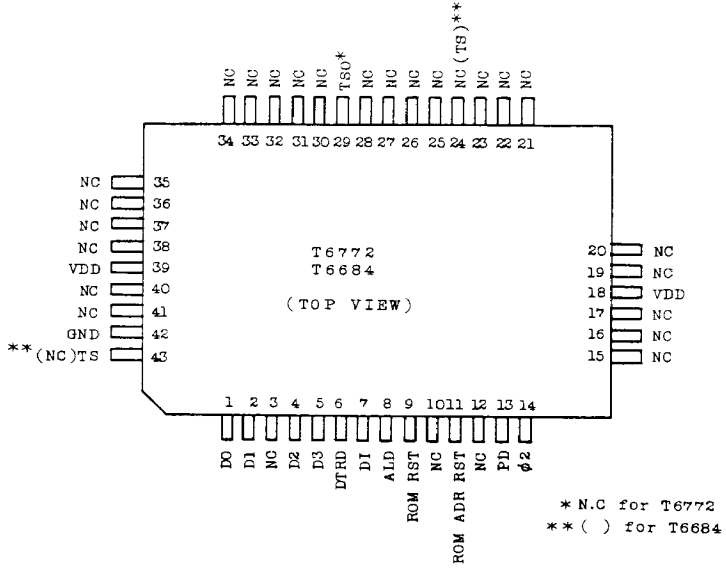
T6721A FP 56 PIN



(2)-2. T6772, T6684 DIP 28 PIN



T6772, T6684 FP 43 PIN



[8] System CONFIGURATION DIAGRAM

(1) LSI Connections

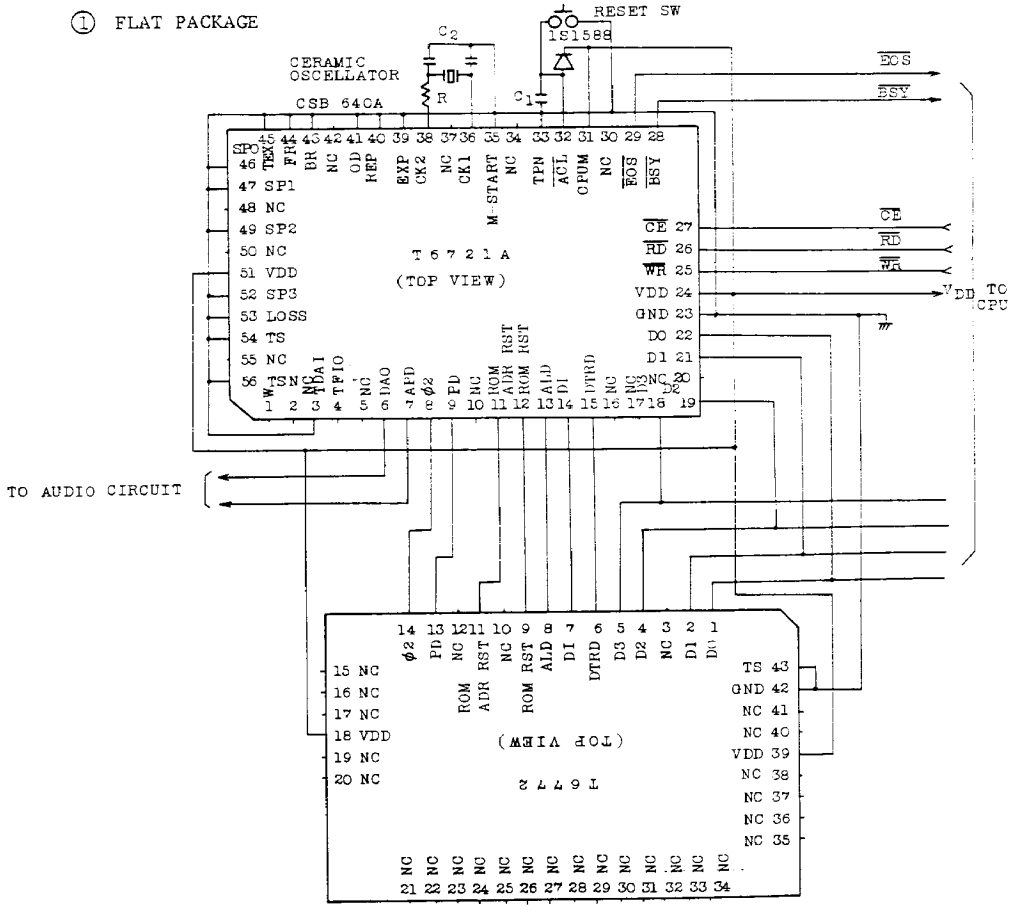
(1)-1. CPU Control Type

R = 5.1 KΩ

C_1 = 1 μF

C_2 = 100 PF

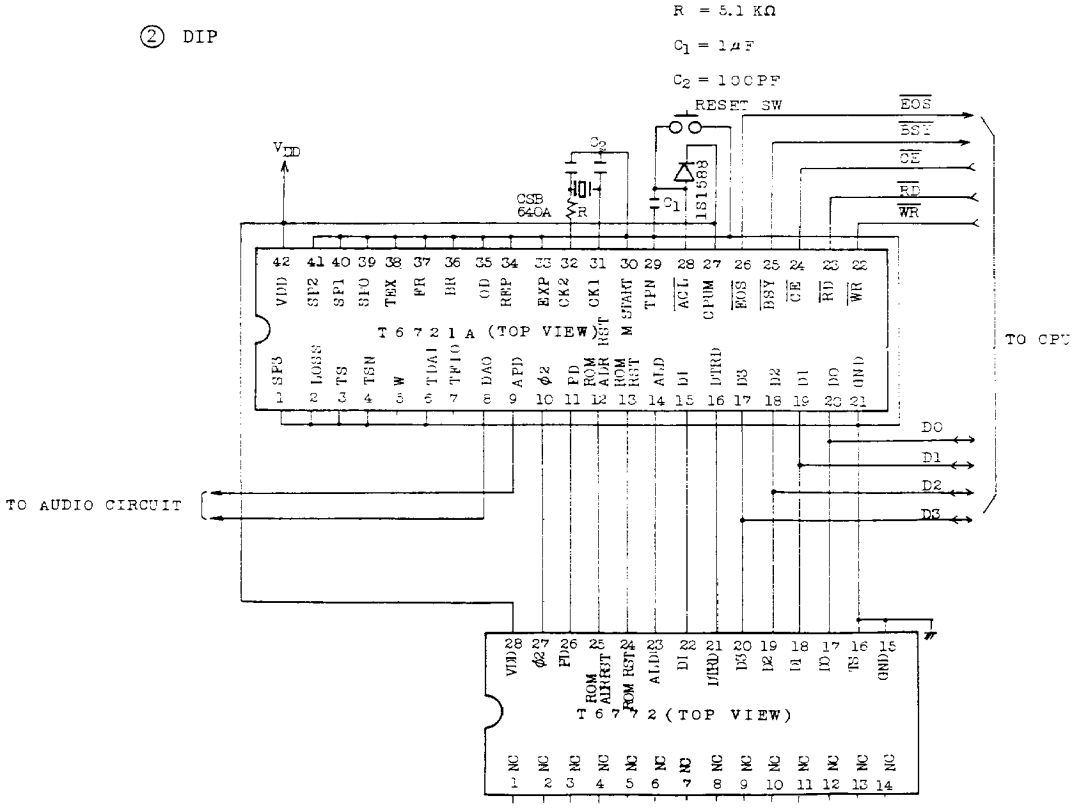
① FLAT PACKAGE



Notes: 1. The ceramic oscillator and capacitor connected to CK_1, and CK_2 of the T6721A should be arranged close to CK_1 and CK_2.

2. Other than NC terminal should not be used as relay terminals.

② DIP



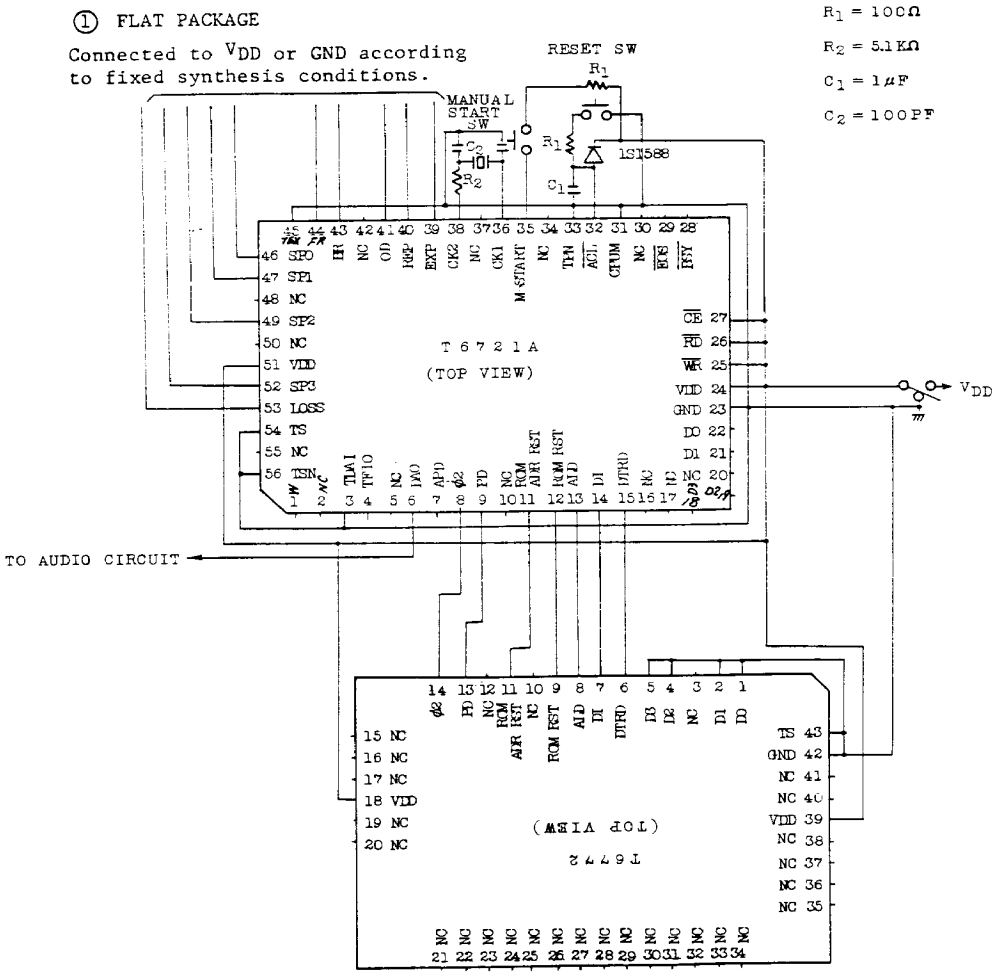
Notes: 1. The ceramic oscillator and capacitor connected to CK_1 and CK_2 of the T6721A should be arranged close to CK_1 and CK_2.

2. Other than NC terminal should not be used as relay terminals.

(1)-2 Manual Control Type

① FLAT PACKAGE

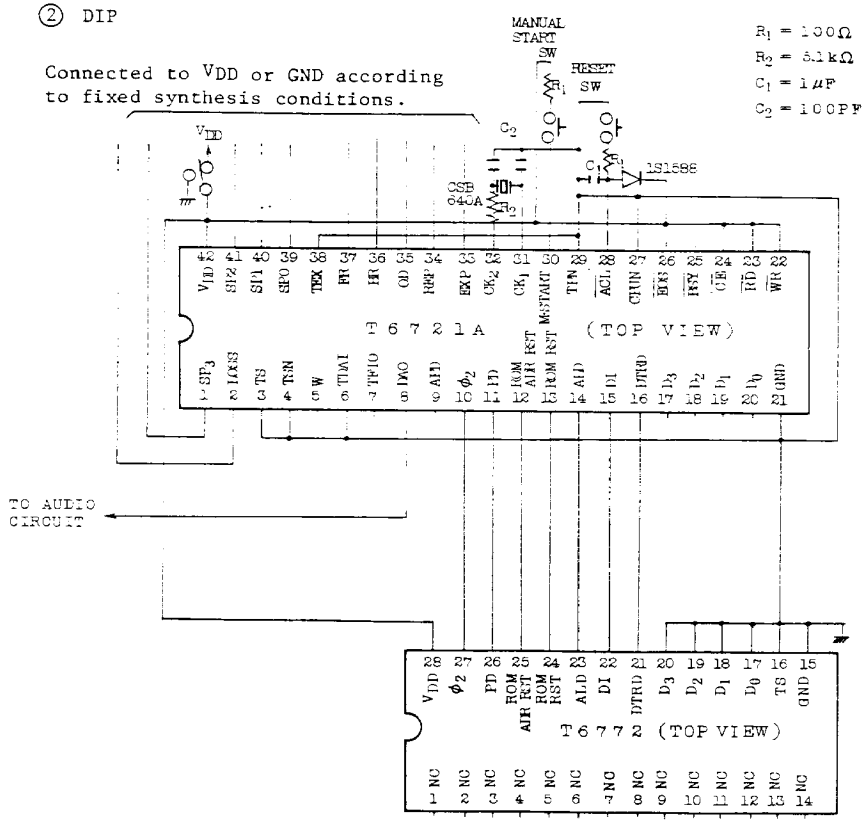
Connected to V_{DD} or GND according to fixed synthesis conditions.



Notes: 1. The ceramic oscillator and capacitor connected CK_1 and CK_2 of the T6721A should be arranged close to CK_1 and CK_2.

2. Other than NC terminal should not be used as relay terminals.

② DIP



Notes: 1. The ceramic oscillator and capacitor connected CK_1 and CK_2 of the T6721A should be arranged close to CK_1 and CK_2.

2. Other than NC terminal should not be used as relay terminals.

[9] ELECTRICAL CHARACTERISITCS

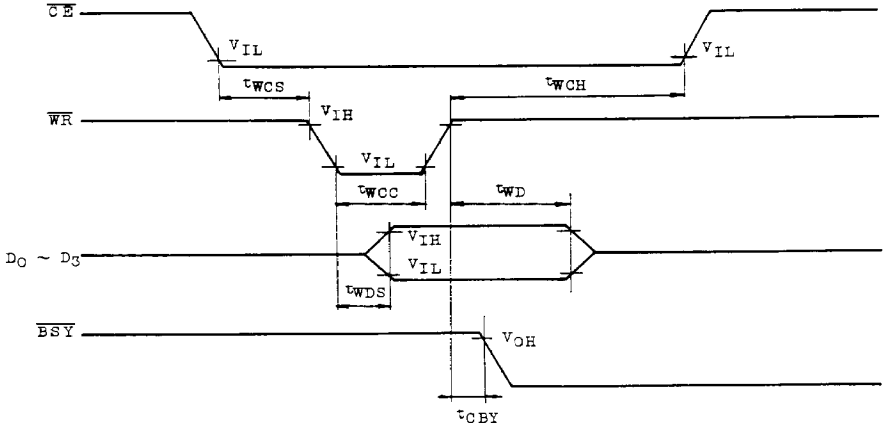
ABSOLUTE MAXIMUM RATING (Applicable to the T6721A, T6772 and T6684.)

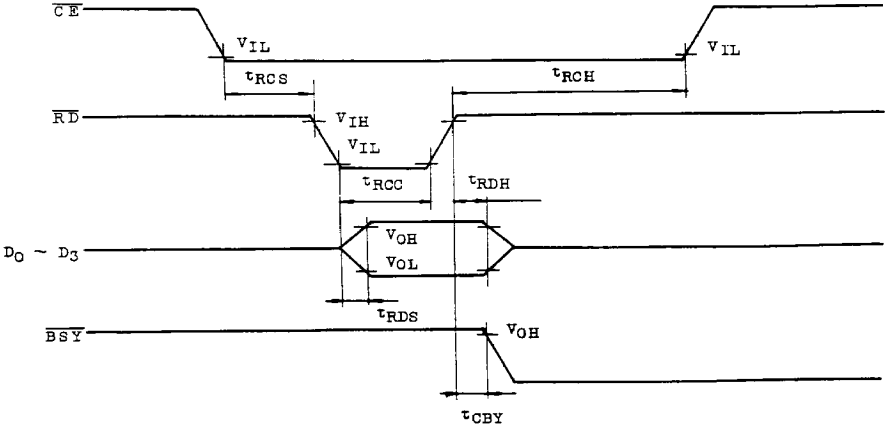
SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	-0.3 ∿ 6.0	V
V_{IN}	Input Voltage	-0.3 ∿ V_{DD}+0.3	V
Tstg	Storage Temperature	-55 ∿ 125	°C
Topr	Operating Temperature	-10 ∿ 55	°C

T6721A AC CHARACTERISTICS ($Ta = -10 \sim 55°C$, $C_L = 15pF$)

SYMBOL	PARAMETER	TEST CONDITION	STANDARD MIN.	STANDARD TYP.	STANDARD MAX.	UNIT
t_{WCS}	$\overline{CE}$ Fall → $\overline{WR}$ Fall time	$V_{DD} = 5V$	200	-	-	ns
t_{WCC}	$\overline{WR}$ Pulse width	"	4	-	-	μs
t_{WCH}	$\overline{WR}$ Rise → $\overline{CE}$ Rise time	"	200	-	-	ns
t_{WDS}	$\overline{WR}$ Fall Time → Effective data time	"	2	-	-	μs
t_{WD}	$\overline{WR}$ Rise → Data hold time	"	10	-	-	μs
t_{CBY}	$\overline{WR}$, $\overline{RD}$ Rise → $\overline{BSY}$ Fall time	"	-	-	2	μs
t_{RCS}	$\overline{CE}$ Fall → $\overline{RD}$ Fall time	"	200	-	-	ns
t_{RCC}	$\overline{RD}$ Pulse width	"	4	-	-	μs
t_{RCH}	$\overline{RD}$ Rise → $\overline{CE}$ Rise Time	"	200	-	-	ns
t_{RDS}	$\overline{RD}$ Fall → Effective data time	"	-	-	2	μs
t_{RDH}	$\overline{RD}$ Rise → Effective data hold time	"	-	-	2	μs

Definition of T6721A AC Characteristics





T6721A DC CHARACTERISTICS (GND=0V, V_{DD}=5V, Ta=25°C, Unless other wise specifed.)

(Standard MIN. and MAX. values are defined by their absolute values.)

SYMBOL	PARAMETER	APPLICATION PIN	CONDITIONS	STANDARD			UNIT
				MIN.	TYP.	MAX.	
V_{DD}	Supply Voltage	V_{DD}	—	3.5	5	5.7	V
$I_{DD}(1)$	Current dissipation during operation	V_{DD}	V_{DD}=5V, Output with no load	-	0.5	1.2	mA
$I_{DD}(2)$	Current during power down	VDD	"	-	0.2	3	uA
f_{ϕ}	Clock operation frequency	-	V_{DD}=3.5∿5.7V, Recommended circuit	144	160	176	kHz
f_{OSC}	" oscillation "	CK_2	" "	608	640	672	kHz
V_{IH}	"1" input voltage	Except $\overline{ACL}$	V_{DD}=3.5 ∿ 5.7V	V_{DD}-0.8	-	V_{DD}	V
V_{IL}	"0" "	"	"	0	-	0.8	V
V_{OH}	"1" output voltage	Except $\overline{ACL}$, DAO, CK_2	Output no load	V_{DD}-0.4	-	V_{DD}	V
V_{OL}	"0" "	"	"	0	-	0.4	V
$R_{INP}(1)$	Input pull-down resistor	M·START		-	30	-	kΩ
$R_{INP}(2)$	" pul-up "	DI, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$		-	500	-	kΩ
I_{IH}	"1" input current	Except TPN, MSTART, TS, TSN	V_{IN}=VDD	-	-	5	uA
I_{IL}	"0" "	Except DI, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$	V_{IN}=0V	-	-	-5	uA
$I_{OH}(1)$	"1" Output current (1)	$\overline{EOS}$, $\overline{BSY}$	V_{OUT}=V_{DD}/2	-0.4	-	-	mA
$I_{OH}(2)$	" (2)	D_0 ∿ D_3	V_{OUT}=V_{DD}-0.4V	-0.2	-	-	mA
$I_{OH}(3)$	" (3)	ϕ_2,W,APD,TFIO	"	-0.2	-	-	mA
$I_{OH}(4)$	" (4)	Except (1), (2), (3), CK_2 DA0 and $\overline{ACL}$	"	-0.2	-	-	mA
$I_{OL}(1)$	"0" " (1)	$\overline{EOS}$, $\overline{BSY}$	V_{OUT} = 0.4V	0.8	-	-	mA
$I_{OL}(2)$	" (2)	D_0 ∿ D_3	"	0.8	-	-	mA
$I_{OL}(3)$	" (3)	ϕ_2,W,APD,TFIO	"	0.5	-	-	mA
$I_{OL}(4)$	" (4)	Same as IOH(4)	"	0.2	-	-	mA
V_{OUT}	D/A converter output voltage	DAO	At time of output with no load	0	-	V_{DD}	V
R_{OUT}	" " impedance	DAO		-	50	-	kΩ

T6772 DC CHARACTERISTICS (GND=0V, V_{DD}=5V, Ta=25°C, Unless other wise specifed.)
(Standard MIN. and MAX. values are defined by their absolute values.)

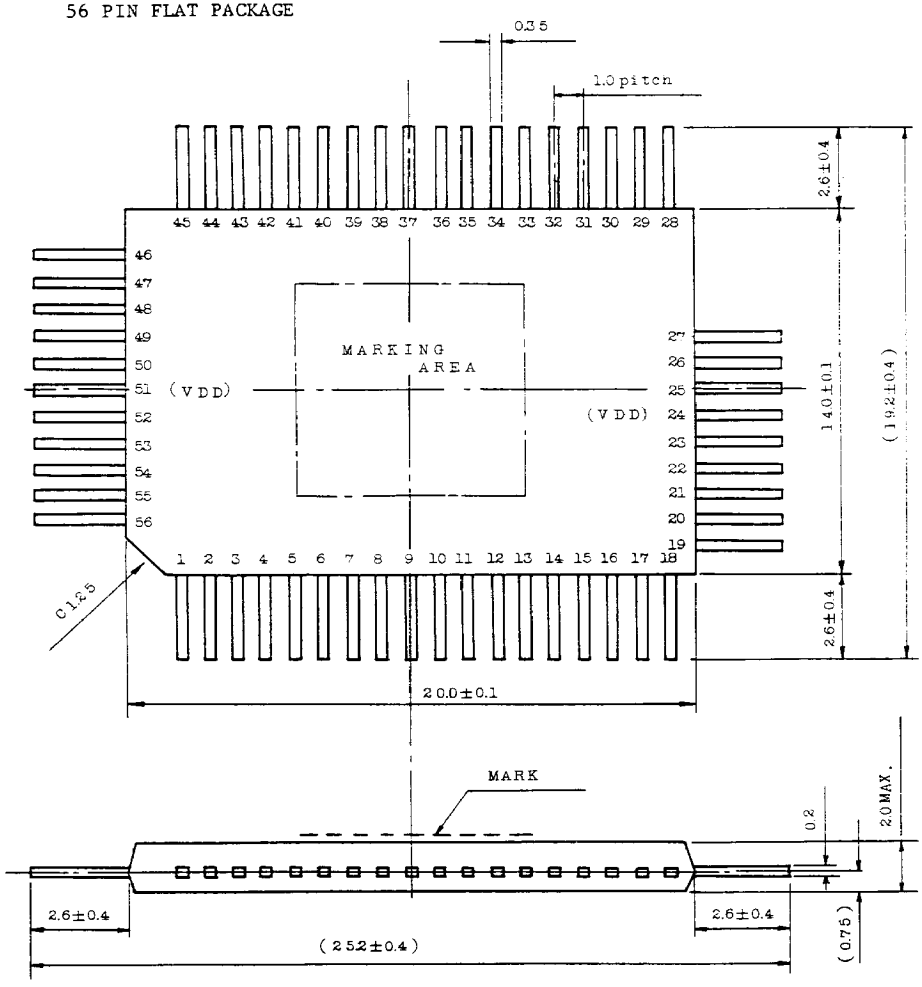
SYMBOL	PARAMETER	APPLICATION PIN	CONDITIONS	STANDARD			UNIT
				MIN.	TYP.	MAX.	
V_{DD}	Supply Voltage	V_{DD}	—	3.5	5	5.7	V
$I_{DD(1)}$	Current dissipation during operation (at selection)	V_{DD}	V_{DD}=5V, output with no load	-	40	80	μA
$I_{DD(2)}$	Current dissipation during operation (at nonselection)	V_{DD}	"	-	20	40	μA
$I_{DD(3)}$	Current during power down	V_{DD}	"	-	0.2	3	μA
fØ	Clock operation frequency	-	V_{DD}=3.5 ∿ 5.7V	144	160	176	kHz
V_{IH}	"1" input voltage	All-input PIN	"	V_{DD}-0.8	-	V_{DD}	V
V_{IL}	"0" "	"	"	0	-	0.8	V
V_{OH}	"1" output voltage	DI	Output no load	V_{DD}-0.4	-	V_{DD}	V
V_{OL}	"0" "	"	"	0	-	0.4	V
I_{IH}	"1" input current	All-input PIN	V_{IN} = V_{DD}	-	-	5	μA
I_{IL}	"0" "	"	V_{IN} = 0V	-	-	-5	μA
I_{OLK}	3-state output OFF leak	DI	$0 \leq V_{IN} \leq V_{DD}$	-	-	±5	μA
I_{OH}	"1" output current	"	V_{OUT}=V_{DD}-0.4V	-0.2	-	-	mA
I_{OL}	"0" "	"	V_{OUT} = 0.4V	0.2	-	-	mA

OUTLINE
56-4 HS

[10] Outline Drawings

Unit in mm

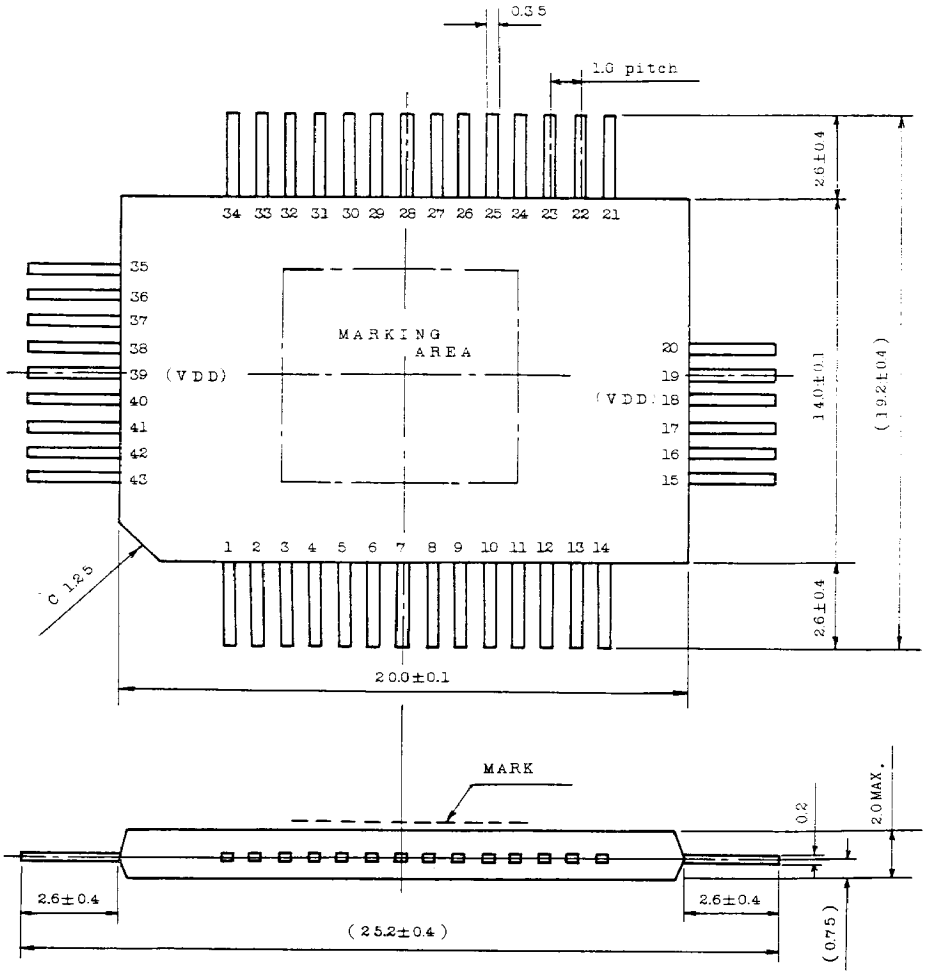
56 PIN FLAT PACKAGE



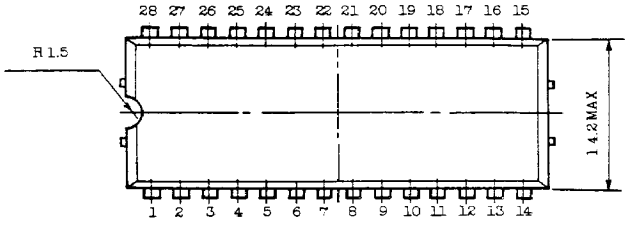
OUTLINE
43-4HS

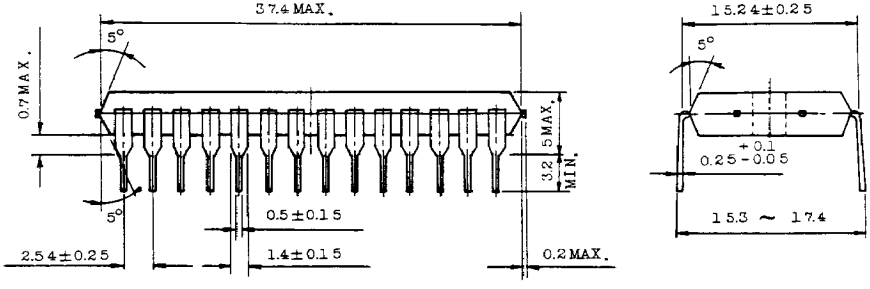
43 PIN FLAT PACKAGE

Unit in mm



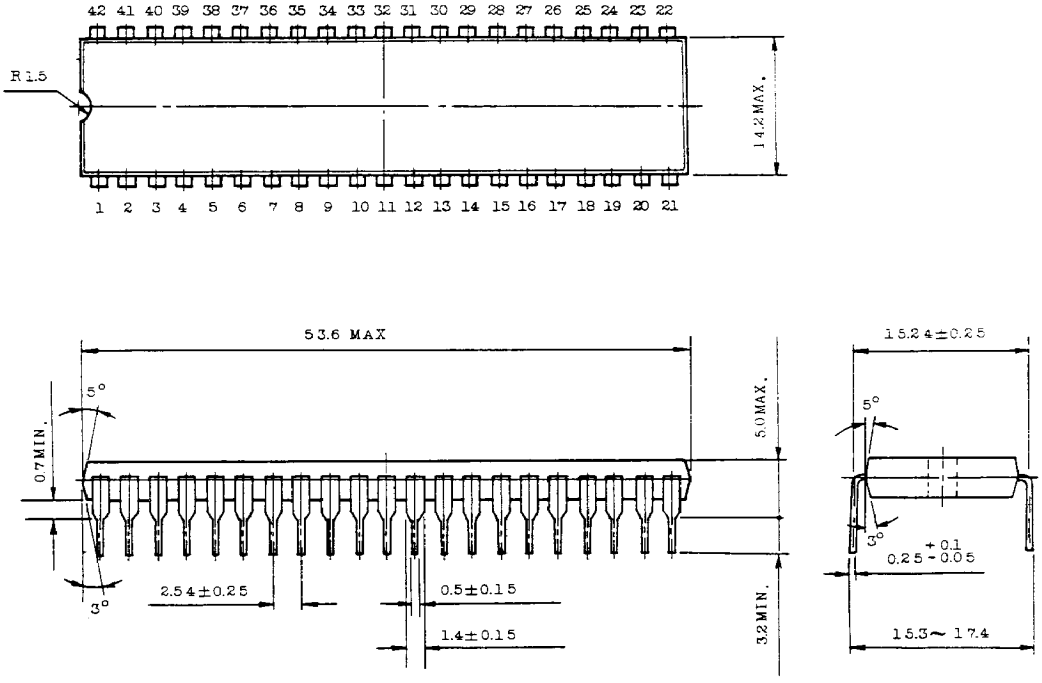
Unit in mm





Note: The lead pitch is 2.54mm and the tolerance is ±0.25mm against the theoretical center of each lead that is obtained on the basis of No.1 and No. 28 leads.

Unit in mm



Note: The lead pitch is 2.54mm and the tolerance is ±0.25mm against the theoretical center of each lead that is obtained on the basis of No. 1 and No. 42 leads.