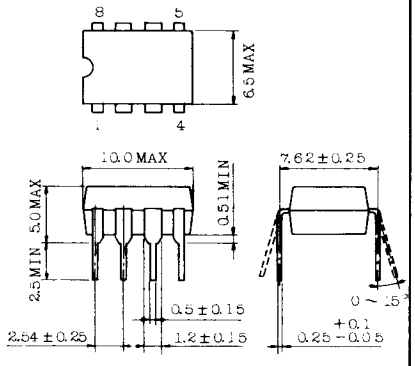
TA7502P

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

. High Gain
. Low Input Offset Voltage : V_{IO}=0.5mV (Typ.)

Unit in mm



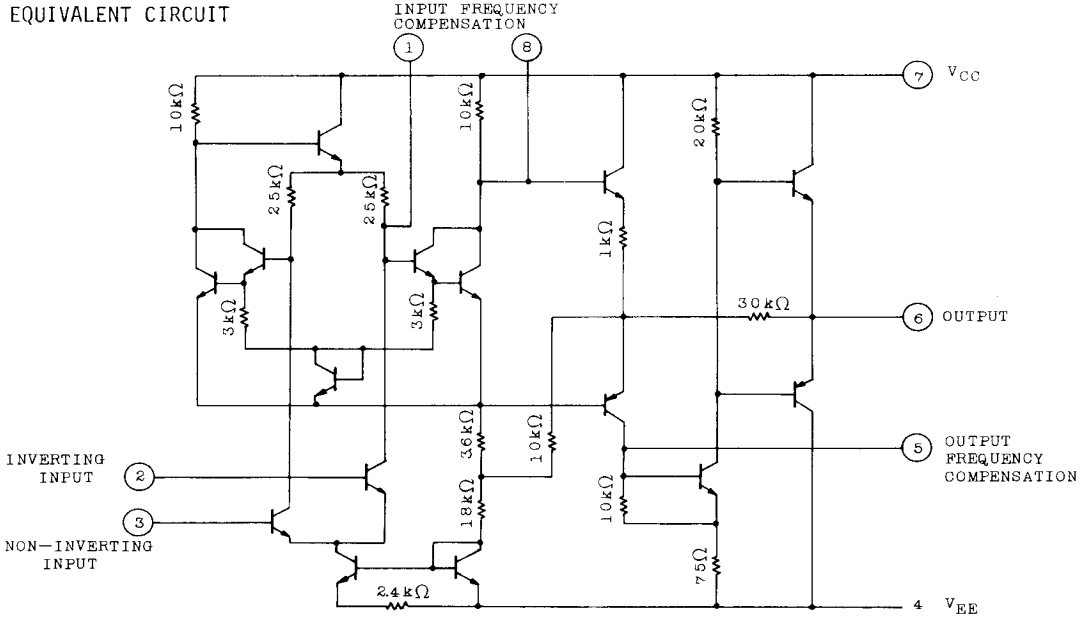
Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.8 leads.

JEDEC	—
TOSHIBA	3D8A-P

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC},V_{EE}	±18	V
Power Dissipation	P_D	300	mW
Differential Input Voltage	DV_{IN}	6	V
Input Voltage (V_{CC},V_{EE}=±15V)	V_{IN}	+10 -15	V
Output Short Circuit Current	I_{OS}	±20	mA
Operating Temperature	T_{opr}	-30 ~ 75	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C

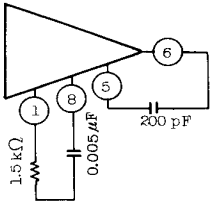
EQUIVALENT CIRCUIT



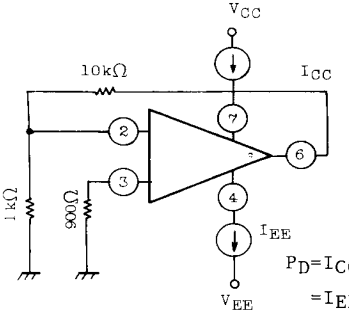
ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	2	$R_g \leqq 10k\Omega$	-	-	5	mV
Input Offset Current	I_{IO}	3	-	-	50	150	nA
Input Bias Current	I_I	3	-	-	200	500	nA
Input Impedance	Z_{IN}	-	f=1kHz	150	380	-	kΩ
Output Impedance	Z_o	-	f=1kHz	-	150	-	Ω
Voltage Gain	G_V	5	$R_L \geqq 2k\Omega$, f=1kHz $V_{OUT}=\pm 10V$	20	45	-	$\times 10^3$
Maximum Output Voltage	V_{OM}	4	$R_L \geqq 10k\Omega$	±12	±14	-	V
	V_{OMR}		$R_L \geqq 2k\Omega$	±10	±13	-	
Maximum Output Voltage Swing	V_{Op-p}	5	$R_L = 10k\Omega$, f=1kHz	24	28	-	V
Common Mode Input Voltage	CMV_{IN}	6	-	+9 -12	+10 -13	-	V
Common Mode Input Signal Rejection Ratio	CMRR	6	f=1kHz	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	2	$R_g=10k\Omega$	-	25	100	μV/V
Power Dissipation	P_D	1	-	-	80	150	mW
Input Noise Voltage	e_{np-p}	7	$R_g=10k\Omega$, f=0 ~100Hz	-	-	20	μV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	2	$R_g \leqq 100\Omega$, Ta=-30~75°C	-	-	20	μV/°C

TEST CIRCUIT



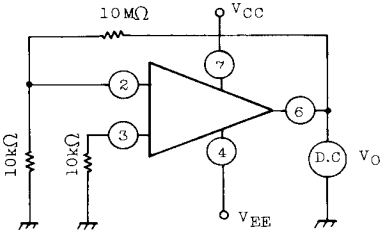
(1) P_D



$P_D = I_{CC}(V_{CC}-V_{EE})$

$= I_{EE}(V_{CC}-V_{EE})$

(2) V_{IO}, SVRR



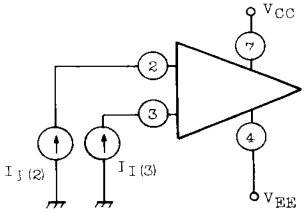
$V_{IO} = V_{OUT}/1000$

$SVRR = (V_{OUT1}-V_{OUT2})/5000$

V_{OUT1}: $V_{CC}=V_{EE}=17.5V$

V_{OUT2}: $V_{CC}=V_{EE}=12.5V$

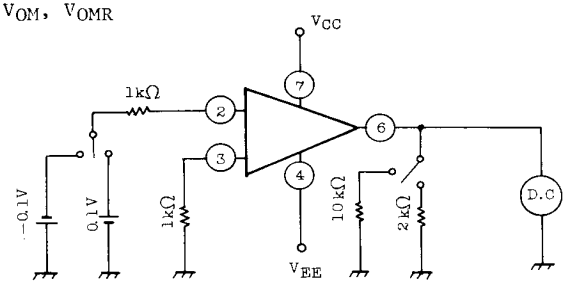
(3) I_I, I_{IO}



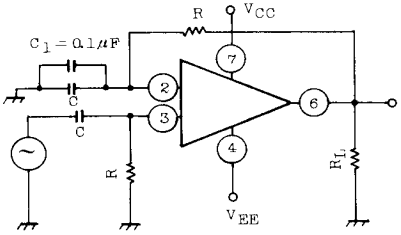
$$I_I = \frac{I_I(-)+I_I(+)}{2}$$

$I_{IO} = |I_I(-)-I_I(+)|$

(4) V_{OM}, V_{OMR}



(5) G_V, V_{Op-p}



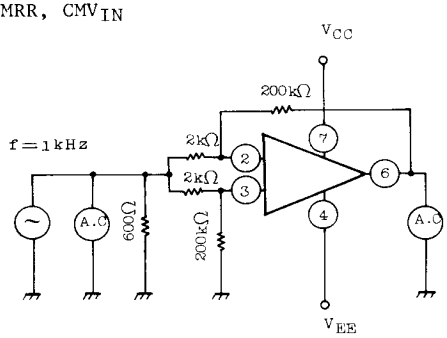
C : DC COUPLE

C_1 : HF BYPASS

$\omega \gg 1/RC$

$G_V = V_{OUT}/V_{IN}$

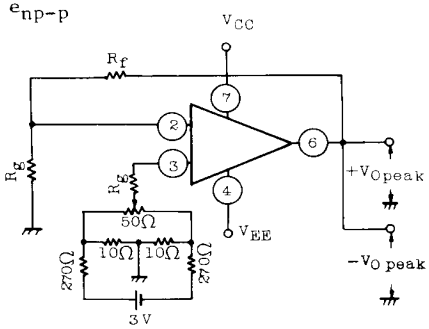
(6) CMRR, CMV_{IN}



$$CMRR = 20 \log \frac{70.7}{V_{OUT}} \text{ (dB)}$$

$V_{IN} = 0.707$ (V_{rms})

(7) e_{np-p}

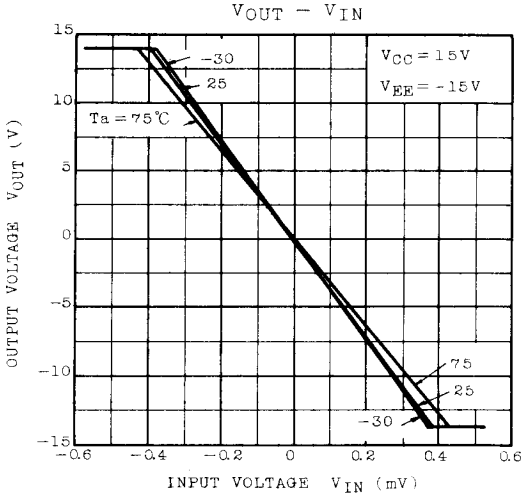


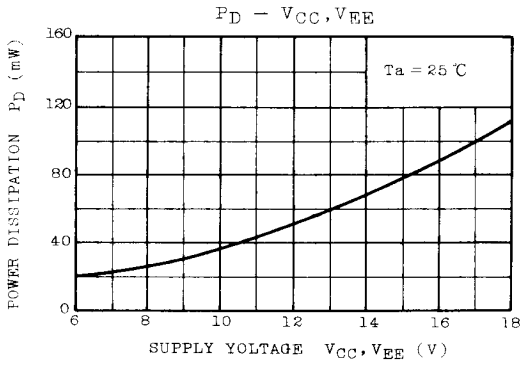
AFTER ADJUSTING BY VR,

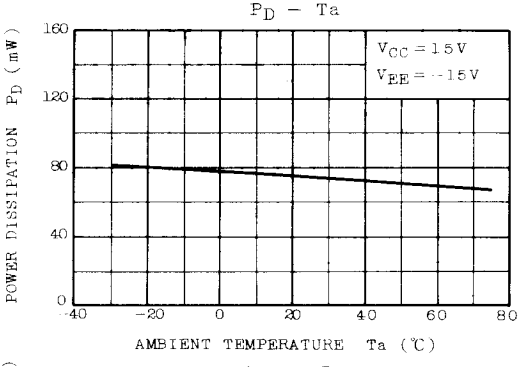
BEING TESTED $+V_{Opeak}$, $-V_{Opeak}$

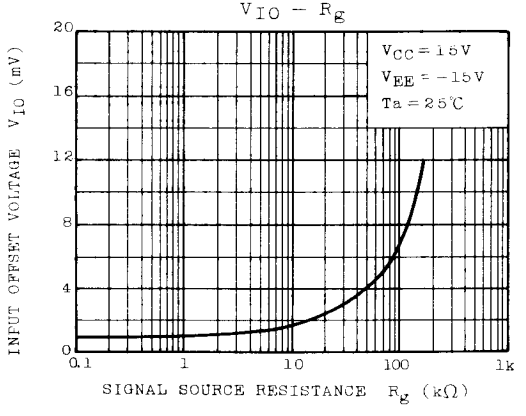
e_{np-p}

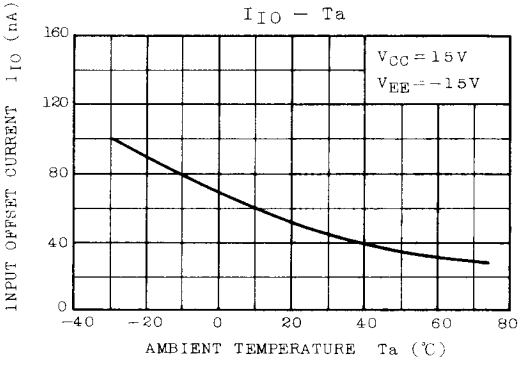
$$= \frac{R_g}{R_f}(|+V_{Opeak}| + |-V_{Opeak}|)$$

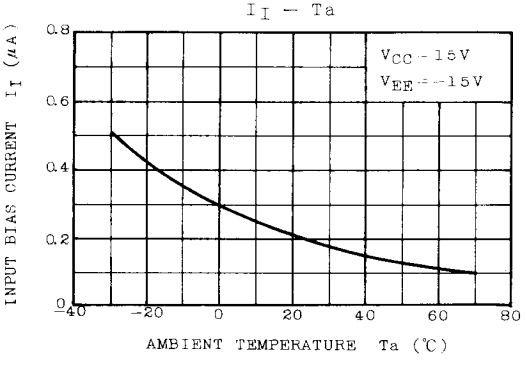


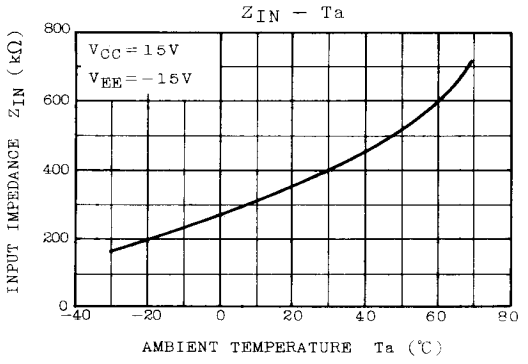


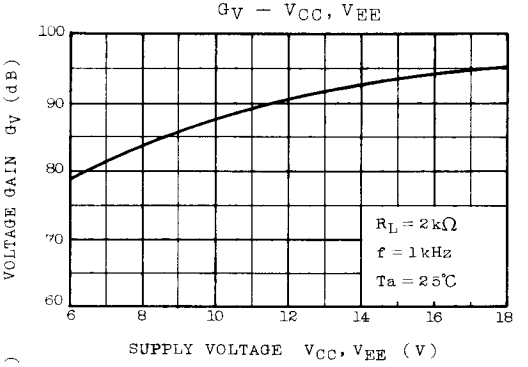


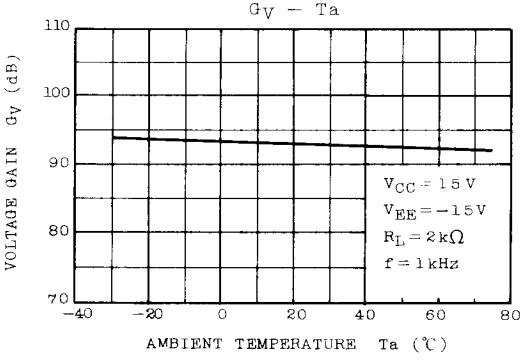


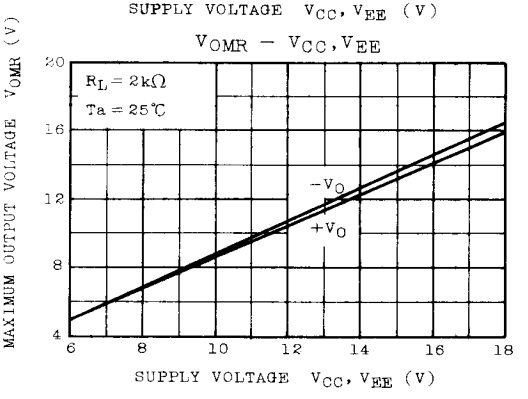


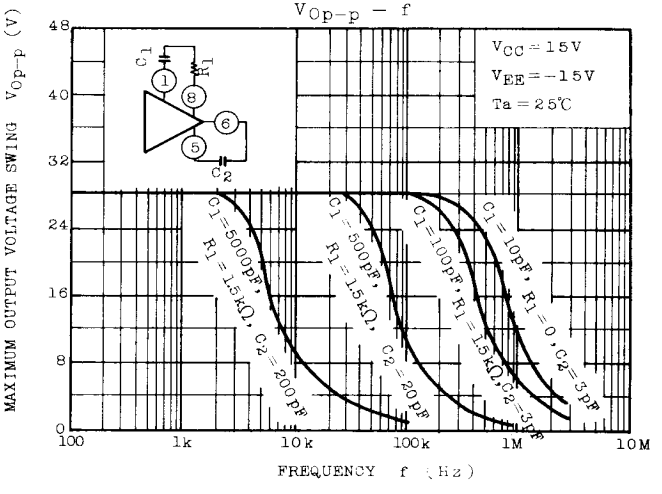


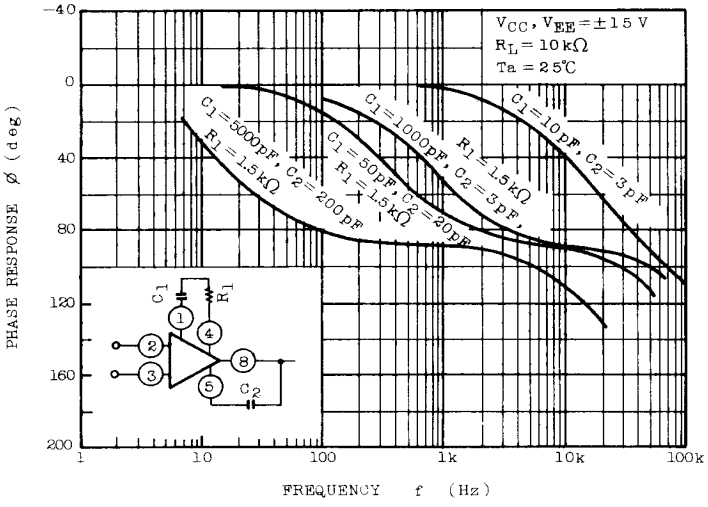


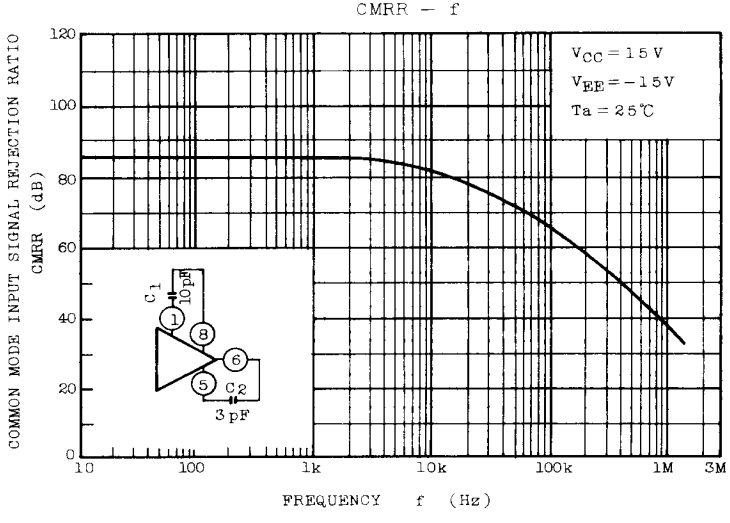


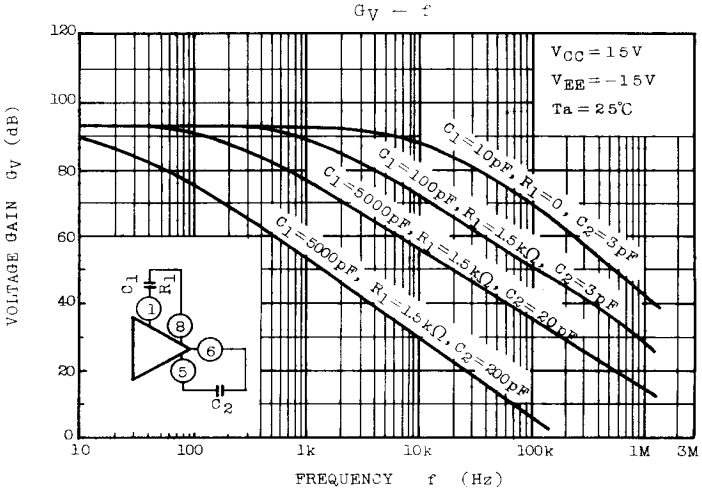


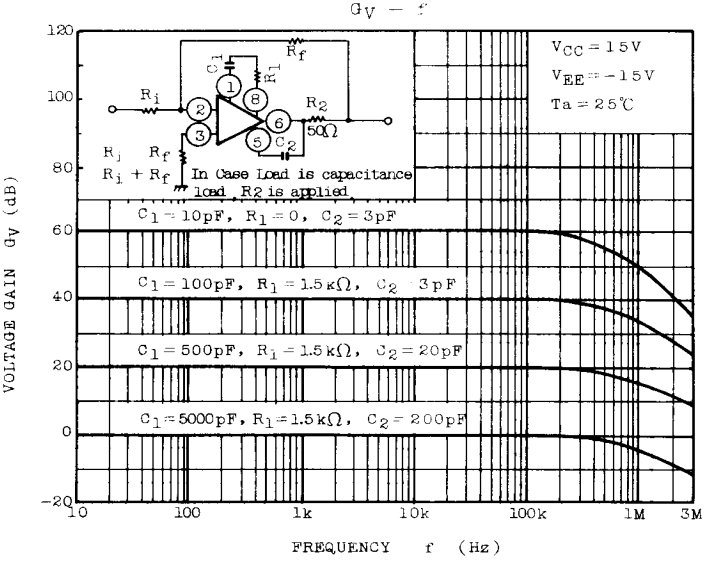


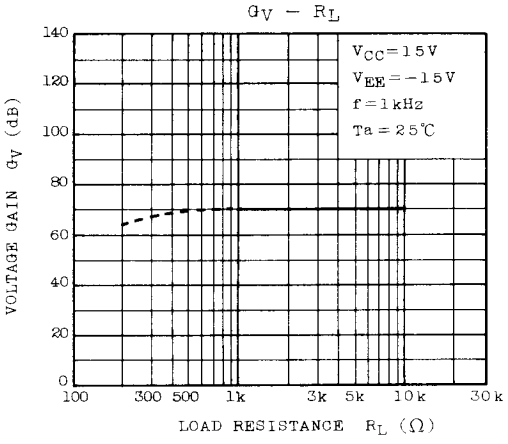


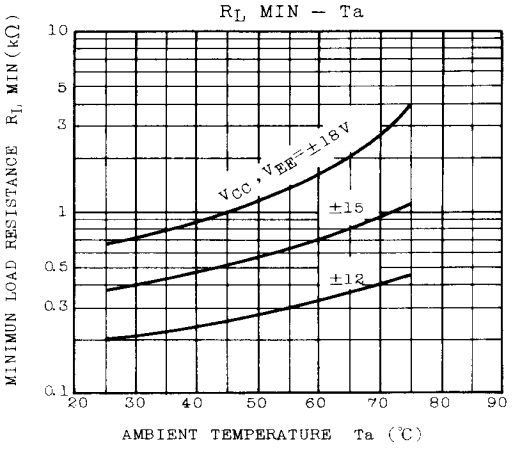


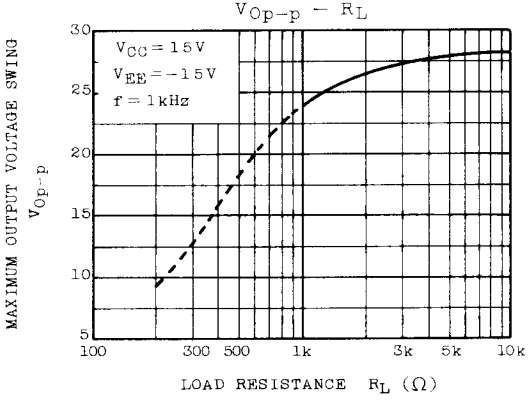












INPUT OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the TA7502P can easily be nulled,as shown in Fig.1 (a) In this way its stability directly depends on power supply stability. The other power supply V_{BB} should be added, as shown in Fig.1 (b), when power supply of operational amplifier is unregulated.

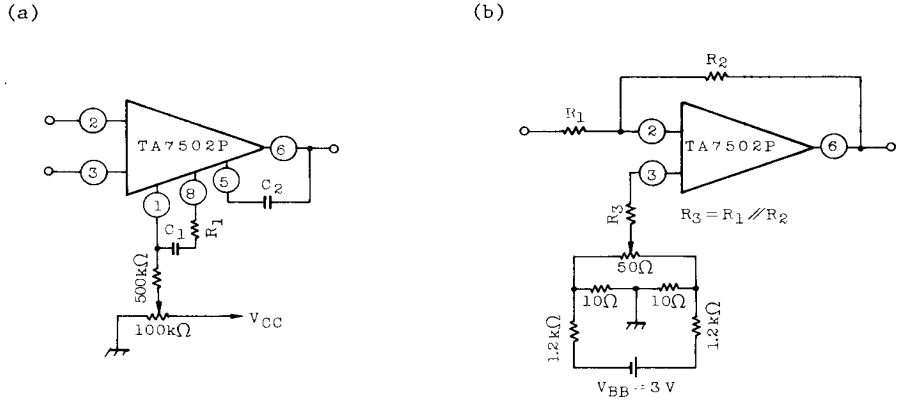


Fig. 1 OFFSET VOLTAGE ADJUSTMENTS

HYSTERESIS PREVENTION

The TA7502P has hysteresis at the positive area in its transfer characteristics. Because when voltage at Term.2 exceeds voltage at Term.1 (about 10V), the transistor in IC chip will be saturated and occur a kind of oscillation phenomenon by becoming positive feedback loop.

It is called "Latch up" and the TA7502P may give rise to abnormal behavior or catastrophic failure under this condition.

To protect against damage from latch up, a diode should be added between Term. 6 and Term. 8, as shown in Fig. 3 (a) and a resistor R should be added in series with feedback loop in Voltage follower application.

The TA7502P has a wide range of common mode input voltage (±9V), and its lineality is guranteed 9 volts in the electrical characteristics. Furthermore, it is possible to improve input voltage ranges by changing power supply voltage, as shown in Table 1.

(a) (b)

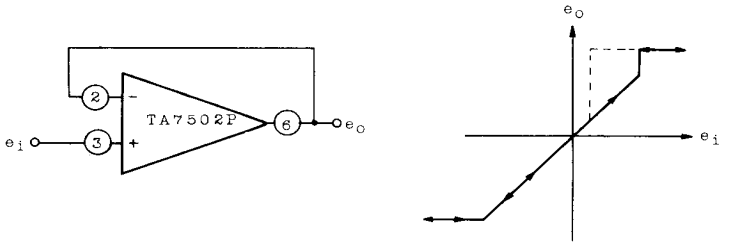
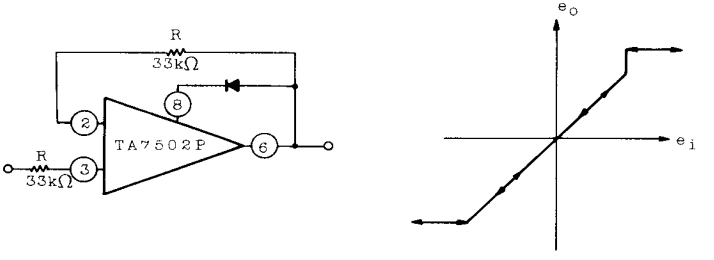


Fig. 2 BASIC VOLTAGE FOLLOWER AND TRANSFER CHARACTERISTIC



(a) VOLTAGE FOLLOWER FREE FROM LATCH UP (b) INPUT/OUTPUT CHARACTERISTICS

V_{CC} (V)	V_{EE} (V)	$CMV_{IN(+)}$ (V)	$CMV_{IN(-)}$ (V)
+5	-25	+1.4	-23.7
+10	-20	+6.0	-18.5
+15	-15	+11.0	-13.7
+20	-10	+15.9	-8.6
+25	-5	+21.1	-3.8

TABLE 1. SUPPLY VOLTAGE-COMMON MODE VOLTAGE

OVERLOAD PROTECTION

Input Protection against differential signal up to the levels of the maximum differential voltage can be provided by the diode clamps of Fig. 4.

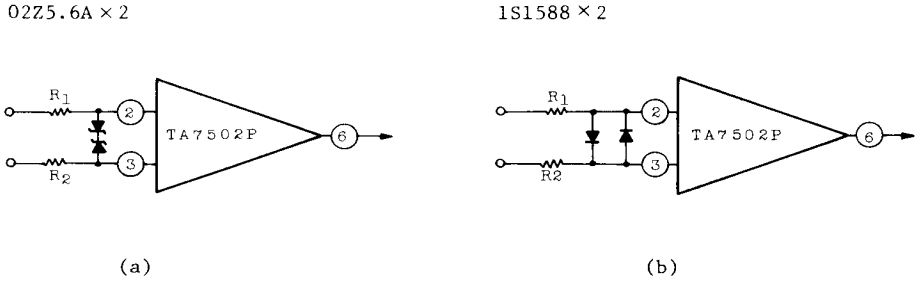


Fig. 4 INPUT PROTECTION AGAINST DIFFERENTIAL INPUT OVERLOAD

OUTPUT SHORT CIRCUIT PROTECTION

The TA7502P endure short circuit current of 80mA maximum for five second at 25°C ambient temperature without degradation. The circuit in Fig. 6 is applied to protect TA7502P from long time short current.

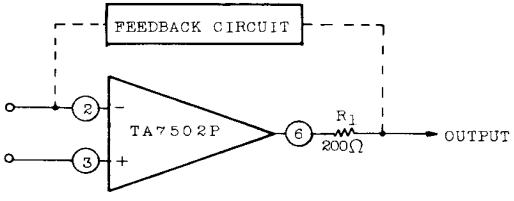


Fig. 5 OUTPUT SHORT CIRCUIT PROTECTION