TA7506P

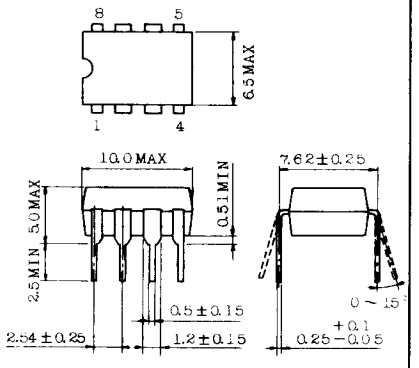
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

- High Gain
- High Input Resistance
- High Differential Input Voltage
- Wide Common Mode Input Voltage Range
- Absence of Latch-up
- Offset Null Capability
- Short Circuit Protection
- Feed Forward Compensation

INDUSTRIAL APPLICATION

Unit in mm



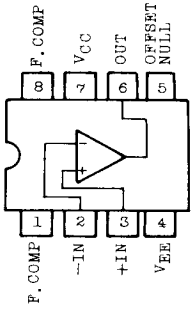
Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.8 leads.

JEDEC	–
TOSHIBA	3D8A-P

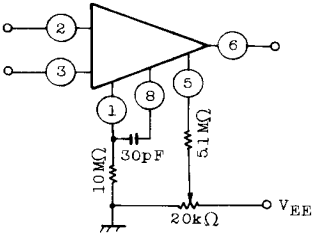
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC},V_{EE}	±18	V
Differential Input Voltage	DV_{IN}	±30	V
Input Voltage	V_{IN}	V_{CC} ~ V_{EE}	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	−30 ~ 75	°C
Storage Temperature	Tstg	−55 ~ 125	°C

PIN CONNECTION
(TOP VIEW)



VOLTAGE OFFSET NULL CAPABILITY



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ELECTRICAL CHARACTERISTICS (V_{CC}, V_{EE}=±5 ~ ±15V, Ta=25 °C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leq 50k\Omega$	-	-	5	mV
Input Offset Current	I_{IO}	2	-	-	2	50	nA
Input Bias Current	I_I	2	-	-	50	250	nA
Common Mode Input Voltage	CMV_{IN}	3	-	±12	-	-	V
Maximum Output Voltage	V_{OM}	4	$R_L \geq 10k\Omega$, V_{CC}=15V	±12	±14	-	V
	V_{OMR}	4	$R_L \geq 2k\Omega$, V_{EE}=-15V	±10	±13	-	V
Maximum Output Voltage Swing	V_{Op-p}	5	$R_L \geq 10k\Omega$, f=1kHz	24	28	-	V
Output Short Circuit Current	I_{OS}	4	-	-	25	-	mA
Input Impedance	Z_{IN}	-	f=1kHz	0.5	2	-	MΩ
Voltage Gain	G_V	5	V_{CC}=15V, V_{EE}=-15V $R_L \geq 2k\Omega$	25	180	-	$\times 10^3$
Common Mode Input Signal Rejection Ratio	CMRR	3	$R_g \leq 50k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g \leq 50k\Omega$	70	90	-	dB
Supply Current	I_{CC}, I_{EE}	-	V_{CC}=15V, V_{EE}=-15V	-	1.8	3	mA
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	1	$R_g \leq 50k\Omega$	-	-	30	μV/°C
Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	-	-	-	-	-0.6	nA/°C

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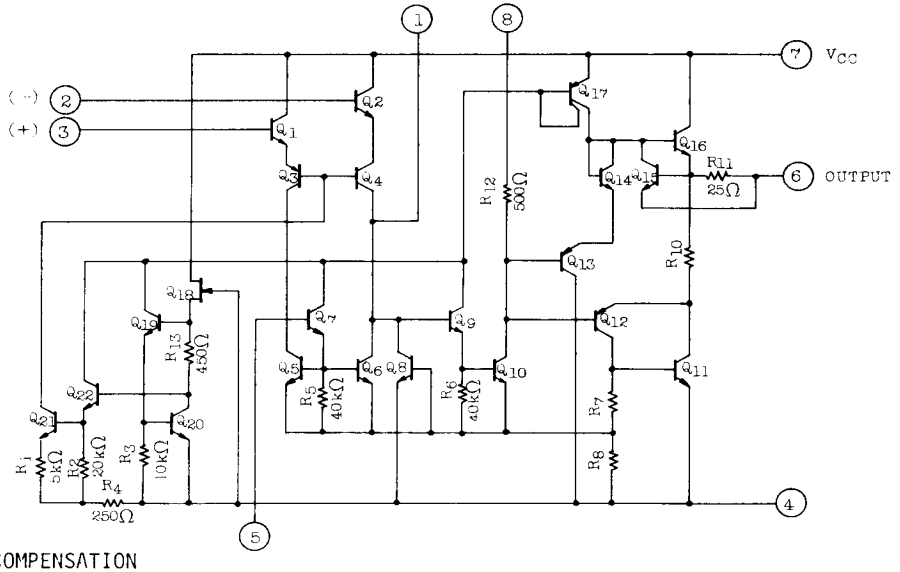
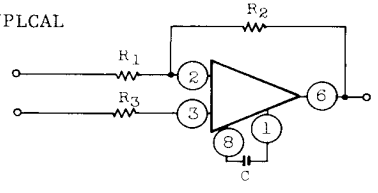
EQUIVALENT CIRCUIT

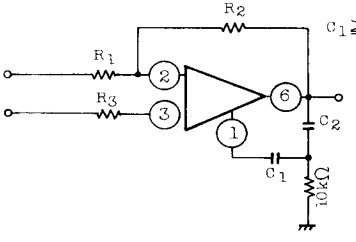


FREQUENCY COMPENSATION CIRCUIT

I. TYPLCAL



II. TWO POLE

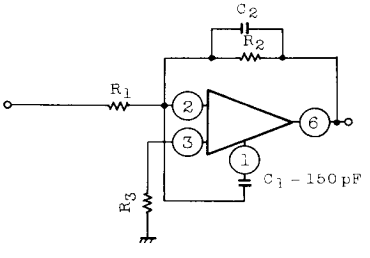


$C_1 \geqq \frac{R_1}{R_1 + R_2} \cdot C_s$

$C_2 \doteqdot 10C_1$

$C_s \doteqdot 30\,pF$

III. FEED FORWARD



$C_2 = \frac{1}{2\pi f_0 R_2}$

$f_0 \doteqdot 3\,MHz$

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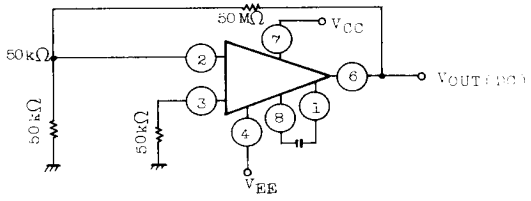
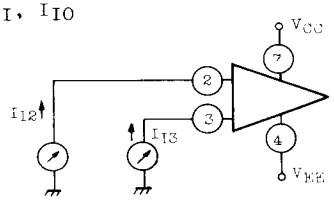
TEST CIRCUIT

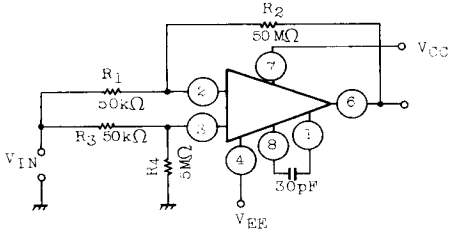
(1) V_{IO}, $\Delta V_{IO}/\Delta T$, SVRR



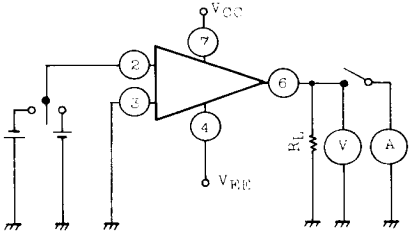
(2) I_I, I_{IO}



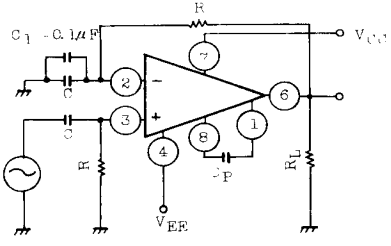
(3) CMV_{IN}, CMRR



(4) V_{OM}, V_{OMR}, I_{OS}



(5) G_V, V_{Op-p}



C_P : FREQUENCY COMPENSATION

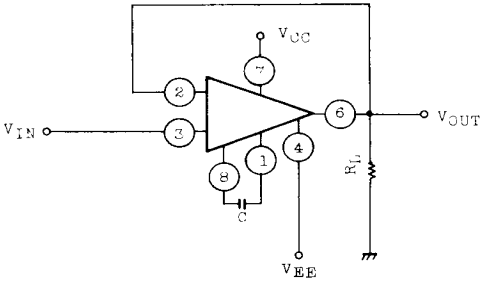
C : COUPLING CONDENSER

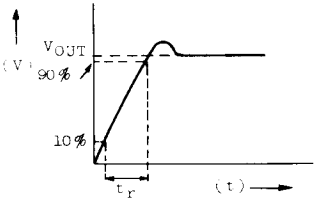
C_I : HIGH FREQUENCY CONDENSER

$\omega \gg 1/RC$

$G_V = V_{OUT}/V_{IN}$

(6) PULSE RESPONSE





$$dv/dt = \frac{1}{t_r} \cdot V_{OUT} \times 0.8 (V/\mu s)$$

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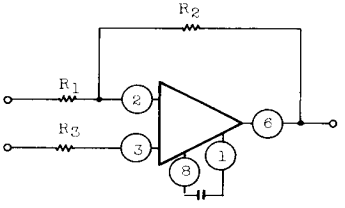
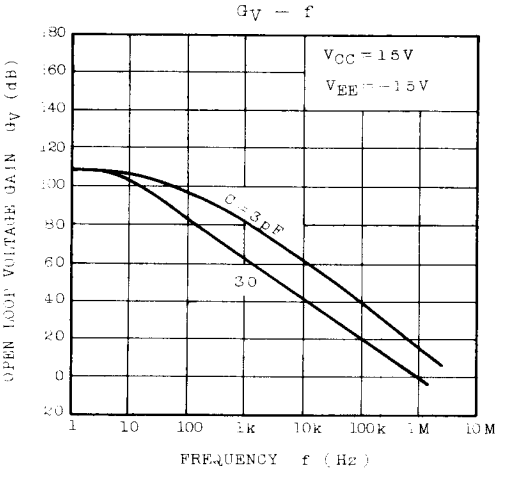
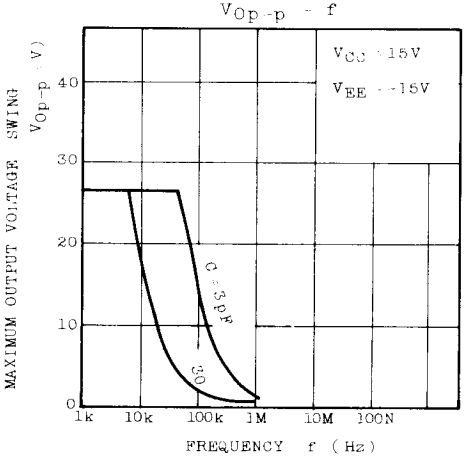
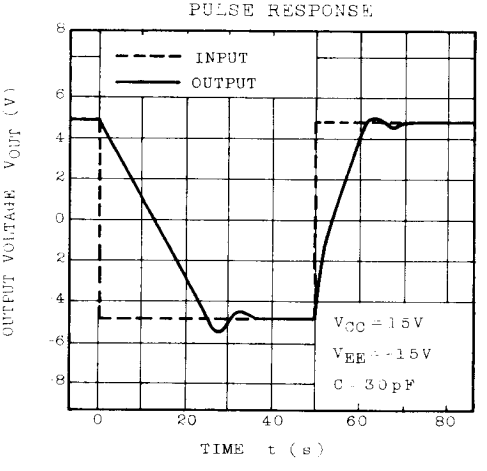
TYPLCAL AMPLIFIER CIRCUIT I









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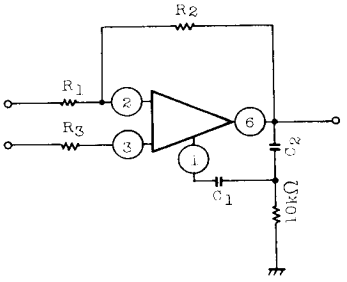
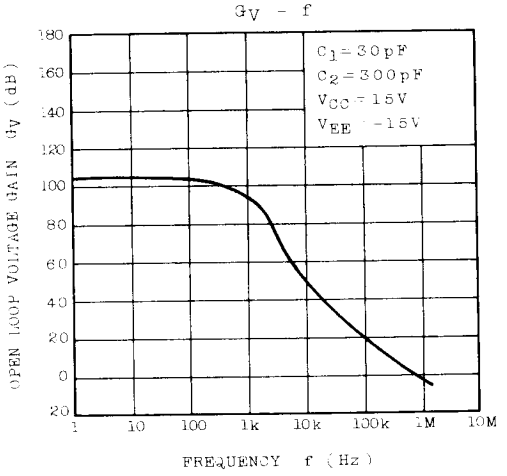
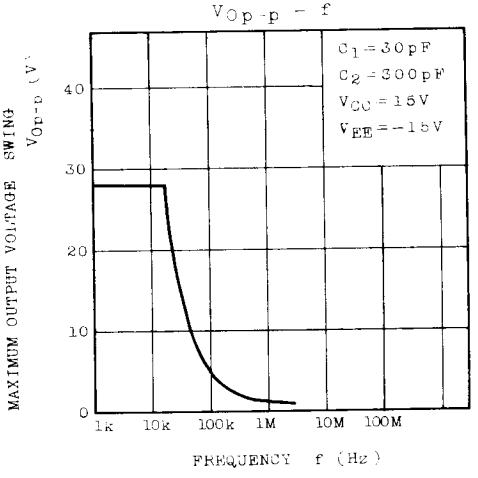
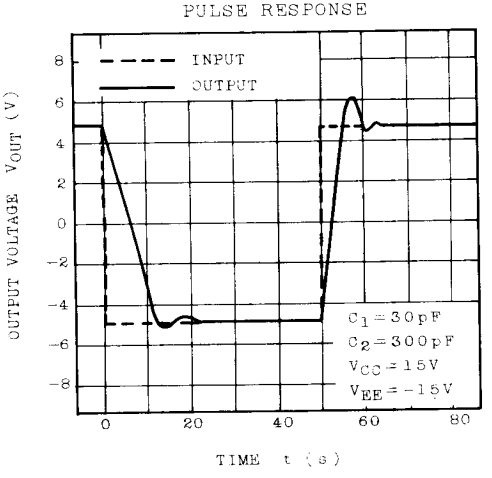
TYPICAL AMPLIFIER CIRCUIT II









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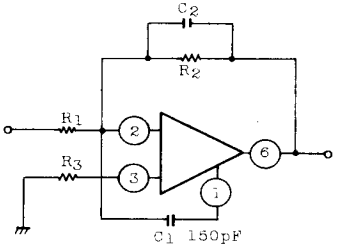
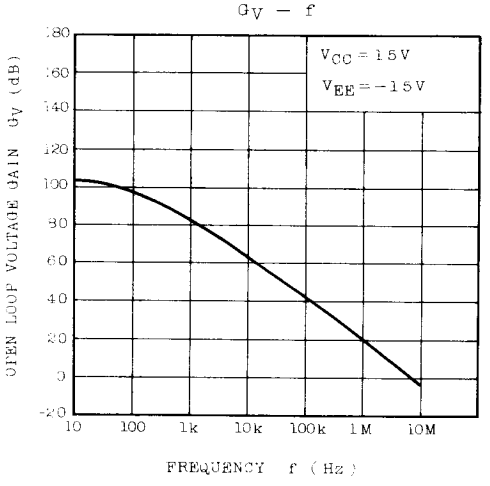
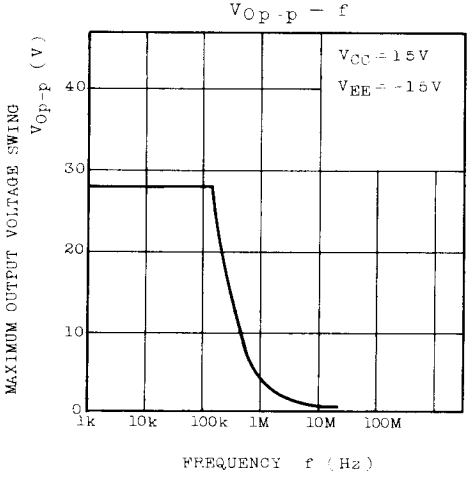
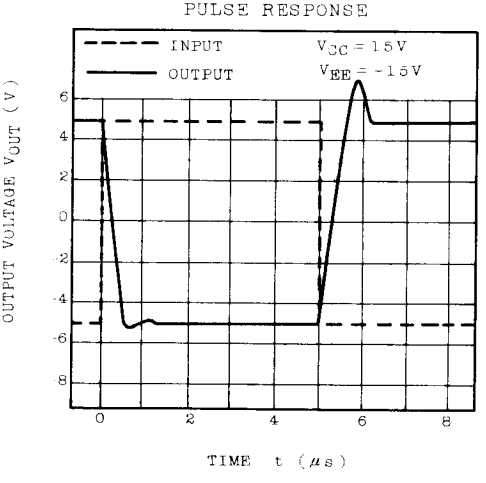
TYPICAL AMPLIFIER CIRCUIT Ⅲ









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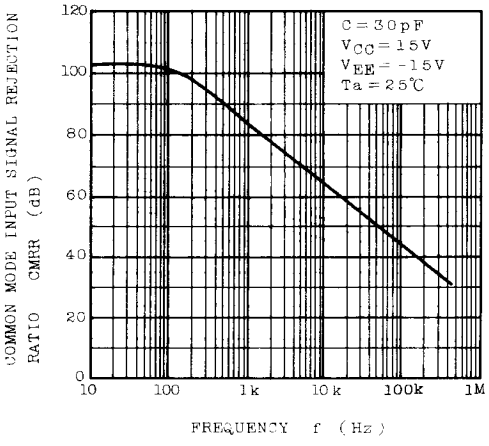
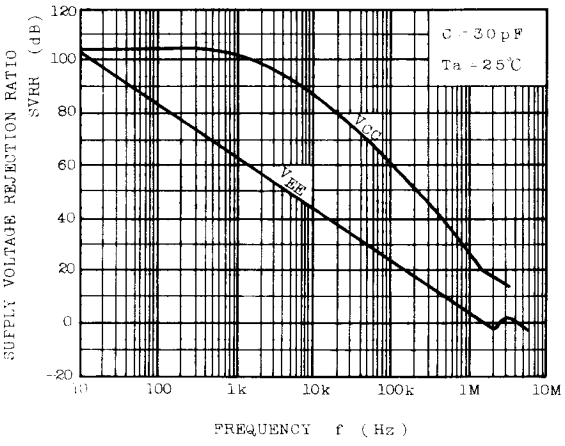
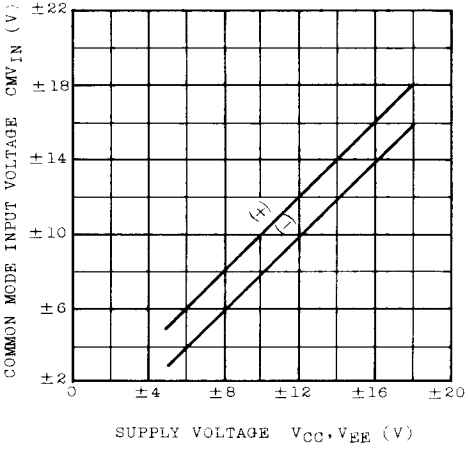
CMRR – f



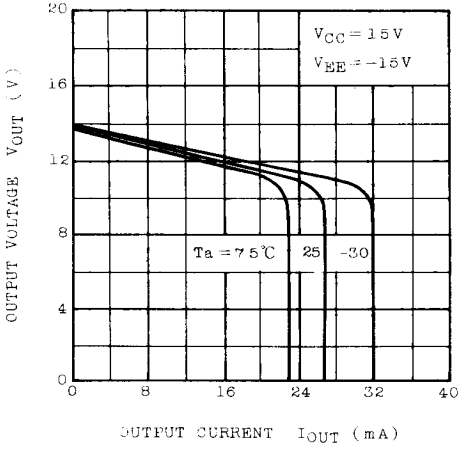
SVRR – f



CMV_{IN} – V_{CC}, V_{EE}



V_{OUT} – I_{OUT}



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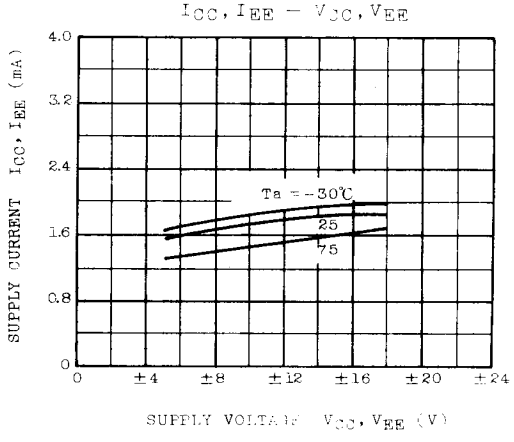

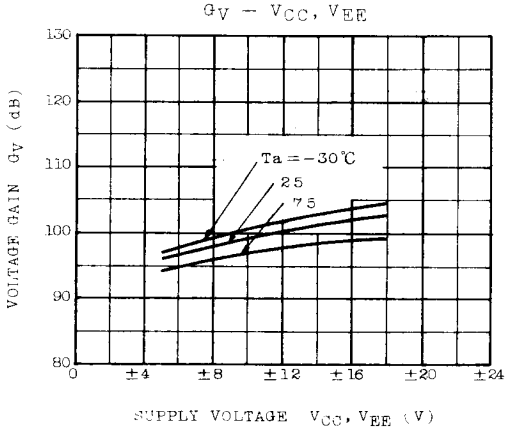

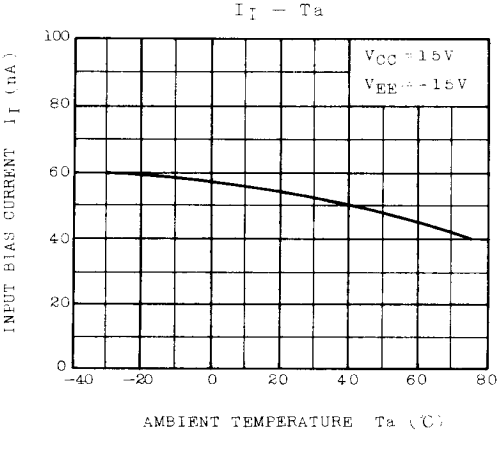

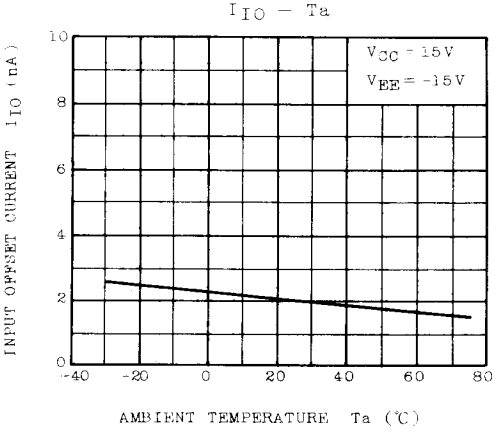

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