SN74AS8840
Digital Crossbar Switch

- High-speed programmable switch for parallel processing applications
- Dynamically reconfigurable for fault-tolerant routing
- 64 bidirectional data I/Os in 16 nibble (four-bit) groups
- Data I/O selection programmable by nibble
- Selectable stored-data or real-time inputs
- Two banks of control flip-flops for storing configuration programs
- Two selectable hard-wired switching configurations
- 156 pin grid-array package
- Texas Instruments quality and reliability

Description

The SN74AS8840 is a high-speed digital crossbar switch with four selectable control sources, including two banks of programmable control flip-flops and two hard-wired control circuits. The device can switch from 1 to 16 nibbles (4 to 64 bits) of data in a single cycle.

The 'AS8840 has 64 I/O pins arranged in 16 switchable nibbles (see Figure 1). A single input nibble can be broadcast to any combination of 15 output nibbles, or even to 16 nibbles (including itself) if operating off registered data. Multiple input nibbles can be switched to multiple outputs, depending on the programmed configurations available in the control flip-flops.

The digital crossbar switch is intended primarily for multiprocessor interconnection and parallel processing applications. The device can be used to select and transfer data from multiple sources to multiple destinations. Since it can be dynamically reprogrammed, it is suitable for use in reconfigurable networks for fault-tolerant routing.

Data Switching

The 64 I/O pins of the 'AS8840 are arranged in 16 nibble (four-bit) groups, and each group of four pins serves as bidirectional inputs to and outputs from a nibble multiplexer. During a switching operation each nibble passes four bits of stored or real-time data to the main 64-bit data bus. Each output multiplexer will independently select as its output one of the 16 nibbles from the 64-bit data bus.

Table 1. 'AS8840 Response to Control Inputs

Signal	High	Low
CNTR15-CNTR0	I/O pins for control flip-flops (see Table 6)	
CRADR1-CRADR0	Selects 16-bit groups of control flip-flops as destination or source for inputs or outputs on CNTR15-CNTR0 (see Table 6)	
CRCLK	Clocks CNTR15-CNTR0 inputs into control flip-flops	
CREAD	Selects second bank of control flip-flops to read on CNTR15-CNTR0 in 16-bit words addressed by CRADR1-CRADR0	Selects first bank of control flip-flops to read on CNTR15-CNTR0 in 16-bit words addressed by CRADR1-CRADR0
CRSEL1-CRSEL0	Selects one of four control functions to control the switch (see Table 2)	
CRSRCE	Control flip-flops load source select (see Table 4)	
CRWRITE	Control flip-flops destination select (see Table 4)	
LSCLK	Clocks LSH of data input into input registers on low-to-high transition	
MSCLK	Clocks MSH of data input into input registers on low-to-high transition	
$\overline{\text{OEC}}$	Inhibits output of data from control flip-flops	Enables output of data from control flip-flops
$\overline{\text{OED15}}$-$\overline{\text{OED0}}$	Inhibits output of data nibbles	Enables output of data nibbles
SELDLS	Selects real-time LSH data input to main internal data bus	Selects stored LSH data input to main internal data bus
SELDMS	Selects real-time MSH data input to main internal data bus	Selects stored MSH data input to main internal data bus
TP1-TP0	Test pins (see Table 7)	
$\overline{\text{WE}}$	Inhibits write to control flip-flops	Enables write to control flip-flops

Data nibbles are organized into two groups: the least significant half (D31-D0) and the most significant half (D63-D32). Stored versus real-time data inputs can be selected separately for the LSH and the MSH. Two clock inputs, LSCLK and MSCLK, are available to latch LSH and MSH data inputs into the data register.

The pattern of output nibbles resulting from the switching operation is determined by a selectable control source, either one of two banks of programmable control flip-flops or one of two hard-wire logic circuits. Inputs to the control flip-flops can be loaded either from the data bus or from control I/Os. A separate clock (CRCLK) is provided for loading the banks of control flip-flops.

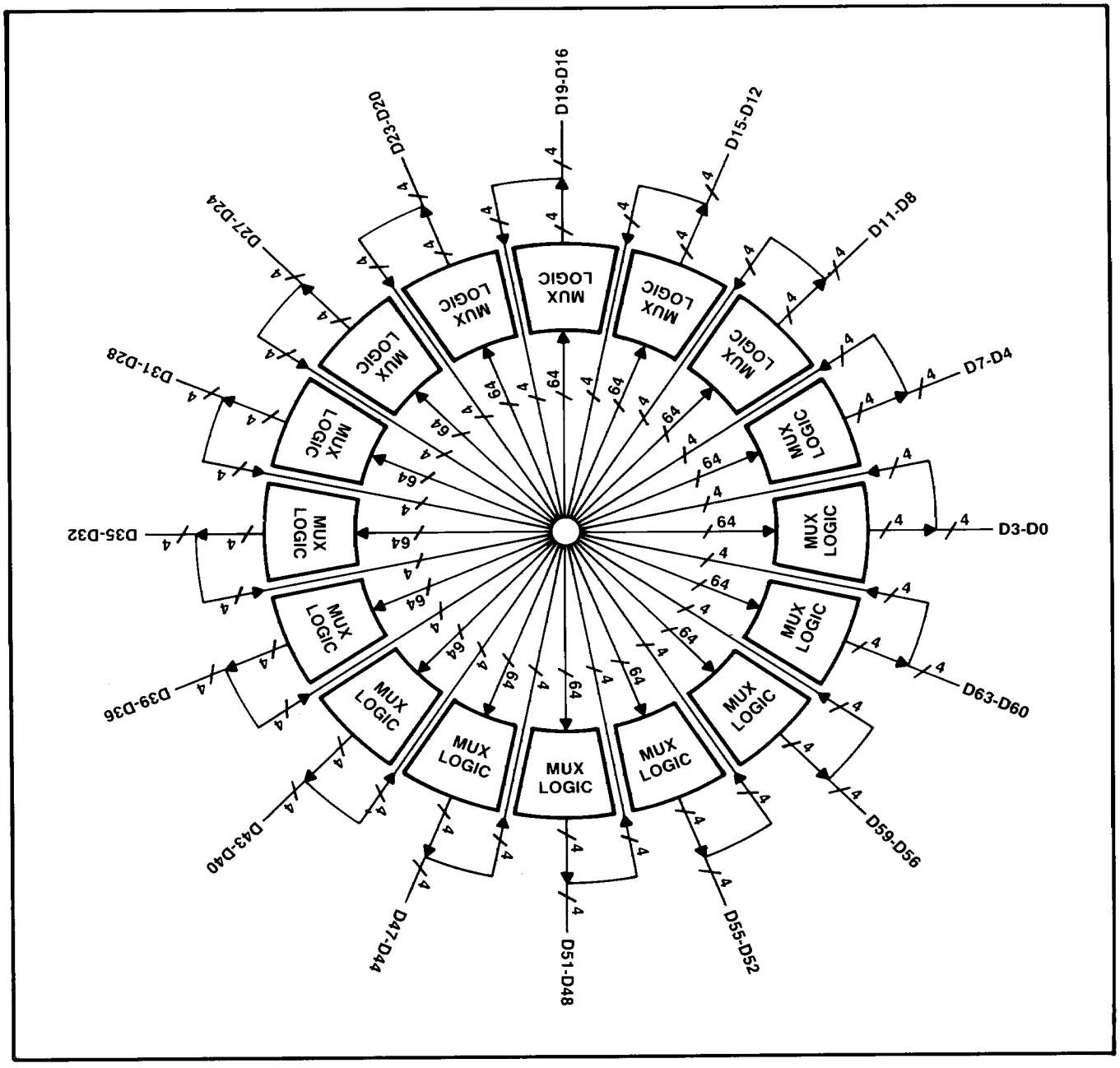

Figure 1. SN74AS8840 Digital Crossbar Switch

Architecture

The 'AS8840 digital crossbar switch has its 64 data I/Os arranged in 16 multiplexer logic groups, as shown in Figure 2. Each multiplexer logic group handles four bits of real-time input and four bits of stored-data input, and either input can be passed to the common data bus.

Two input multiplexer controls are provided to select between stored and real-time inputs. SELDLS controls input data selection for the LSH (D31-D0) of the 64-bit data input, and SELDMS for the MSH (D63-D32). The input register clocks, LSCLK and MSCLK, are grouped in the same way and are used to clock data into the registers in the multiplexer logic groups. The 16 data input nibbles make up the 64 data bits on the main bus.

This common bus supplies 16 data nibbles to a 16-to-1 output multiplexer in each multiplexer logic group (see Figure 3). As determined by one of four selectable control sources, the 16-to-1 output multiplexer selects a data nibble to send to the outputs via the three-state output driver.

Control of the input and output multiplexers determines the input-to-output pattern for the entire crossbar switch. Many different switching configurations can be set up by selecting the appropriate data inputs and by programming the control flip-flops to determine the outputs from the 16-to-1 multiplexers.

For example, the switch can be programmed to broadcast one data input nibble through the other 15 nibbles (60 outputs). Conversely, a 15-to-1 nibble multiplexer can be configured by programming the switch to select and output a single data nibble from the 64-bit bus.

Multiplexer Logic Group

External data flows into a multiplexer logic group on four data I/Os connected to an input data register and an input multiplexer. Data inputs are either clocked into the data register or passed directly to the main bus. The 64 bits of data from the main bus are presented to a 16-to-1 multiplexer, which selects the data nibble output.

Each of the 16 multiplexer logic groups contains two control flip-flop (CF) groups. Each CF group consists of four D-type edge-triggered flip-flops. In Figure 3 the CF groups are shown as CFXX1 and CFXX2, where XX indicates the number of the multiplexer logic group ($15 \geq XX \geq 0$). CFXX1 represents the 16 CF groups which make up flip-flop bank 1, and CFXX2 the 16 CF groups in flip-flop bank 2.

Table 2. 16-to-1 Output Multiplexer Control Source Selects

CRSEL1	CRSEL0	Control Source Selected
L	L	Flip-flop bank 1 (programmable)
L	H	Flip-flop bank 2 (programmable)
H	L	MSH/LSH exchange*
H	H	Read-back (output echoes input)*

*Hard-wired control function

In addition to the two banks of programmable flip-flops, two hard-wired control functions can be selected. The MSH/LSH exchange directs the input nibbles from each half of the switch to the control flip-flops or data outputs directly opposite, for example, D23-D20 $\longleftrightarrow$ D55-D52. The read-back function causes all 64 input bits to be output on the same I/Os on which they were input. Neither of the hard-wired control functions affects the contents of the control flip-flops.

A CF group can store a four-bit word (CFN3-CFN0) to select the output of the 16-to-1 multiplexer. One control word is loaded in each CF group, a total of 16 words in each flip-flop bank. Table 3 lists the output multiplexer control words, which can be loaded either 16 bits at a time on the control I/Os (CNTR15-CNTR0) or all 64 bits at once on the data inputs (D63-D0).

Each control word in Table 3 can be stored in a CF group and sent as an internal control signal to a 16-to-1 multiplexer. For example, any CF group loaded with the word "LHHH" can be used to select inputs D31-D28 as the outputs from a 16-to-1 multiplexer, or all 16 CF groups in bank 1 can be loaded with "LHHH" and the same outputs will be selected by the entire switch.

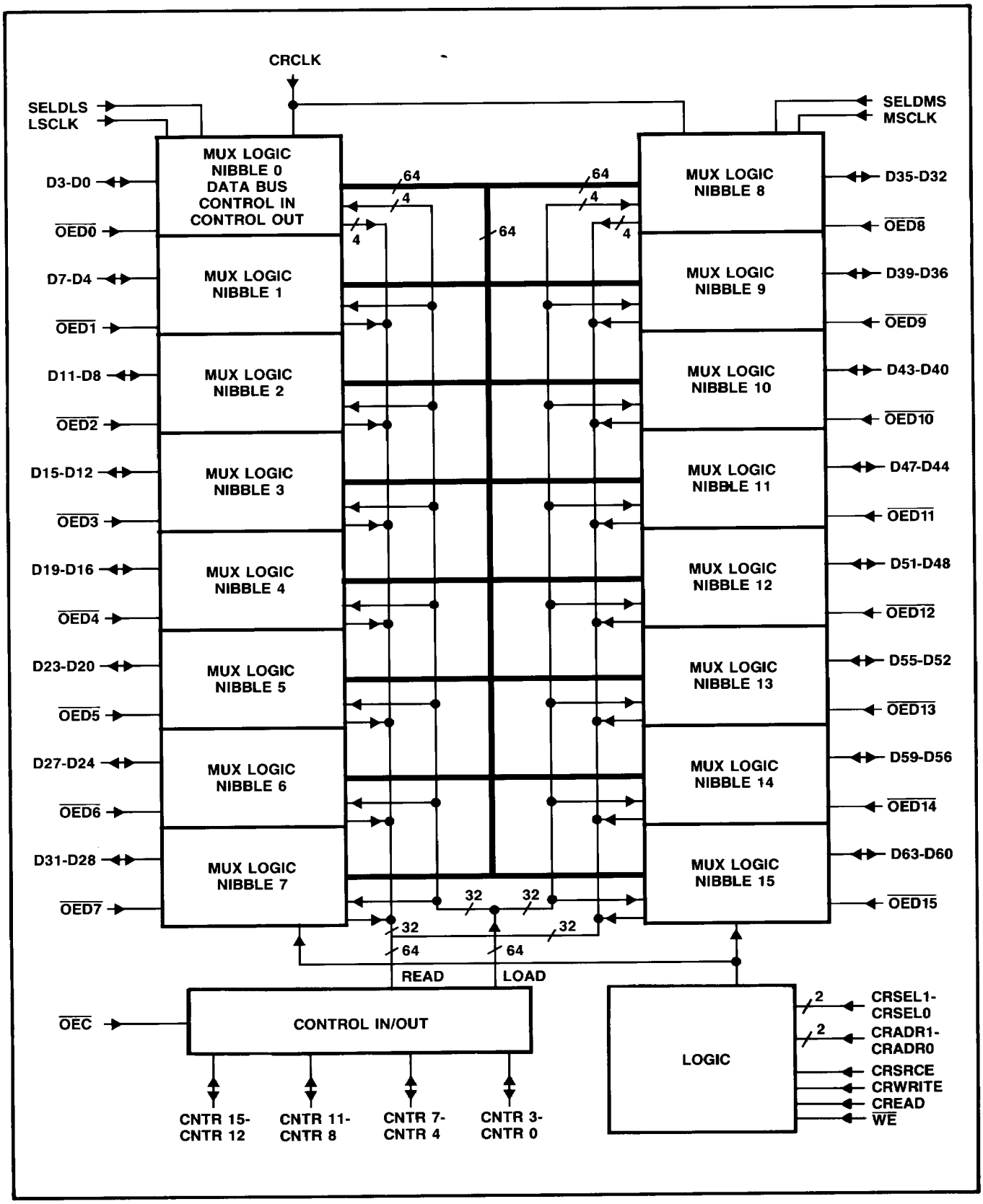

Figure 2. Block Diagram Digital Crossbar Switch AS8840

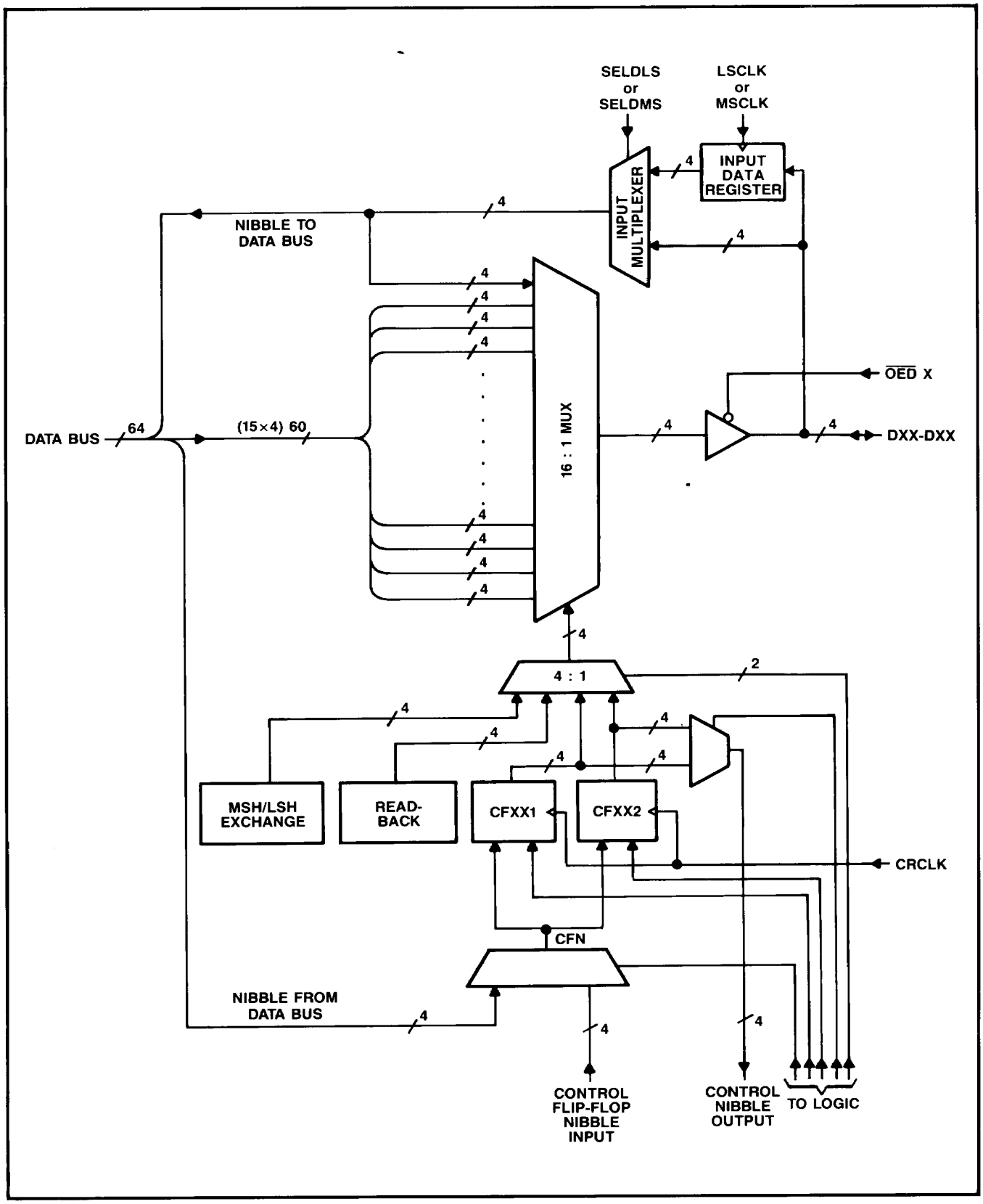

Figure 3. Data Nibble Multiplexer Logic

Table 3. 16-to-1 Output Multiplexer Control Words

Internal Signals CFN3	CFN2	CFN1	CFN0	Input Data Selected as Multiplexer Output
H	H	H	H	D63-D60
H	H	H	L	D59-D56
H	H	L	H	D55-D52
H	H	L	L	D51-D48
H	L	H	H	D47-D44
H	L	H	L	D43-D40
H	L	L	H	D39-D36
H	L	L	L	D35-D32
L	H	H	H	D31-D28
L	H	H	L	D27-D24
L	H	L	H	D23-D20
L	H	L	L	D19-D16
L	L	H	H	D15-D12
L	L	H	L	D11-D8
L	L	L	H	D7-D4
L	L	L	L	D3-D0

The control flip-flops load source select, CRSRCE, determines whether the control word is loaded from data inputs or from CNTR15-CNTR0.

CRWRITE selects whether bank 1 or bank 2 of flip-flops is being loaded. In effect CRSRCE and CRWRITE are used together to select the source and destination for loading flip-flops (see Table 4).

Table 4. Control Flip-Flops Load Selects

CRSRCE	CRWRITE	Source and Destination
L	L	CNTR inputs to flip-flop bank 1
L	H	CNTR inputs to flip-flop bank 2
H	L	Data inputs to flip-flop bank 1
H	H	Data inputs to flip-flop bank 2

When a bank of flip-flops is being loaded from the data inputs, the four signals, $\overline{WE}$, CRSRCE, CRWRITE, and the control flip-flop clock CRCLK, are used in combination to load all 16 control words (64 bits) in a single cycle. Data nibbles sent to the main bus by one half of the switch are loaded into the corresponding flip-flops of the other half. For instance, data inputs D3-D0 go to the data bus and then to the control flip-flops for data outputs D35-D32, while the inputs D35-D32 are sent to the control flip-flops for D3-D0. Table 5 shows the pattern of MSH/LSH exchange when a bank of flip-flops is loaded from data inputs.

Table 5. Inputs to Control Flip-Flops (CF)

Control Flip-Flop Nibbles	Data Outputs Affected	CNTR Inputs to Control Flip-Flops	Data Inputs to Control Flip-Flops
CF15	D63-D60	CNTR15-	D31-D28
CF14	D59-D56	CNTR12	D27-D24
CF13	D55-D52		D23-D20
CF12	D51-D48		D19-D16
CF11	D47-D44	CNTR11-	D15-D12
CF10	D43-D40	CNTR8	D11-D8
CF9	D39-D36		D7-D4
CF8	D35-D32		D3-D0
CF7	D31-D28	CNTR7-	D63-D60
CF6	D27-D24	CNTR4	D59-D56
CF5	D23-D20		D55-D52
CF4	D19-D16		D51-D48
CF3	D15-D12	CNTR3-	D47-D44
CF2	D11-D8	CNTR0	D43-D40
CF1	D7-D4		D39-D36
CF0	D3-D0		D35-D32

Control I/Os (CNTR15-CNTR0)

CNTR15-CNTR0 inputs can load four control words per CRCLK cycle to the flip-flop addresses (CFXX) selected by CRADR1-CRADR0, as shown in Table 6. The same address signals can be used to read out the flip-flop settings except that $\overline{OEC}$ is pulled low and no CRCLK signal is needed.

Table 6. Loading Control Flip-Flops from CNTR I/Os

CRADR1	CRADR0	$\overline{WE}$	CRCLK	Control (CNTR) I/O Numbers 15-12	11-8	7-4	3-0
L	L	L	⎍	CF12	CF8	CF4	CF0
L	H	L	⎍	CF13	CF9	CF5	CF1
H	L	L	⎍	CF14	CF10	CF6	CF2
H	H	L	⎍	CF15	CF11	CF7	CF3
X	X	H	X	Inhibit write to flip-flops			

Using the control I/Os to read the flip-flop settings can be valuable during debugging or diagnostics. Flip-flop settings are volatile and will be lost if the switch is powered off. An external program

controlling switch operation may need to read the flip-flop settings so that it can save and restore the current switch configurations.

Test Pins

Test pins, TP1-TP0, are provided for system testing. As Table 7 shows, these pins should be maintained high or open during normal operation. To force all outputs and I/Os low, low signals are placed on TP1-TP0 and all output enables ($\overline{OED15}$-$\overline{OED0}$ and $\overline{OEC}$). To force all outputs and I/Os high, TP1 is left low, TP0 is taken high, and all output enables are pulled low. When TP0 is left low and a high signal is placed on TP1, all outputs on the 'AS8840 are placed in a high-impedance state, isolating the chip from the rest of the system.

Table 7. Test Pin Inputs

TP1	TP0	$\overline{OED15}$-$\overline{OED0}$	$\overline{OEC}$	Result
L	L	L	L	All outputs and I/Os forced low
L	H	L	L	All outputs and I/Os forced high
H	L	X	X	All outputs placed in a high-impedance state
H	H	X	X	Normal operation (default state)

Examples

Most 'AS8840 switch configurations are straightforward to program, involving few control signals and procedures to set up the control words in the banks of flip-flops. Control signals and procedures for loading and using control words are shown in the following examples.

Broadcasting a Nibble

Any of the 16 data input nibbles can be broadcast to the other 15 data nibbles for output. For ease of presentation, input nibble D63-D60 is used in this example. Example 1 of Figure 4 presents the microcode sequence for loading flip-flop bank 1 and executing the nibble broadcast.

The low signal on CRSRCE selects CNTR15-CNTR0 as the input source, and the low signal on CRWRITE selects flip-flop bank 1 as the destination. Table 3 shows that to select data on D63-D60 as the output nibble the four bits in the control word CFN3-CFN0 must be high; therefore the CNTR15-CNTR0 inputs are coded high. The four microcode instructions shown in Example 1 load the same control word from CNTR15-CNTR0 into all 16 CF groups of bank 1.

Once the control flip-flops have been loaded, the switch can be used to broadcast nibble D63-D60 as programmed. The microcode instruction to execute the broadcast is shown as the last instruction in Example 1. $\overline{WE}$ is held high and the data to be broadcast is input on D63-D60. The high signal on SELDMS selects a real-time data input for the broadcast. MSCLK and LSCLK (not shown) can be used to load the input registers if the input nibble is to be retained. No register clock signals are needed if the input data is not being stored.

The bank of control flip-flops not selected as a control source can be loaded with new control words or read out on CNTR15-CNTR0 while the switch is operating. For example, the MSH data inputs can be used to load flip-flop bank 2 of the LSH while bank 1 of the LSH is controlling data I/O.

Programming an MSH/LSH Exchange

A second, more complicated example involves programming the switch to swap corresponding nibbles between the MSH and the LSH (first nibble in the LSH for first nibble in the MSH, and so on). This swap can be implemented using the hard-wired logic circuit selected when CRSEL1 is high and CRSEL0 low. Programming this swap without using the MSH/LSH exchange logic requires loading a different control word into each mux logic group. This is described below for purposes of illustration.

Each nibble in one half, either LSH or MSH, selects as output the input from the corresponding nibble in the other half. The input nibble from

Example 1. Programming a Nibble Broadcast

Inst. No.	CRSRCE	CRWRITE	CRADR1	CRADR0	CNTR I/O Numbers 15-12	11-8	7-4	3-0	CRSEL1	CRSEL0	$\overline{WE}$	SELDMS	SELDLS	$\overline{OED15}$-$\overline{OED0}$	$\overline{OEC}$	CRCLK
1	0	0	0	0	1111	1111	1111	1111	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
2	0	0	0	1	1111	1111	1111	1111	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
3	0	0	1	0	1111	1111	1111	1111	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
4	0	0	1	1	1111	1111	1111	1111	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
5	X	X	X	X	XXXX	XXXX	XXXX	XXXX	0	0	1	1	X	1000 0000 0000 0000	1	None

Example 2. Programming an MSH/LSH Exchange on CNTR Inputs

Inst. No.	CRSRCE	CRWRITE	CRADR1	CRADR0	CNTR I/O Numbers 15-12	11-8	7-4	3-0	CRSEL1	CRSEL0	$\overline{WE}$	SELDMS	SELDLS	$\overline{OED15}$-$\overline{OED0}$	$\overline{OEC}$	CRCLK
1	0	1	0	0	0100	0000	1100	1000	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
2	0	1	0	1	0101	0001	1101	1001	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
3	0	1	1	0	0110	0010	1110	1010	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
4	0	1	1	1	0111	0011	1111	1011	X	X	0	X	X	XXXX XXXX XXXX XXXX	1	⌐
5	X	X	X	X	XXXX	XXXX	XXXX	XXXX	0	1	1	1	1	0000 0000 0000 0000	1	None

Figure 4. Microcoded Examples

D35-D32 is to be output on D3-D0, the input from D3-D0 is output on D35-D32, and so on for the remaining nibbles. As shown in Table 3, the flip-flops for D3-D0 have to be set to 1000 and the D35-D32 inputs must be low. The CF groups and control words involved in this switching pattern are listed in Table 8.

Table 8. Control Words for an MSH/LSH Exchange

Control Flip-Flop Nibbles	CNTR Inputs to Load Flip-Flops	Control Word Loaded	Results
CF15	CNTR15-CNTR12	0111	D31-D28 → D63-D60
CF14		0110	D27-D24 → D59-D56
CF13		0101	D23-D20 → D55-D52
CF12		0100	D19-D16 → D51-D48
CF11	CNTR11-CNTR8	0011	D15-D12 → D47-D44
CF10		0010	D11-D8 → D43-D40
CF9		0001	D7-D4 → D39-D36
CF8		0000	D3-D0 → D35-D32
CF7	CNTR7-CNTR4	1111	D63-D60 → D31-D28
CF6		1110	D59-D56 → D27-D24
CF5		1101	D55-D52 → D23-D20
CF4		1100	D51-D48 → D19-D16
CF3	CNTR3-CNTR0	1011	D47-D44 → D15-D12
CF2		1010	D43-D40 → D11-D8
CF1		1001	D39-D36 → D7-D4
CF0		1000	D35-D32 → D3-D0

With this list of control words and the signals in Table 6, the 16-bit control inputs on CNTR15-CNTR0 can be arranged to load the control flip-flops in four cycles. Example 2 of Figure 4 shows the microcode instructions for loading the control words and executing the exchange.

In Example 2 bank 2 of flip-flops is being programmed. Bank 2 is selected by taking CRWRITE high and leaving CRSRCE low (see Table 4) when the control words are loaded on CNTR15-CNTR0. With $\overline{WE}$ held low, the CRCLK is used to load the four sets of control words. Once the flip-flops are loaded, data can be input on D63-D0 and the programmed pattern of output selection can be executed. A microinstruction to select real-time data inputs and bank 2 as the control source is shown as the last instruction in Example 2 of Figure 4.

The control flip-flops could also have been loaded from the data input nibbles in one CRCLK cycle. All control words to set up a switching pattern should be loaded before the bank of flip-flops is selected as control source. Table 5 shows how input nibbles from one half are mapped onto the control flip-flops of the other half. The microcode instructions to load bank 1 with the 16 control words in one cycle are presented in Example 3.

Example 3. Loading the MSH/LSH Exchange from Data Inputs

CRSRCE	CRWRITE	$\overline{WE}$	SELDMS	SELDLS	$\overline{OED15}$-$\overline{OED0}$	CRCLK
1	0	0	1	1	1111 1111 1111 1111	⌐

These control nibbles may be loaded from the - input as a 64-bit real-time input word or as two 32-bit words stored previously. To use stored control words, MSCLK and LSCLK are used to load the LSH and MSH input registers with the correct sequence of control nibbles. Whenever the flip-flops are loaded from the data inputs, all 64 bits of control data must be present when the CRCLK is used so that all control nibbles in a program are loaded simultaneously. Example 4 presents the three microcode instructions to load the MSH and LSH input registers and then to pass the registered data to flip-flop bank 2.

The control words in a program can also be read back from the flip-flops using the CNTR outputs. Four instructions are necessary to read the 64 bits in a bank of flip-flops out on CNTR16-CNTR0. $\overline{WE}$ is held high and $\overline{OEC}$ is taken low. No CRCLK signal is required. The high signal on CREAD selects bank 2 of flip-flops and CRADR1-CRADR0 select in sequence the four addresses of the 16-bit words to be read out on the CNTR outputs. Example 5 shows the four microcode instructions.

Example 4. Loading Control Flip-Flops from Input Registers

Inst. No.	CRSRCE	CRWRITE	$\overline{WE}$	SELDMS	SELDLS	$\overline{OED15}$-$\overline{OED0}$	CRCLK	MSCLK	LSCLK	Inputs Loaded
1	X	X	1	X	X	1	None	⌐	None	D63-D32
2	X	X	1	X	X	1	None	None	⌐	D31-D0
3	1	1	0	0	0	1	⌐	None	None	X

Example 5. Reading Control Settings on CNTR Outputs

Inst. No.	CREAD	$\overline{OEC}$	CRADR1	CRADR0	$\overline{WE}$	CNTR I/O Numbers 15-12	11-8	7-4	3-0
1	1	0	0	0	1	0100	0000	1100	1000
2	1	0	0	1	1	0101	0001	1101	1001
3	1	0	1	0	1	0110	0010	1110	1010
4	1	0	1	1	1	0111	0011	1111	1011

'AS8840s in a Dynamic Computer Group

The 'AS8840 performs a range of switching operations, some controlled by hard-wired control functions and others programmed to suit the application. Since it can be dynamically reprogrammed, the switch supports alternate routing schemes which require reconfigurable data paths among multiple sources and destinations.

The 'AS8840 can be used to switch data and address interconnections among multiple processors and memories in a reconfigurable architecture called a dynamic computer group. This architecture combines groups of processors and memories to form larger processor elements which can be configured to perform parallel processing. These same processing elements can be reconfigured dynamically to support alternative network or processing structures.

Figure 5 shows a dynamic computer group with four 32-bit processors and four 32-bit memories, along with the interconnecting switch network, network control and interface processor, memories, and external network I/O devices. In this sample application the processors are 'AS8832 registered ALUs with associated 'AS8835 microsequencers. The four processors P1-P4 can send data, addresses, and control signals through the 'AS8840s to memories M1-M4. Switching patterns within the group are determined by the control flip-flop settings or the hard-wired control functions of the 'AS8840s.

Another 'AS8832 serves as a network control and interface (NCI) processor. This processor sets up the configuration of the processor groups, assigns memories to processors, and loads the programs to switch data, addresses, and control signals through the 'AS8840s.

The NCI processor can load control words into the 'AS8840 flip-flop banks using either the control inputs or the data inputs. Four register clock cycles are required to load a bank of flip-flops from the control inputs CNTR15-CNTR0. Loading one bank of flip-flops from the control inputs can be done without interrupting normal switch operation since the other bank of flip-flops can control the switch during the loading.

In Figure 5 four 'AS8840s provide 32-bit data communication, and three 'AS8840s pass address and control signals between processors and memories. Each 'AS8832 can operate as a single 32-bit ALU, as two 16-bit ALUs, or as four 8-bit ALUs, executing single instructions on multiple data streams (SIMD). If the four 'AS8832s are set to operate in synchronous SIMD mode, the computer group can function as sixteen 8-bit processors, eight 16-bit processors, or four 32-bit processors. Alternatively, the ALUs and crossbars can be reconfigured into a network of processor elements performing multiple instruction/multiple data (MIMD) processing.

'AS8840s can be cascaded to switch data from up to eight 32-bit buses, which can connect eight 'AS8832 ALUs to memories or other devices. To partition each 32-bit data path symmetrically among the digital crossbars, each 'AS8840 would switch one nibble from each of the eight 32-bit buses, requiring eight crossbars to switch eight buses. Both the 'AS8832 ALUs and the 'AS8840s are fully microprogrammable so that a range of processing and switching operations can be designed to perform SIMD and MIMD parallel processing algorithms.

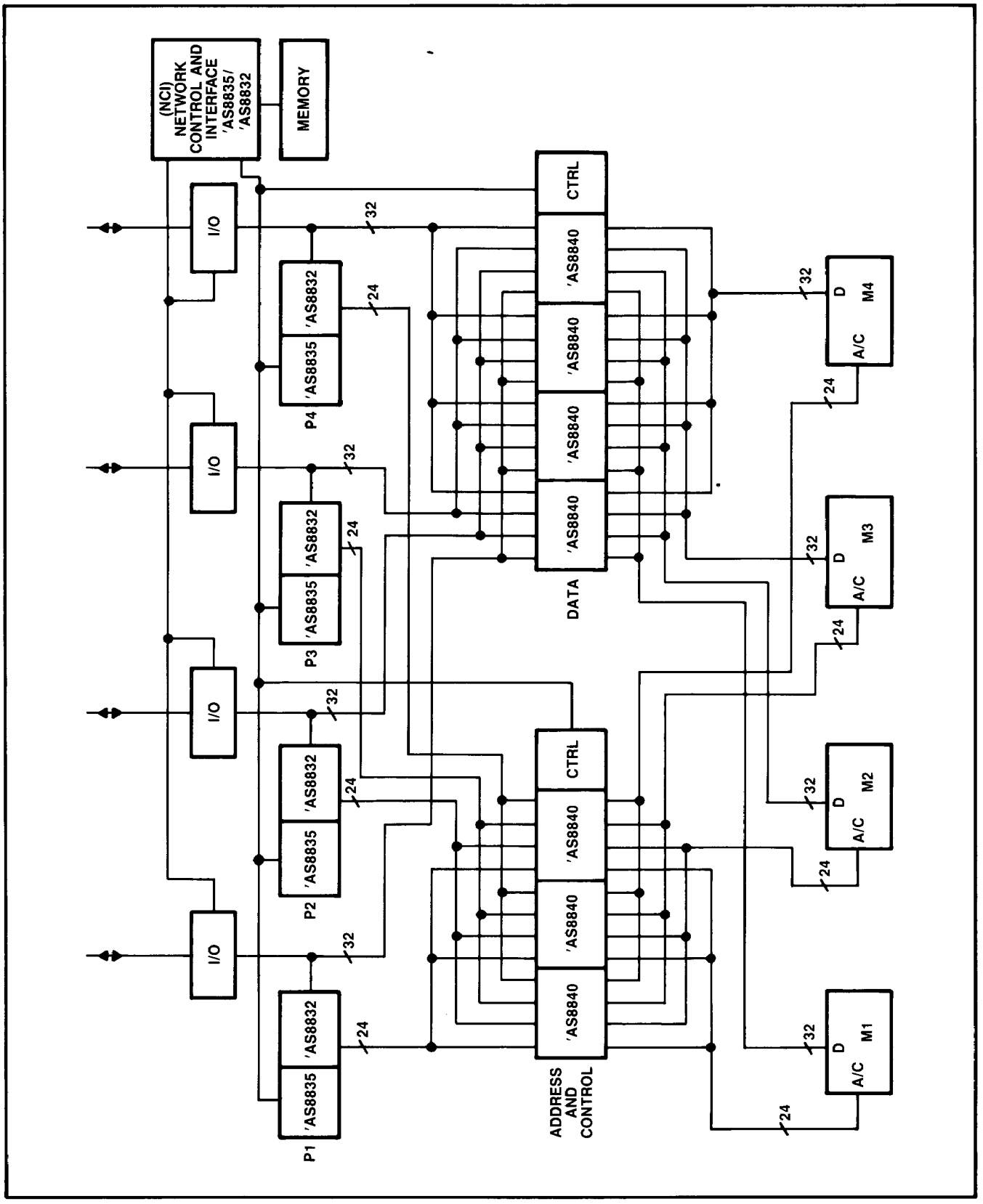

Figure 5. Dynamic Computer Group

Specifications

Table 9. Absolute Maximum Ratings Over Operating Temperature Range (unless otherwise noted)

Supply voltage, C_{CC1}	7 V
Supply voltage, V_{CC2}	3 V
Input Voltage	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

Table 10. Recommended Operating Conditions

		MIN	NOM	MAX	Unit
V_{CC1}	I/O supply voltage	4.5	5	5.5	V
V_{CC2}	STL internal logic supply voltage	1.9	2	2.1	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Table 11. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Parameter		Test Conditions		MIN	TYP	MAX	Unit
V_{IK}		V_{CC1} = 4.5 V	II = 18 mA			−1.2	V
V_{OH}		V_{CC1} = 4.5 V	I_{OH} −2.6 mA	2.4	3.2		V
V_{OL}		V_{CC1} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	
		V_{CC1} = 5.5 V	I_{OL} = 24 mA		0.35	0.5	V
I_I	I/O*	V_{CC1} = 5.5 V	V_I = 5.5 V			0.1	mA
	Others	V_{CC1} = 5.5 V	V_I = 7 V			0.1	
I_{IH}	I/O*	V_{CC1} = 5.5 V	V_I = 2.7 V			40	μA
	Others	V_{CC1} = 5.5 V	V_I = 2.7 V			20	
I_{IL}		V_{CC1} = 5.5 V	V_I = 0.4 V			−0.4	mA
I_O**		V_{CC1} = 5.5 V	V_O = 2.25 V	−30		−112	mA
I_{CC1}		V_{CC1} = 5.5 V					mA
I_{CC2}		V_{CC1} = 2.1 V					mA

*All typical values are at V_{CC} = 5 V, T_A = 25°C
**For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current
***The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS}.

Table 12. 'AS8840 Preliminary Performance Data

Data or Control Path	Typical Timing (NS)
Data in → Data out (See note 1)	20
MSCLK → Data out	25
LSCLK → Data out	25
SELDMS → Data out	23
SELDLS → Data out	23
CRCLK → Data out	35
CRSEL1-CRSEL0 → Data out	30
TP1-TP0 → Data and control out (See note 2)	25
CREAD → Control out (See note 3)	18
CRCLK → Control out	28
CRADR1-CRADR0 → Control out	25

NOTE 1: Patterns of data output on data I/Os D63-D0 are programmable and vary according to the control source selected.

NOTE 2: Output enables $\overline{\text{OED15}}$-$\overline{\text{OED0}}$ and $\overline{\text{OEC}}$ must be low when test pins are used to force outputs and I/Os high or low.

NOTE 3: Patterns of control outputs on CNTR15-CNTR0 vary according to the sequence of addresses in which the control flip-flop settings are read out.

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