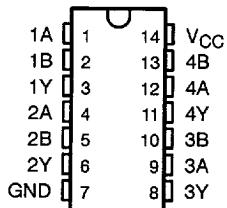


- EPIC™ (Enhanced-Performance Implanted CMOS) 2- $\mu$  Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE  
(TOP VIEW)**description**

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

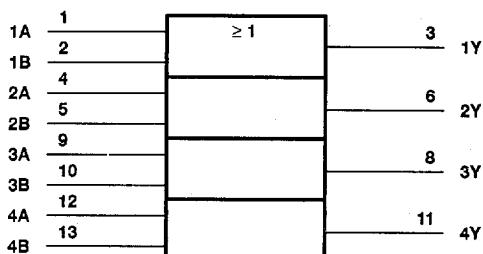
The SN74LV32 performs the Boolean functions  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

The SN74LV32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV32 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

**logic symbol†****logic diagram, each gate (positive logic)**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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# SN74LV32

## QUADRUPLE 2-INPUT POSITIVE-OR GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package .....	1.25 W
DB or PW package .....	0.5 W
Storage temperature range .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

### recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
$V_I$	Input voltage	0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		V
$I_{OH}$	High-level output current			–6	mA
$I_{OL}$	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100	ns/V	
$T_A$	Operating free-air temperature	–40	85		°C

NOTE 4: Unused or floating inputs must be held high or low.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$ <sup>‡</sup>	MIN	TYP	MAX	UNIT
$V_{OH}$	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$		3 V	2.4		
$V_{OL}$	$I_{OL} = 100 \mu\text{A}$	MIN to MAX	0.2		0.4	V
	$I_{OL} = 6 \text{ mA}$		3 V		0.4	
$I_I$	$V_I = V_{CC}$ or GND	3.6 V		±1		μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20		μA
$\Delta I_{CC}$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at $V_{CC}$ or GND	One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND			500	μA
$C_I$	$V_I = V_{CC}$ or GND	3.3 V		2.5		pF

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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**SN74LV32**  
**QUADRUPLE 2-INPUT POSITIVE-OR GATE**

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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Note 5)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y		8	17		22	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

**operating characteristics,  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS			TYP	UNIT
	$C_L = 50 \text{ pF}$	$f = 10 \text{ MHz}$			
$C_{pd}$	Power dissipation capacitance per gate			23	pF

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