DS3F Device
DS3 Framer
TXC-03401B

DATA SHEET

FEATURES

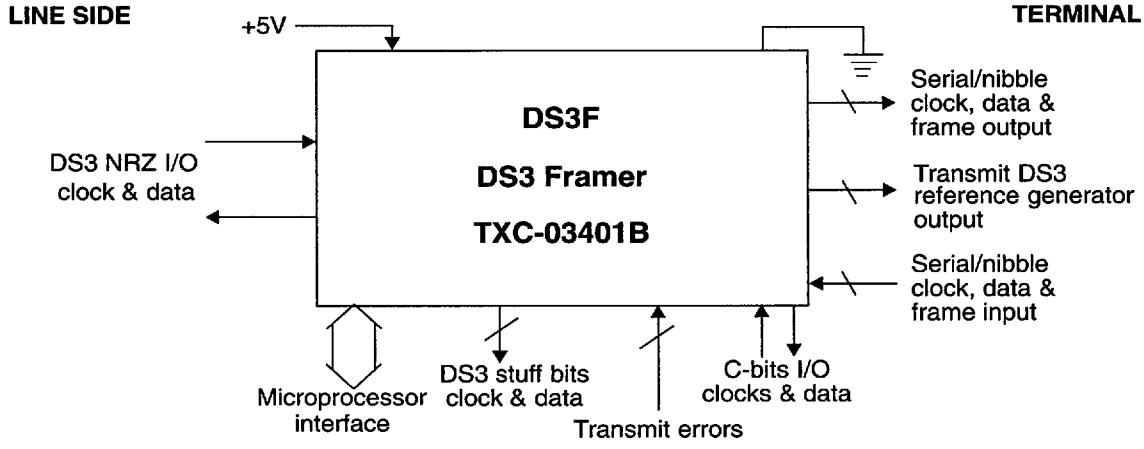
- DS3 payload access, bit-serial or nibble-parallel
- C-bit parity or M13 operating mode
- C-bit interface (13 C-bits in, 14 out)
- Detect and generate DS3 AIS, and idle signals
- Transmit reference generator for serial operation
- Transmit and receive Far End Alarm and Control (FEAC) with double word capability and automatic transmission
- Maskable hardware interrupt for eight alarms
- Transmit single errors: framing, FEBE, C-bit parity, and P-bit parity
- FEBE, C-bit, and P-bit performance counters
- Counters for F-bit and M-bit errors
- Counter for coding violations and excessive zeros
- Transmit-to-Receive and Receive-to-Transmit loopbacks
- Outputs can be set to high-impedance state
- Selectable mode for TXC-03401 emulation
- Single +5 volt power supply
- 68-pin plastic leaded chip carrier

DESCRIPTION

The DS3F is designed for DS3 framer applications in which broadband payloads are mapped into the 44.736 Mbit/s DS3 frame format. Although the C-bit parity format is recommended, the DS3F can also operate in the M13 mode. In the C-bit parity format, the DS3F provides a separate interface for selected C-bits. The DS3F also provides for transmitting and receiving the FEAC channel and Blue code AIS conditions, and generates and detects DS3 AIS, DS3 idle, P-bit parity and C-bit parity. In addition, performance counters are provided, as well as the ability to generate single framing, FEBE, C-bit parity and P-bit parity errors. The device also provides X-bit inversion, receive loop timing and indications for FEAC idle channel, FEAC word stack overflow and Severely Errored Frame. The payload interface is selectable through software as either a bit-serial or nibble-parallel format.

APPLICATIONS

- Subrate multiplexing
- Wideband data or video transport
- DS3 monitor and test
- Channel extenders
- DS3 test sets



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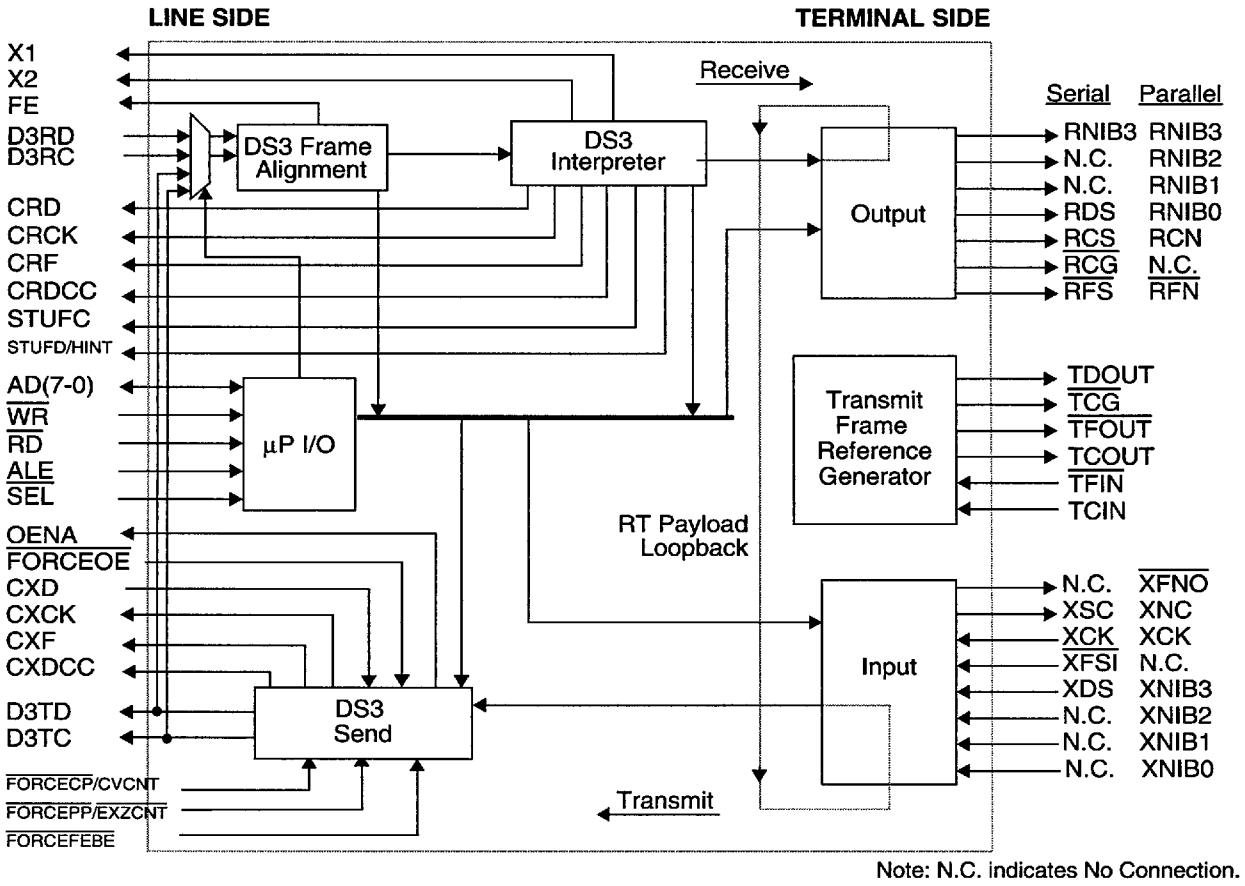
BLOCK DIAGRAM



Note: N.C. indicates No Connection.

Figure 1. DS3F TXC-03401B Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows the block diagram of the DS3F device.

The DS3F is designed to operate in both "Normal" (N) and "Extended-features" (E) modes of operation. In the Normal mode, the device emulates the TranSwitch TXC-03401 DS3F device. In the Extended-features mode, all the additional capabilities described in this Data Sheet are available. Technical Bulletin TB-511 describes the differences between the TXC-03401 and the TXC-03401B (document number TXC-03401-TB1). Either mode of operation can be selected by setting control bit EMODE in the memory map. Two input pins (FORCECP/CVCNT and FORCEPP/EXZCNT) and one output pin (STUFD/HINT) can change their functions according to the mode selected (N/E). Memory map addresses above 07H are effective only in the Extended-features mode.

The DS3F receives a line side DS3 data signal (D3RD) and a clock signal (D3RC) from a line interface device such as the TranSwitch ART/ARTE VLSI device (TXC-02020/02021) or DS3LIM-SN module (TXC-20153D or TXC-20153G). The DS3 Frame Alignment Block performs DS3 frame alignment that will not lock to a false framing pattern. There are internal 8-bit F- and M-bit error counters included in the Extended-features mode of the framer to monitor errors. The DS3F also monitors the signal and the input clock for loss of signal (LOS), out of frame (OOF), and loss of clock (LOC). A framing error (FE) output is provided to indicate when any of the 28 framing bits in the DS3 signal are in error.

The DS3 Interpreter Block performs P-bit and C-bit parity detection and error counting, receive AIS and idle pattern detection, far end block error (FEBE) detection and error counting, far end alarm and control (FEAC) code word detection of up to 4 different types, C-bit reception and X-bit reception. Serial interfaces are provided for the received X-bits and for 14 of the 21 C-bits. In the Extended-features mode, groups of the C-bits can be set by writing to the memory map. The receive C-bit interface consists of a serial data signal (CRD), clock signal (CRCK), framing pulse (CRF), and a data communication link clock signal (CRDCC). The clock signal (CRCK) is gapped and is available only for clocking out C-bits C2 through C6, and C13 through C21. The CRDCC clock signal is present only for C-bits C13, C14 and C15, which are assigned as a data communication channel when operating in the C-bit parity mode. In the Extended-features mode, the timing of the CRDCC receive clock edges can be reversed by setting a control bit in the memory map.

When operating in the M13 mode, an interface (output pin STUFD) that indicates the state of the stuff opportunity bit during each of the seven DS3 subframes and a clock signal (STUFC) are also provided. The Stuff Data Status (STUFD) output pin is shared with the Hardware Interrupt (HINT) pin for the Extended-features mode. The Hardware Interrupt output is used to the inform the microprocessor that a severe alarm condition has occurred. The polarity of the Hardware Interrupt output is selectable by a control bit to meet the requirements of the microprocessor's interrupt input pin. When a hardware interrupt does occur, it can be isolated to one of up to up to eight different latched alarm types if they are enabled in the memory map.

The Output Block provides a bit-serial or a nibble-parallel interface for C-bit parity mode. The M13 mode uses the bit-serial interface only. Note that since the sum of the payload and C-bits in a DS3 frame is not evenly divisible by four, M13 nibble mode operation is not feasible. The interface type is selected by writing to a control bit in the memory map (SER), and is common to the DS3F receive and transmit circuitry. The signals provided for the bit-serial interface consist of a data signal (RDS), a clock signal (RCS), a receive clock gap signal ($\overline{\text{RCG}}$) and framing pulse ($\overline{\text{RFS}}$). The nibble-parallel interface consists of the nibble data signal (RNIB3 through RNIB0), a clock out signal (RCN), and a framing pulse output ($\overline{\text{RFN}}$). The RNIB3 bit corresponds to the first bit received in a four-bit serial bit stream segment.

In the transmit direction, the Input Block provides either a bit-serial or nibble-parallel interface. The bit-serial interface consists of a data signal (XDS), clock signals (XCK and optionally XSC), and a framing pulse ($\overline{\text{XFSI}}$). The nibble-parallel interface consists of the nibble data (XNIB3 through XNIB0), a clock out signal (XCK), a framing pulse ($\overline{\text{XFNO}}$), and a nibble clock signal (XNC). The XNIB3 bit corresponds to the first bit transmitted.

The DS3 Send Block performs P-bit and C-bit parity generation, AIS and idle pattern generation, far end alarm and control (single or double FEAC word) transmission, X-bit insertion, and C-bit insertion. For C-bit Parity mode, the C-bits may be generated internally (such as C-bit parity), written by the microprocessor (such as the FEAC channel), or provided from the external C-bit interface. The transmit C-bit interface consists of a data input signal (CXD), a clock signal (CXCK), a framing pulse (CXF) and a data communication link clock (CXDCC). For M13 mode, the C-bits are input from the terminal side's bit-serial interface. The DS3 transmit line side interface consists of the data signal (D3TD) and a clock signal (D3TC).

DS3F transmit-to-receive (TR) loopback is controlled by setting a bit in the memory map (3LOOP). The entire device is used when loopback is in effect, but the line side input data and clock are blocked (by the gate preceding the DS3 Frame Alignment Block shown in Figure 1). In the Extended-features mode of operation, a receive-to-transmit payload (RTP) loopback is also available by use of control bit RTPLOOP.

The capability to generate and transmit single overhead bit errors is also provided. External interfaces are provided for transmitting a far end block error (FORCEFEBE), a P-bit parity error (FORCEPP), a C-bit parity error (FORCECP) and an overhead bit error (FORCEOE). The FORCEOE signal is used in conjunction with the enable signal (OENA) for introducing an overhead bit error in the next 85-bit segment of the DS3 frame. When the Extended-features mode (EMODE), Coding Violation Enable (CVEN) and Excessive Zeros Enable (EXZEN) control bits in the memory map are set to 1, the Coding Violations Count (CVCNT) function and Excessive Zeros Count (EXZCNT) functions pin replace the FORCECP and FORCEPP functions, respectively. The purpose of these pins is to utilize the DS3F's 16-bit counter CVEXZ to count coding violation and/or excessive zeros events. Indications of these events are provided to the DS3F by TranSwitch's ART or ARTE devices (TXC-02020/02021). The ART's CV output pin indicates both coding violations and excessive zeros. Therefore, only the CVCNT input pin to the DS3F is required to count both types of event. When the ARTE is used in conjunction with the DS3F, there are separate CV and EXZ inputs available to the DS3F, which can be or-gated together in the DS3F's 16-bit counter, if required. The DS3F has an internal 16-bit shadow counter incorporated into its counter design. This prevents CV or EXZ counts being lost during a read cycle.

The Transmit Frame Reference Generator Block provides reference timing for bit-serial operation. This block accepts an external 44.736MHz clock signal (TCIN) and derives a clock signal (TCOUT), a framing pulse (TFOUT), a clock gap signal (TCG) and a data signal (TDOUT). The DS3 data signal consists of framing bits and zeros elsewhere. An optional input framing pulse (TFIN) is also provided, but is not required for normal operation.

The DS3F microprocessor bus interface consists of eight bidirectional data and address leads (AD0-AD7), along with other microprocessor control leads. The microprocessor bus is used to write control information and to read status information and alarms. When operating in the Extended-features mode the DS3F memory map contains twenty-one effective addresses (00H-14H), compared with eight (00H-07H) in the Normal mode.

When the DS3F is operating in the Extended-features mode, its many additional features may be activated via control bits in the memory map. These features include: ability to tri-state all output ports, X-bit inversion, receive loop timing, receive and transmit Blue Code AIS conditions, FEAC Idle Channel Indication, a receive FEAC FIFO stack overflow bit, a Severely Errored Frame indication, and double FEAC word handling.

PIN DIAGRAM

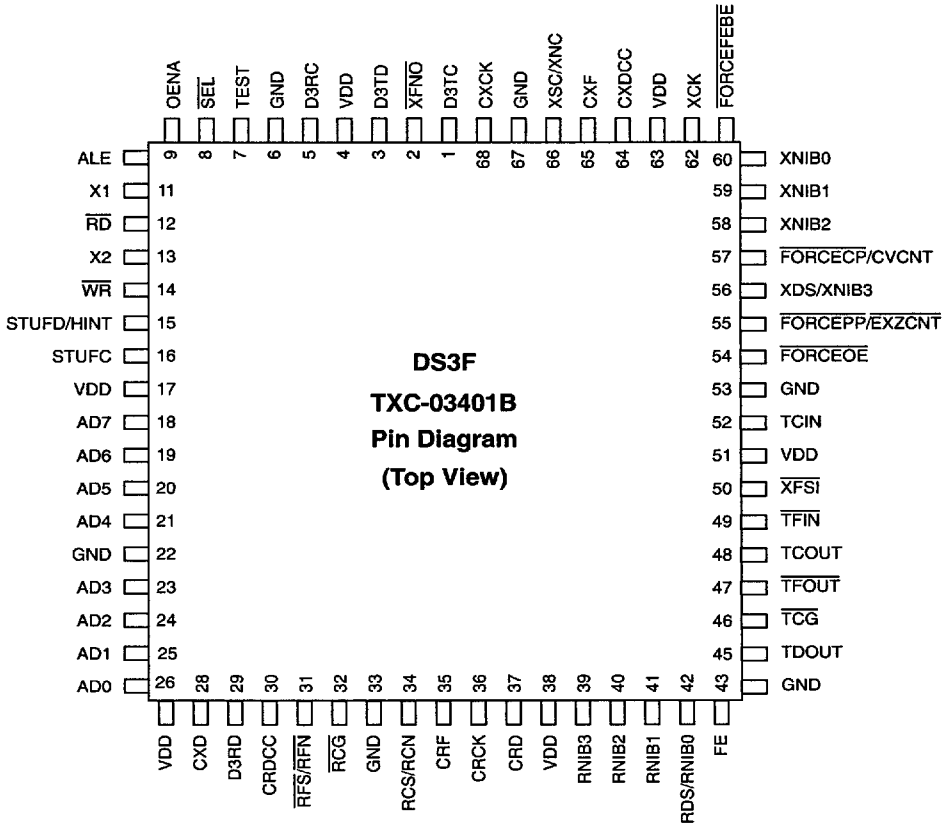


Figure 2. DS3F TXC-03401B Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	4, 17, 27 38, 51, 63	P		**VDD:** +5 volt supply voltage, ± 5%
GND	6, 22, 33 44, 53, 67	P		**Ground:** 0 volts reference.

*Note: I = Input; O = Output; P = Power

DS3 RECEIVE LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type*	Name/Function
D3RC	5	I	CMOS	**DS3 Receive Clock:** A 44.736 MHz clock used for clocking in receive data, and as the time base for the DS3F receiver. Line side serial data is clocked into the DS3F on positive transitions of the clock.
D3RD	29	I	TTL	**DS3 Receive Data:** DS3 line side serial receive data.

DS3 TRANSMIT LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
D3TC	1	O	CMOS4mA	**DS3 Transmit Clock:** A 44.736 MHz clock that is derived from the transmit clock (XCK) signal and is used for clocking out the line side DS3 data signal. Data (D3TD) is clocked out on positive transitions of the clock.
D3TD	3	O	CMOS4mA	**DS3 Transmit Data:** DS3 line side serial transmit data.

RECEIVE TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RFS}}/\overline{\text{RFN}}$	31	O	CMOS4mA	**Receive Framing Pulse Serial/Nibble Interface:** The framing pulse is active low for one clock cycle (RCS/RCN), and is synchronous with the first bit 1 in the DS3 frame. For the nibble interface, the framing pulse is synchronous with nibble 1175.
RCS/RCN	34	O	CMOS4mA	**Receive Clock Serial/Nibble Interface:** Clock used for clocking out the terminal side receive serial and nibble data. This clock is derived from the line side clock (D3RC). Data is clocked out of the DS3F on negative transitions of this clock.
RNIB3 RNIB2 RNIB1 RDS/RNIB0	39 40 41 42	O	TTL4mA	**Receive Nibble/Serial Interface:** Nibble data is clocked out on positive transitions of the nibble clock (RCN). There are 1176 nibbles provided each frame. The data and clock are stretched to accommodate the 56 individual overhead bits (first bit in the 85-bit group), which are not provided at the interface. The first bit received in a nibble is present on RNIB3. The nibble interface is operational in the C-bit parity operating mode only. Serial data (RDS) consists of all the bits in the frame (including the states of the overhead bits), and is operational in either operating mode, M13 or C-bit parity. Serial data is clocked out on negative transitions of the receive clock (RCS). For serial data, a gapped clock signal is generated by the receive circuitry and provided on the RNIB3 pin when control bits SER and RGCEN are both set to 1.

*See Input, Output and I/O Parameters section for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{RCG}$	32	O	CMOS4mA	**Receive Clock Gap Signal:** The active low gap signal is synchronous with each overhead bit in the serial DS3 frame (first bit in the 85-bit group).

TRANSMIT TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{XFNO}$	2	O	TTL4mA	**Transmit Nibble Interface Framing Pulse:** An active low, one nibble clock cycle wide (XNC) pulse that occurs during the second nibble time.
$\overline{XFSI}$	50	I	TTLp	**Serial Data Transmit Framing Pulse:** A framing pulse whose leading edge must be synchronous with bit 1 in the transmit serial data DS3 frame. The DS3F rewrites the 56 overhead bits based on the location of the transmit framing pulse. If this signal is held low for a duration greater than 1 frame, then all register bit positions at Addresses 02H-04H, 05H bit 6 and 08H-14H (except 10H bit 6) will be reset to 0 until the pin is taken high. The $\overline{XFSI}$ pulse must not be applied while control bit RTPLOOP is set to 1.
XDS/XNIB3 XNIB2 XNIB1 XNIB0	56 58 59 60	I	TTL	**Transmit Nibble/Serial Interface:** Nibble data is clocked in on positive transitions of the nibble clock (XNC). There are 1176 nibbles in each frame. The clock is stretched to accommodate the 56 overhead bits which are not required at the interface. The DS3F inserts the X, F, C, P, and M overhead bits into the transmitted frame based on the framing pulse $\overline{XFNO}$. The first bit transmitted in a nibble is present on XNIB3. The nibble interface is operational in the C-bit parity mode only. The serial data should consist of all the bits in the frame (4760 bits). The DS3F rewrites the 56 overhead bits in the frame based on the location of the framing pulse $\overline{XFSI}$, when operating in the C-bit parity mode. In the M13 operating mode, the 21 C-bits are treated as user data, while the other overhead bits (X, F, P, and M bits) are written into the DS3 frame by the DS3F. Serial data is clocked into the DS3F on positive transitions of the transmit clock (XCK).
XCK	62	I	CMOS	**Transmit Clock:** Provides the time base for the transmitter in the DS3F. In order to meet cross-connect objectives, the clock must operate at 44.736 Mbit/s with a stability of ±20 ppm and a duty cycle of (50±10)%. If XCK fails, the DS3F uses the D3RC receive clock in its place.

Symbol	Pin No.	I/O/P	Type	Name/Function
XSC/XNC	66	O	CMOS4mA	**Transmit Nibble/Serial Clock:** Clock signal derived from the transmit clock (XCK). For nibble data, this clock (XNC) is stretched in order to accommodate the 56 overhead bit positions which are not required by the external terminal circuitry for the nibble interface (XNIBn). For serial data, a gapped clock signal (XSC) is generated and provided on this pin when control bits SER and TGCEN are both set to 1. This signal is synchronous with bit 1 in each 85-bit group (56 overhead bits) in the DS3 frame.

TRANSMIT REFERENCE GENERATOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TDOUT	45	O	TTL4mA	**Transmit Reference Generator Data Output:** DS3 frames are provided on this output that contain either all zeros or all ones. The number of frames with ones is 7 of every 18 frames. The pattern of the ones is one frame of every three for 15 frames and two of the last 3 of the 18-frame group; this completes the 7 of 18 pattern. The purpose of this pattern is to ease the requirement to provide an all-ones and all-zeros C-bit pattern to insure a DS2 frequency that is very nearly equal to its specified value.
$\overline{\text{TCG}}$	46	O	TTL4mA	**Transmit Reference Generator Clock Gap Signal:** An active low, one clock cycle wide (TCOUT) signal that is synchronous with bit 1 in each 85-bit group (56 overhead bits) in the DS3 frame.
$\overline{\text{TFOUT}}$	47	O	TTL4mA	**Transmit Reference Generator Framing Pulse:** An active low, one clock cycle wide (TCOUT) pulse that is synchronous with bit 1 in the DS3 frame. May be used as the serial data transmit framing pulse ($\overline{\text{XFSI}}$) if properly delayed such that $\overline{\text{XFSI}}$ is aligned with an overhead-bit clock cycle.
TCOUT	48	O	CMOS4mA	**Transmit Reference Generator Clock Out:** Clock signal that is derived from the transmit reference generator clock input (TCIN). Provides a time base for multiplexing an external payload into the serial signal TDOUT provided by the reference generator. May be used as the transmit input clock (XCK) in the serial mode. Transmit reference generator signals are clocked out on positive transitions of this clock.
TCIN	52	I	TTL	**Transmit Reference Generator Clock In:** Provides a time base for generating the various signals in the DS3F transmit reference generator. In order to meet DS3 cross-connect objectives, this clock must operate at 44.736 Mbit/s with a stability of ±20 ppm and a duty cycle of (50±10)%.

RECEIVE C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CRDCC	30	O	TTL4mA	**C-Bit Receive Data Link Clock:** A gapped clock provided for clocking the three data link bits (C13, C14, and C15) into external circuitry from the serial data (CRD). The rising edge of CRDCC indicates when valid data is available. In Extended mode, control bits are available to convert the three cycles into a single envelope pulse and/or to invert the signal's polarity (see Figure 10).
CRF	35	O	TTL4mA	**C-Bit Receive Framing Pulse:** Provides a time base reference for clocking in the C-bits in a DS3 frame.
CRCK	36	O	TTL4mA	**C-Bit Receive Clock:** A gapped clock which clocks C-bit data out of the DS3F. The falling edge of CRCK indicates when valid data is available.
CRD	37	O	TTL4mA	**C-Bit Receive Data:** Serial interface for receiving the following C-bits in the C-bit parity mode: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. Availability of data is indicated by the clock signals CRDCC and CRCK, described above.

TRANSMIT C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CXD	28	I	TTL	**C-Bit Transmit Data:** Serial interface for transmitting the following C-bits in the C-bit parity mode: C2, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. C-bit data is clocked into the DS3F on positive transitions of the C-bit gapped clock (CXCK). A C-bit must be transmitted as a one if not used.
CXDCC	64	O	TTL4mA	**C-Bit Transmit Data Link Clock:** A gapped clock provided for clocking the three data link bits (C13, C14, and C15). In Extended mode, a control bit is available to convert the three cycles into a single envelope pulse (see Figure 9).
CXF	65	O	TTL4mA	**C-Bit Transmit Framing Pulse:** Identifies the location of the first C-bit in the DS3 frame.
CXCK	68	O	TTL4mA	**C-Bit Transmit Clock:** A gapped clock which clocks the external C-bit serial data into the DS3F on positive transitions.

OTHER SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TEST	7	I	TTLp	**TranSwitch Test Pin:** Leave open.
OENA	9	O	TTL4mA	**Overhead Enable:** An active high signal that enables an overhead error to be introduced into the overhead bit in the next 85th group by placing a low on the $\overline{\text{FORCEOE}}$ lead.
X1	11	O	TTL4mA	**DS3 Received X-Bit 1:** An output indication of the state of the first X-bit received in the DS3 frame (bit 1). The indication is active until the next X1 state is detected.
X2	13	O	TTL4mA	**DS3 Received X-Bit 2:** An output indication of the state of the second X-bit received in the DS3 frame (bit 680). The indication is active until the next X2 state is detected.
STUFD/HINT	15	O	TTL4mA	**Stuff Data Status / Hardware Interrupt:** In the Normal mode of operation (EMODE=0), this pin performs the Stuff Data Status function. This output pin provides an indication of the state of the stuff opportunity bit from the receive DS3 frame when operating in the M13 mode. For an M13 DS3 formatted signal, the first stuff opportunity bit occurs in the first bit after F4 (last 85-bit group) in subframe 1, and the last stuff opportunity bit in the frame occurs in the seventh bit after F4 (last 85-bit group) in subframe 7. In the Extended-features mode of operation (EMODE=1), this output pin can be used (if HINTEN=1) to perform the Hardware Interrupt function. It may be used as input to the interrupt pin of the microprocessor. When at least one of the eight interrupt enable mask bits (Address 11H, bits 7-0) is 1, occurrence of a corresponding alarm condition causes the pin to go high. This pin is used to inform the microprocessor that a severe alarm condition has occurred. The Hardware Interrupt signal may be changed to active low by setting control bit HINTINV to 1.
STUFC	16	O	TTL4mA	**Stuff Clock:** Provided for clocking out the stuff opportunity bit state. The positive transition occurs at the start of the second F-bit in a subframe and the negative transition occurs at the end of the fifth 85-bit group.
FE	43	O	TTL4mA	**Framing Error Indication:** The FE pin will go high for every F-bit framing error. It stays high for a period of 1.9µs (85 clock periods). During an Out of Frame condition the FE pin is held low.
$\overline{\text{TFIN}}$	49	I	TTLp	**Transmit Framing Input:** An optional active low input signal which resets the counters of the Transmit Frame Reference Generator block to zero and holds the output signals of the block to their corresponding states.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{FORCEOE}}$	54	I	TTLp	**Force DS3 Overhead Bit Error:** An active low signal used in conjunction with the overhead enable signal (OENA) for introducing an overhead bit error in the next transmitted 85-bit group.
$\overline{\text{FORCEPP}}$/ $\overline{\text{EXZCNT}}$	55	I	TTLp	**Force P-Bit Parity Error / Excessive Zeros Count:** In the Normal mode of operation (EMODE=0), this pin performs the Force DS3 P-Bit Parity Error function. An active low signal generates and transmits a P-bit error by inverting both P-bits. If an active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame. In the Extended-features mode of operation (EMODE=1), this pin performs the Excessive Zeros Count function when EXZEN=1. An internal 16-bit counter, CVEXZ at Addresses 12H and 13H, is incremented when the pin is low during the rising edge of D3RC. This pin is intended to be driven by the $\overline{\text{EXZ}}$ Excessive Zeros output pin of the TranSwitch TXC-02021 ARTE device.
$\overline{\text{FORCECP}}$/ CVCNT	57	I	TTLp	**Force C-Bit Parity Error / Coding Violation Count:** In the Normal mode of operation (EMODE=0), this pin performs the Force DS3 C-Bit Parity Error function. An active low signal generates and transmits a C-bit parity error when operating in the C-bit parity mode. The error is transmitted by inverting C7, C8 and C9 (C-bit parity value) in subframe 3. If the active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame. In the Extended-features mode of operation (EMODE=1), this pin performs the performs the Coding Violation Count function when CVEN=1. An internal 16-bit counter, CVEXZ at Addresses 12H and 13H, is incremented when the pin is high during the rising edge of D3RC. This pin is intended to be driven by the CV Coding Violation / Excessive Zeros output pin of the TranSwitch TXC-02020 ART device or the CV Coding Violation output pin of the TranSwitch TXC-02021 ARTE device.
$\overline{\text{FORCEFEBE}}$	61	I	TTLp	**Force FEBE Error:** An active low signal generates and transmits a far end block error (FEBE) when operating in the C-bit parity mode. If the active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{SEL}$	8	I	TTL	**Microprocessor Select:** A low enables the microprocessor to access the DS3F memory map for control, status and alarm information.
ALE	10	I	TTL	**Address Latch Enable:** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle on the falling edge.
$\overline{RD}$	12	I	TTL	**Read:** An active low signal generated by the microprocessor for reading the registers which reside in the DS3F memory map. The DS3F memory I/O is selected by placing a low on the select lead.
$\overline{WR}$	14	I	TTL	**Write:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The DS3F memory I/O is selected by placing a low on the select lead.
AD(7-4) AD(3-0)	18-21 23-26	I/O	TTL8mA	**Address/Data Bus:** These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the DS3F memory map.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	+6.0	V
DC input voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Operating junction temperature	T_J		150	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		40	42	°C/W	0 ft/min linear airflow

RECOMMENDED OPERATING CONDITIONS AND POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
T_A, ambient operating temperature	-40		85	°C	0 ft/min linear airflow
V_{DD}, supply voltage	4.75	5.0	5.25	V	
I_{DD}, supply current			150	mA	
P_{DD}, supply power			790	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			0.2	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has an internal pull-up resistor.

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}		1.4		ns	$C_{LOAD} = 15$ pF
t_{FALL}		2.7		ns	$C_{LOAD} = 15$ pF

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}		1.9		ns	C_{LOAD} = 15 pF
t_{FALL}		2.0		ns	C_{LOAD} = 15 pF

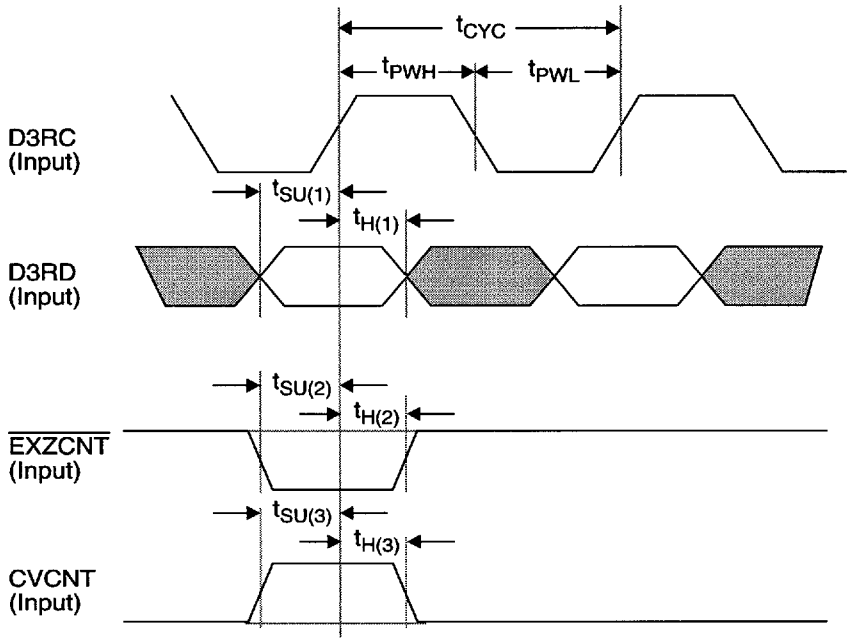
Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}		1.3		ns	C_{LOAD} = 25 pF
t_{FALL}		2.5		ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

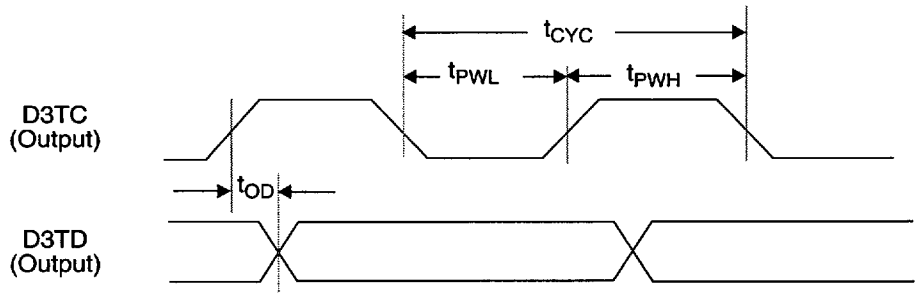
Detailed timing diagrams for the DS3F are illustrated in Figures 3 through 16, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 3. Line Side DS3 Receive Input Timing



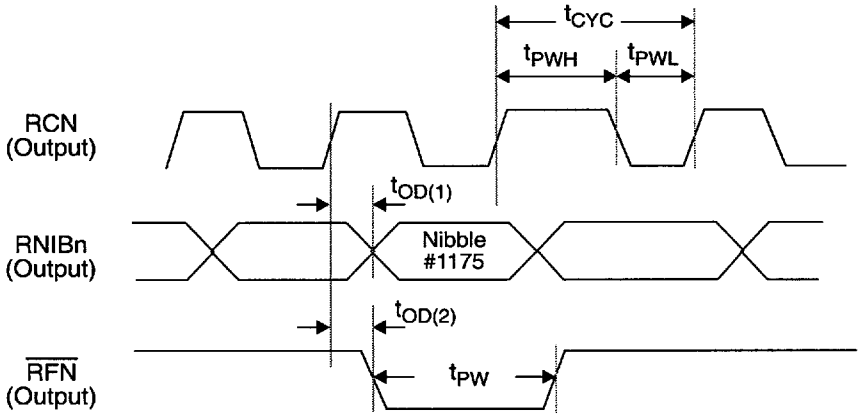
Parameter	Symbol	Min	Typ	Max	Unit
D3RC clock period	t_{CYC}	20	22.35		ns
D3RC high time	t_{PWH}	8			ns
D3RC low time	t_{PWL}	8			ns
D3RC duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
D3RD set-up time to D3RC↑	$t_{SU(1)}$	4			ns
D3RD hold time after D3RC↑	$t_{H(1)}$	6			ns
$\overline{\text{EXZCNT}}$ set-up time to D3RC↑	$t_{SU(2)}$	4			ns
$\overline{\text{EXZCNT}}$ hold time after D3RC↑	$t_{H(2)}$	6			ns
CVCNT set-up time to D3RC↑	$t_{SU(3)}$	4			ns
CVCNT hold time after D3RC↑	$t_{H(3)}$	6			ns

Figure 4. Line Side DS3 Transmit Output Timing



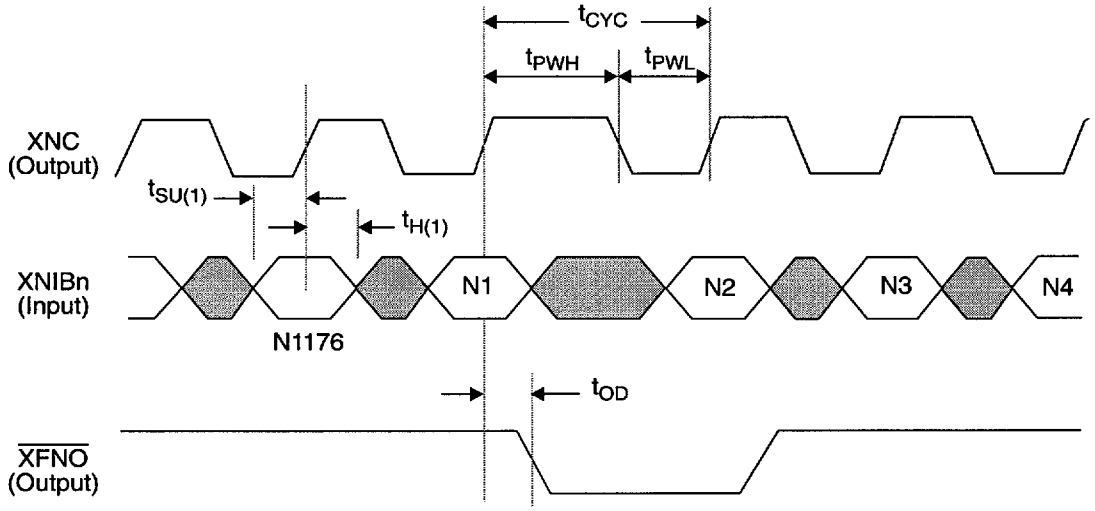
Parameter	Symbol	Min	Typ	Max	Unit
D3TC clock period	t_{CYC}	20	22.35		ns
D3TC high time	t_{PWH}	8			ns
D3TC low time	t_{PWL}	8			ns
D3TD output delay after D3TC↑	t_{OD}	3		12	ns

Figure 5. Terminal Side Receive Nibble Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
RCN clock period	t_{CYC}	89	90.5	111	ns
RCN high time	t_{PWH}	40			ns
RCN low time	t_{PWL}	40			ns
RNIBn delay after RCN ↑	$t_{OD(1)}$	20	23	26	ns
$\overline{RFN}$ delay after RCN ↑	$t_{OD(2)}$	20	23	26	ns
$\overline{RFN}$ pulse width	t_{PW}	89	1 t_{CYC}	93	ns

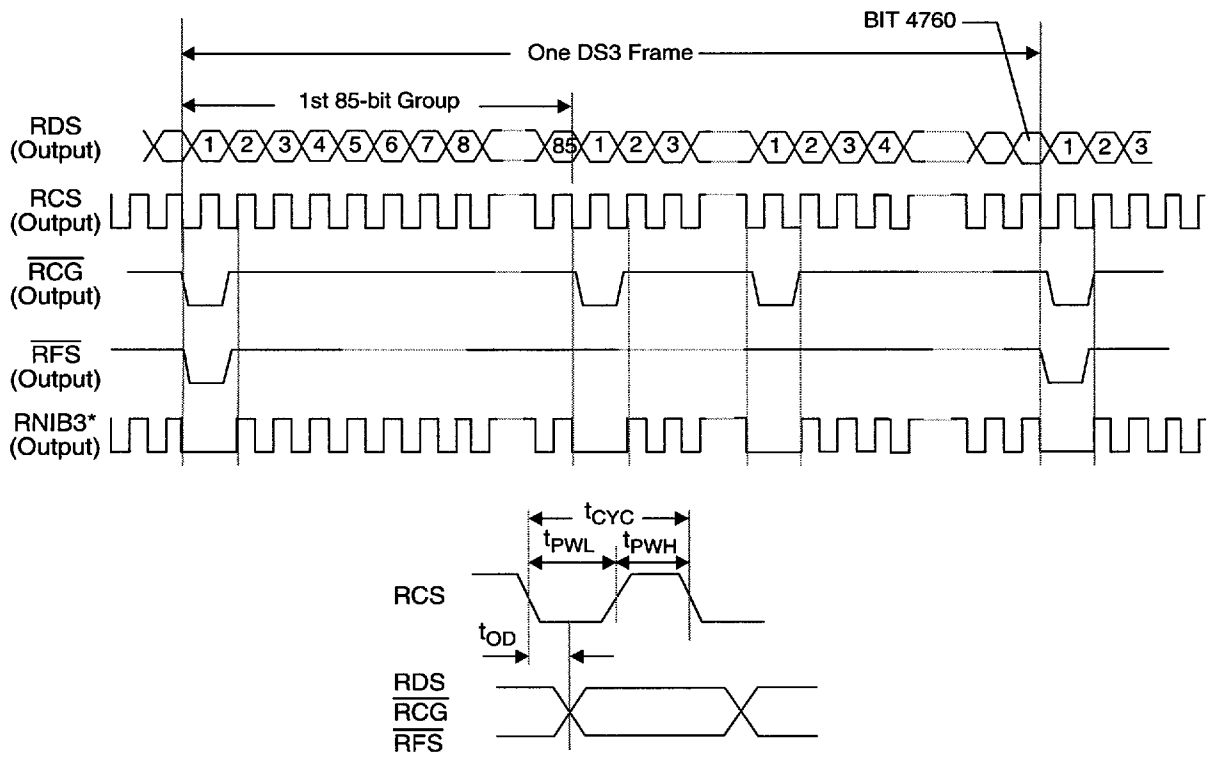
Figure 6. Terminal Side Transmit Nibble Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
XNC clock cycle	t_{CYC}	89.0	90.5	111	ns
XNC high time	t_{PWH}	40		63	ns
XNC low time	t_{PWL}	40		50	ns
XNIBn set-up time to XNC↑	$t_{SU(1)}$	26			ns
XNIBn hold time after XNC↑	$t_{H(1)}$	-14			ns
$\overline{\text{XFNO}}$ output delay after XNC↑	t_{OD}	0	2	8	ns

Note: XNIB data input is latched at the midpoint of XNC low.

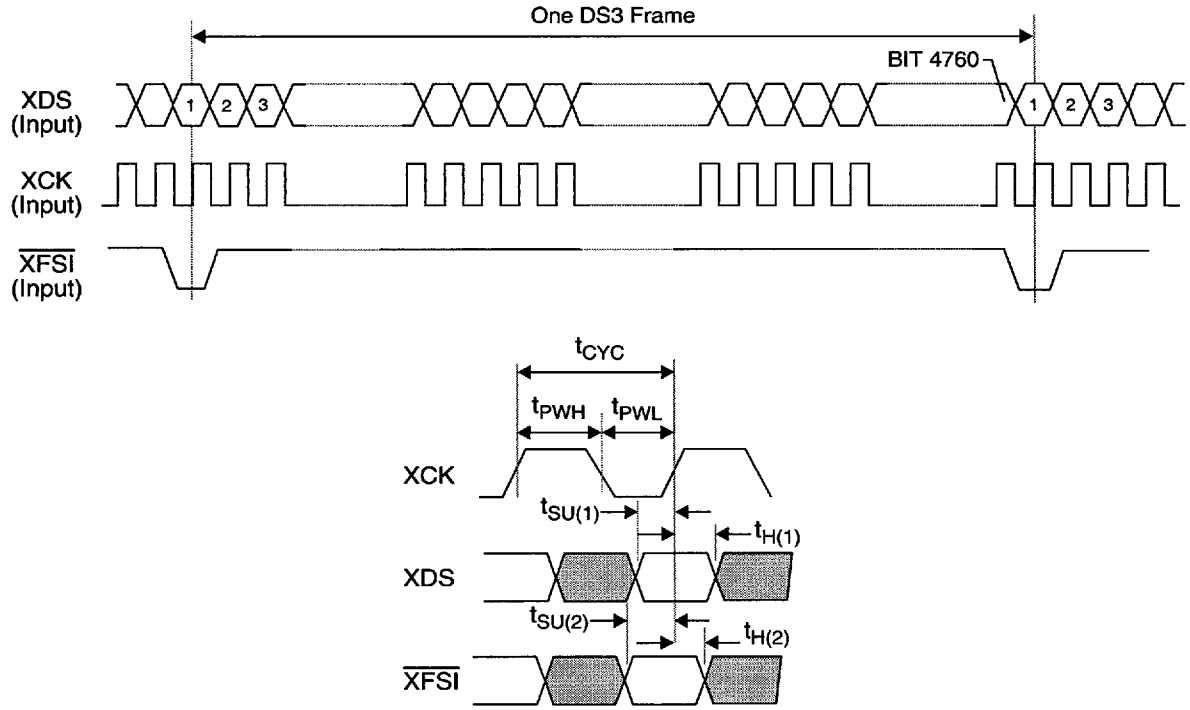
Figure 7. Terminal Side Receive Serial Output Timing



* Note: Waveform generated when control bits SER and RGCEN are both set to 1.

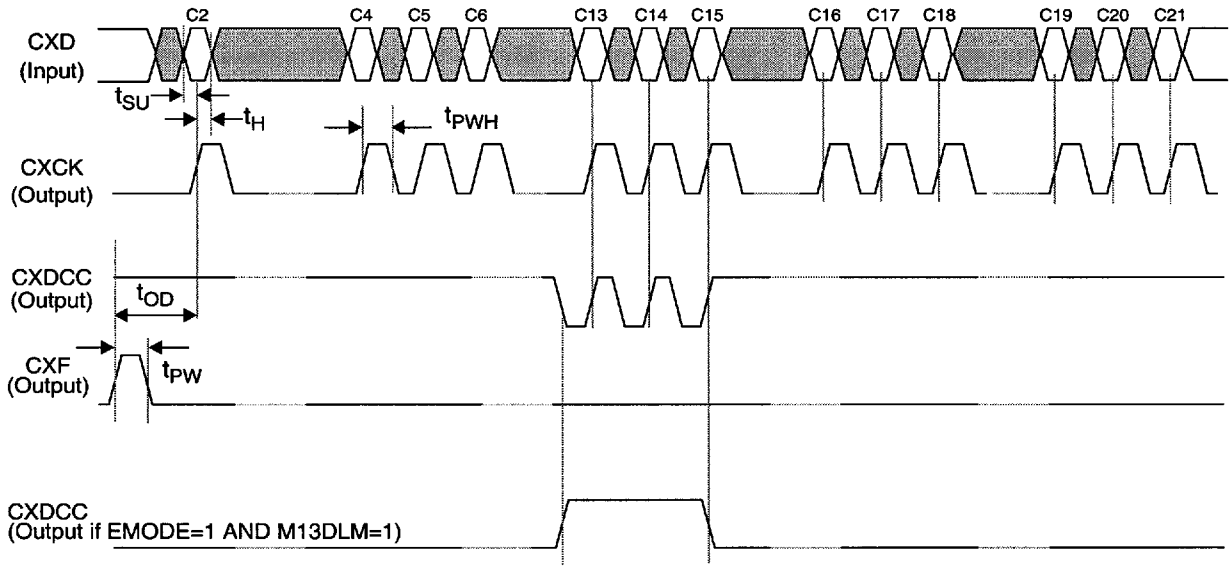
Parameter	Symbol	Min	Typ	Max	Unit
RCS clock period	t_{CYC}	20	22.35		ns
RCS high time	t_{PWH}	8			ns
RCS low time	t_{PWL}	8			ns
RDS, $\overline{RCG}$, $\overline{RFS}$ output delay after RCS↓	t_{OD}	0	2.5	5	ns

Figure 8. Terminal Side Transmit Serial Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
XCK clock period	t_{CYC}	20	22.35		ns
XCK high time	t_{PWH}	8			ns
XCK low time	t_{PWL}	8			ns
XDS set-up time to XCK↑	$t_{SU(1)}$	0			ns
XDS hold time after XCK↑	$t_{H(1)}$	8			ns
$\overline{\text{XFSI}}$ set-up time to XCK↑	$t_{SU(2)}$	2			ns
$\overline{\text{XFSI}}$ hold time after XCK↑	$t_{H(2)}$	5			ns

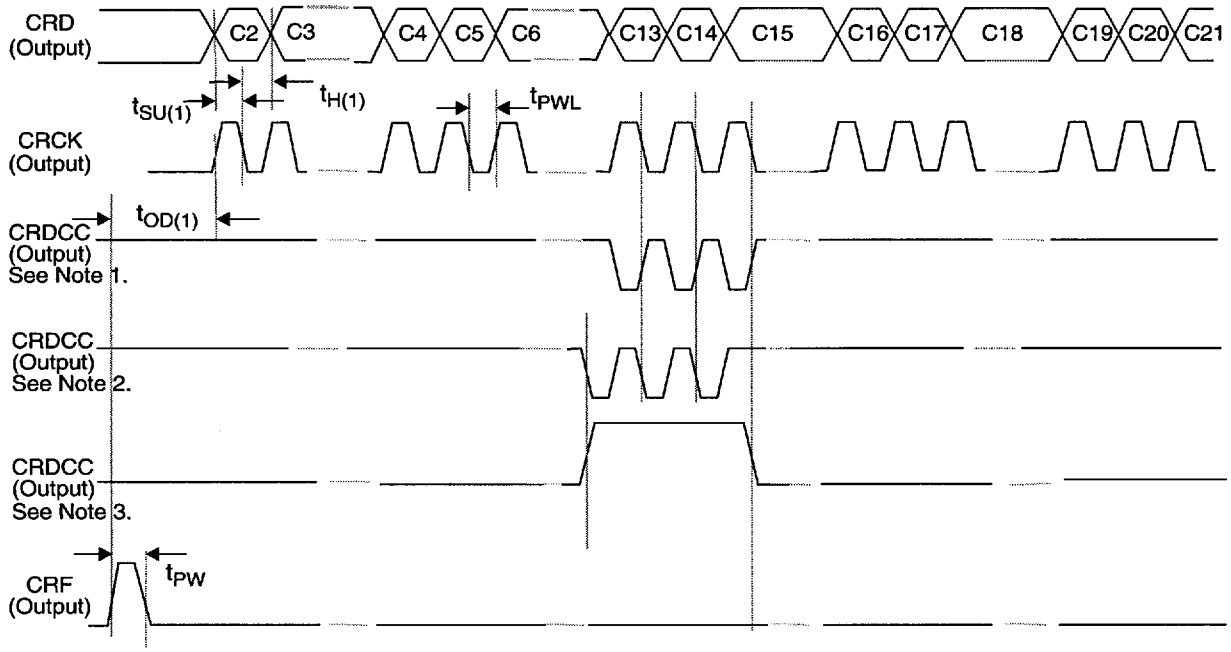
Figure 9. C-Bit Transmit Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CXCK high time	t_{PWH}		85 t_{CYC}		ns
CXD set-up time to CXCK↑	t_{SU}	20			ns
CXD hold time after CXCK↑	t_H	40			ns
CXCK output delay after CXF↑	t_{OD}		170 t_{CYC}		ns
CXF pulse width	t_{PW}		85 t_{CYC}		ns

Note: t_{CYC} is the D3TC clock period (see Figure 4).

Figure 10. C-Bit Receive Output Timing

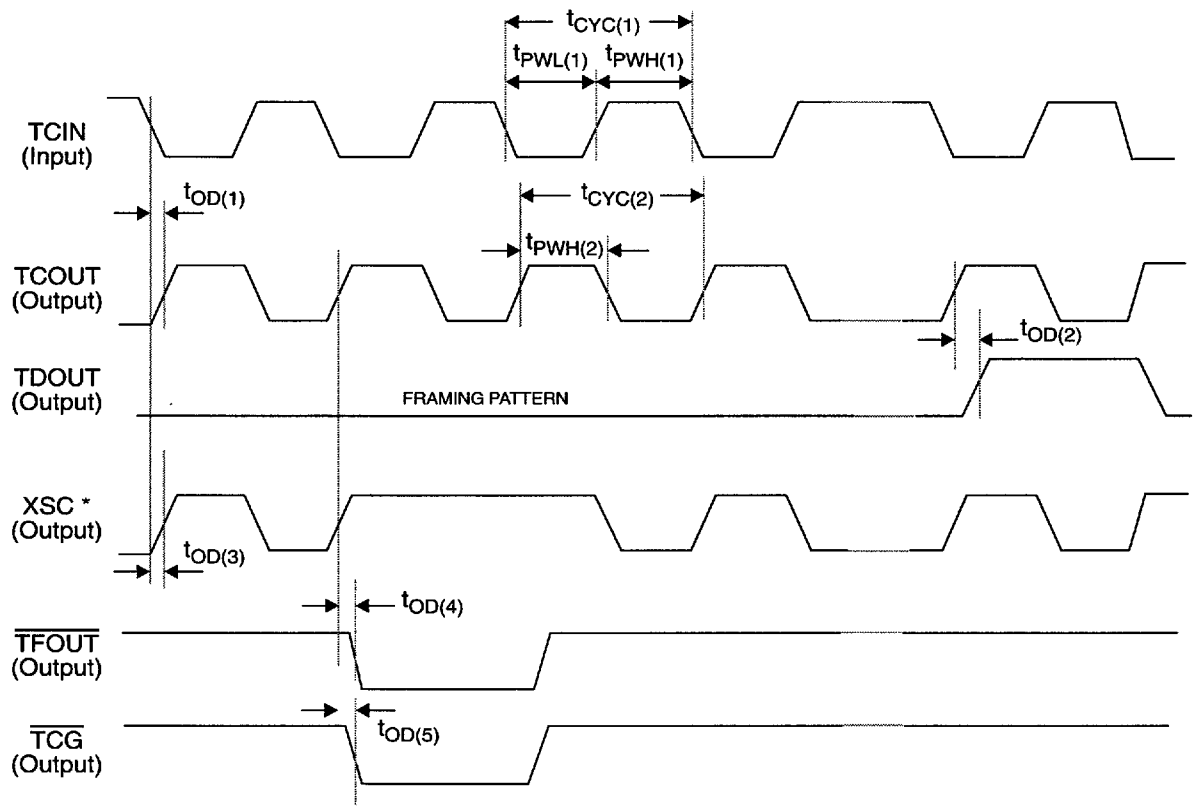


Notes:
1. Output for EMODE=0 or (EMODE=1, CRDCINV=0 and M13DLM=0)
2. Output for (EMODE=1, CRDCINV=1 and M13DLM=0)
3. Output for (EMODE=1, CRDCINV=X and M13DLM=1)

Parameter	Symbol	Min	Typ	Max	Unit
CRCK low time	t_{PWL}		85 t_{CYC}		ns
CRD set up time before CRCK↓	$t_{SU(1)}$		85 t_{CYC}		ns
CRD hold time after CRCK↓	$t_{H(1)}$		85 t_{CYC}		ns
CRCK output delay after CRF↑	$t_{OD(1)}$		170 t_{CYC}		ns
CRF pulse width (high)	t_{PW}		85 t_{CYC}		ns

Note: t_{CYC} is the RCS clock period (see Figure 7).

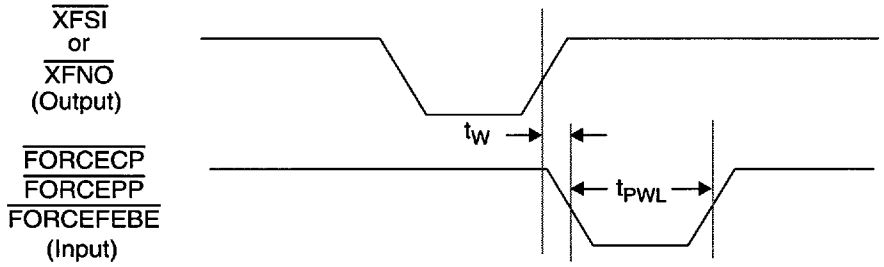
Figure 11. Transmit Reference Generator Timing



* Note: XSC signal occurs at pin 66 when control bits SER and TCGEN are both set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TCIN clock period	$t_{CYC(1)}$	20	22.3		ns
TCIN high time	$t_{PWH(1)}$	10	11.2		ns
TCIN low time	$t_{PWL(1)}$	10	11.2		ns
TCIN duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	40	50	60	%
TCOUT clock period	$t_{CYC(2)}$	$t_{CYC(1)}$	22.3		ns
TCOUT high time	$t_{PWH(2)}$	$t_{PWH(1)}$	11.2		ns
TCOUT output delay after TCIN↓	$t_{OD(1)}$	2	4		ns
TDOUT output delay after TCOUT↑	$t_{OD(2)}$	2	4	7	ns
XSC output delay after TCIN↓	$t_{OD(3)}$	2	4		ns
$\overline{\text{TFOUT}}$ output delay after TCOUT↑	$t_{OD(4)}$	2	4	7	ns
$\overline{\text{TCG}}$ output delay after TCOUT↑	$t_{OD(5)}$	2	4	7	ns

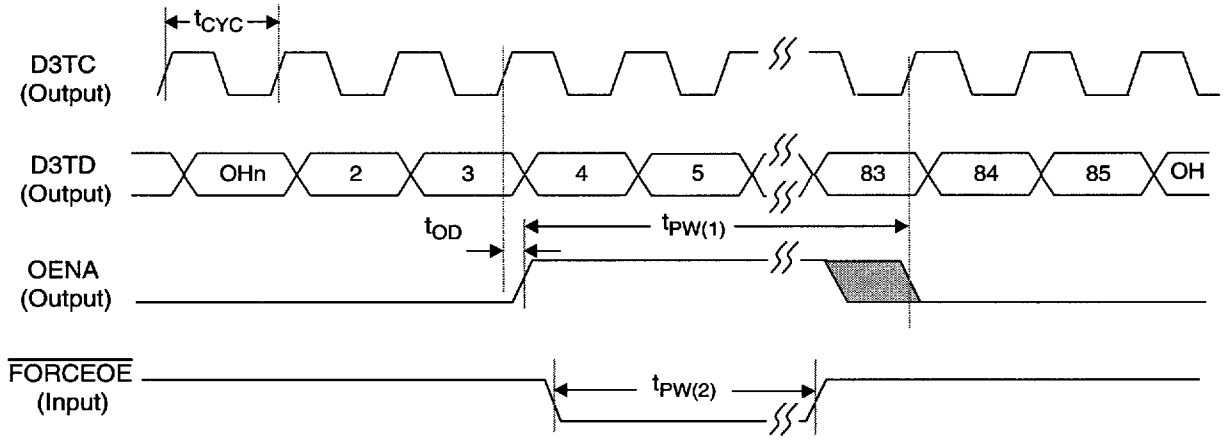
Figure 12. Force Error Timing (C-Bit Parity, P-Bit Parity, FEBE)



Parameter	Symbol	Min	Typ	Max	Unit
Force error wait time after framing pulse	t_W			Note	ns
Force error low time	t_{PWL}	20	22		ns

Note: If the force error signal occurs during the first subframe of the DS3 frame (680 XCK clock cycles), then the error occurs during that frame. Otherwise, the error is transmitted in the next frame.

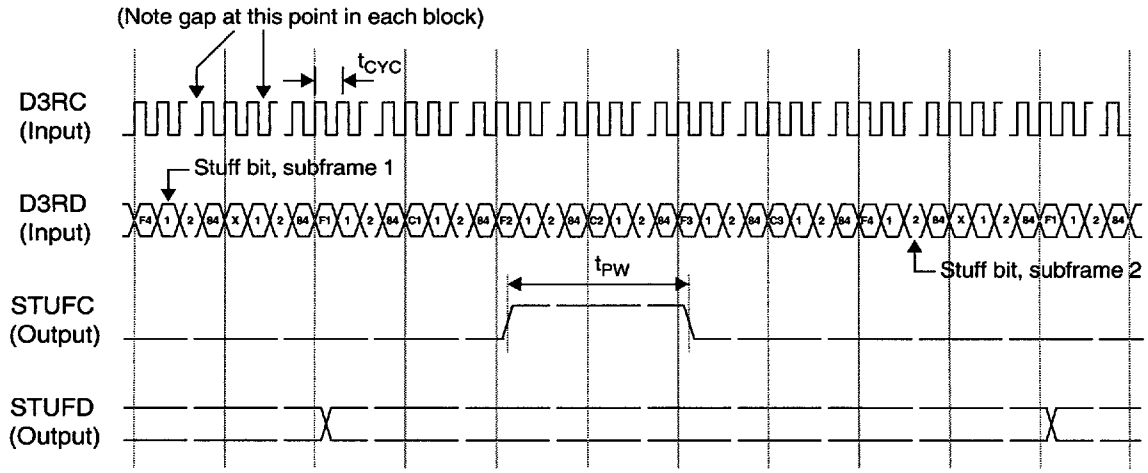
Figure 13. Force Overhead Bit Error Timing



Parameter	Symbol	Min	Typ	Max	Unit
D3TC clock period	t_{CYC}	20	22.35		ns
OENA output delay after D3TC↑	t_{OD}	0		4	ns
OENA pulse width (high)	$t_{PW(1)}$	9 t_{CYC}		80 t_{CYC}	
$\overline{\text{FORCEOE}}$ pulse width (low)	$t_{PW(2)}$	2 t_{CYC}		45 t_{CYC}	

Note: $\overline{\text{FORCEOE}}$↑ resets OENA.

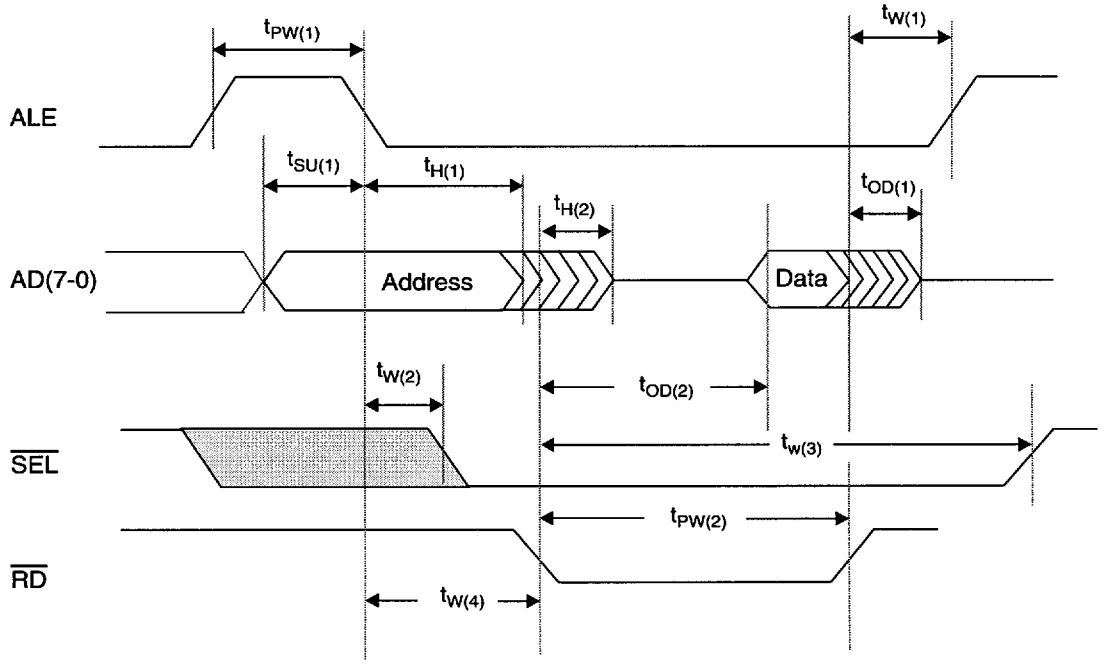
Figure 14. Stuff Opportunity Bit Timing (M13 Mode)



Parameter	Symbol	Min	Typ	Max	Unit
D3RC clock period	t_{CYC}		22.35		ns
STUFC pulse width (high)	t_{PW}		3800		ns

Notes:
1. See Figure 3 for timing of the D3RC and D3RD signals.
2. Each block of 85 22.35 ns time slots is 1900 ns in duration.
3. The clock output STUFC is intended to be used to strobe the data output STUFD. It is a low frequency signal that repeats at 15.2 µs intervals. STUFD has a 3.8 µs set up time to STUFC↑ and a hold time of 11.4 µs after STUFC↑.

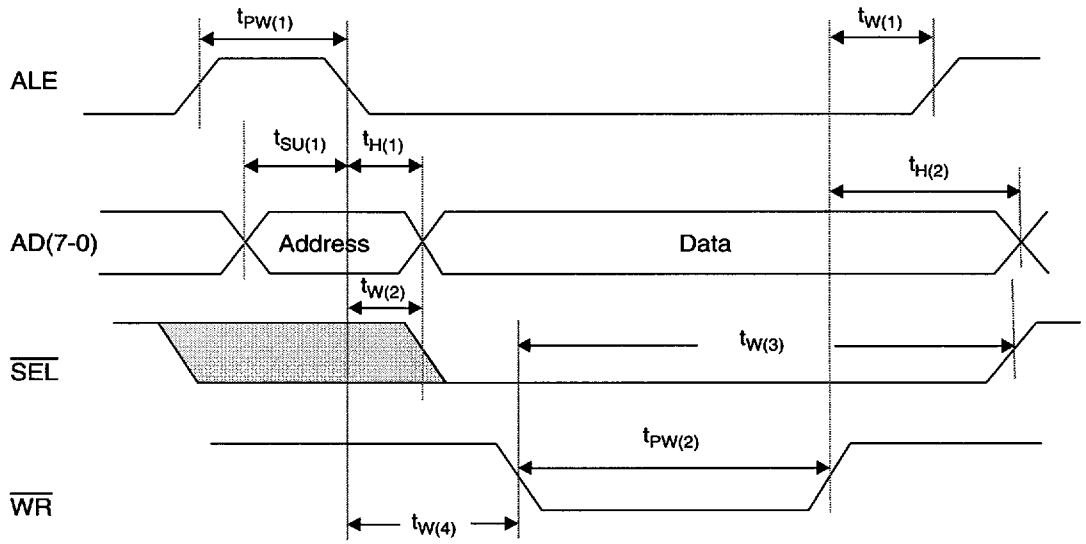
Figure 15. Microprocessor Read Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	30			ns
ALE wait after $\overline{RD}$ ↑	$t_{W(1)}$	0			ns
Address set-up time to ALE ↓	$t_{SU(1)}$	20			ns
Address hold time after ALE ↓	$t_{H(1)}$	10			ns
Address hold time after $\overline{RD}$ ↓	$t_{H(2)}$			50	ns
Data output delay (to tristate) after $\overline{RD}$ ↑	$t_{OD(1)}$	10		20	ns
Data output delay after $\overline{RD}$ ↓	$t_{OD(2)}$			80	ns
$\overline{SEL}$ wait after ALE ↓	$t_{W(2)}$			40	ns
$\overline{SEL}$ wait after $\overline{RD}$ ↓	$t_{W(3)}$	40			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	100			ns
$\overline{RD}$ wait after ALE ↓	$t_{W(4)}$	10			ns

Notes:
1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the read cycles are valid.

Figure 16. Microprocessor Write Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	0			ns
Address set-up time to ALE ↓	$t_{SU(1)}$	30			ns
Address hold time after ALE ↓	$t_{H(1)}$	10			ns
Data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns
$\overline{SEL}$ wait after ALE ↓	$t_{W(2)}$			40	ns
$\overline{SEL}$ wait after $\overline{WR}$ ↓	$t_{W(3)}$	40			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	50			ns
$\overline{WR}$ wait after ALE ↓	$t_{W(4)}$	10			ns

Notes:
1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the write cycles are valid.

OPERATION

POWER, GROUND AND EXTERNAL COMPONENTS

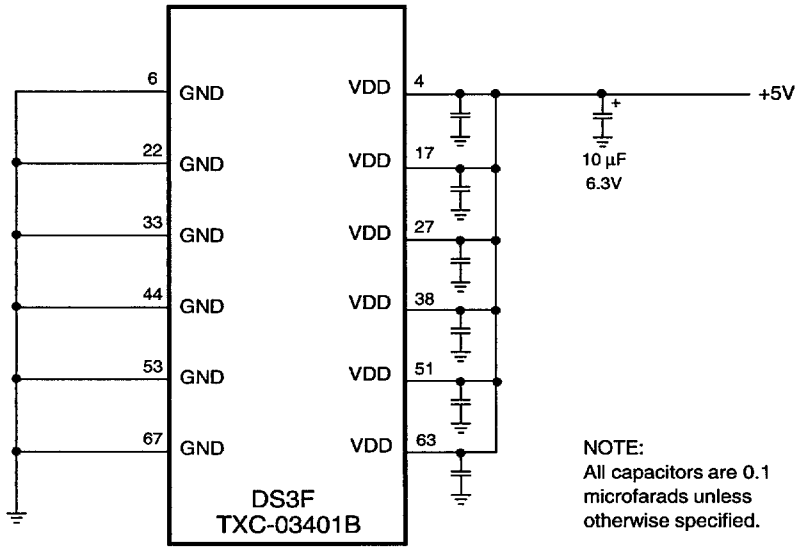


Figure 17. Power Supply Connections

Figure 17 shows the recommended power and ground connection method for the DS3F device. Separate planes should be employed for VDD and GND. Bypass networks consist of a 10 µF capacitor in parallel with 0.1 µF capacitors for each VDD pin, as shown. These 0.1 µF capacitors should be RF-quality and closely connected to each of the device's VDD pins to decouple them to ground.

THROUGHPUT DELAYS

The DS3F throughput delays for the serial terminal interface are given below in terms of DS3 bit times (1 bit = 22.35 nsec nominal):

1. The throughput delay from the transmit terminal side input to the transmit line side output is 3 bit times.

2. The throughput delay from the receive line side input to the receive terminal side output is 2 bit times.

MEMORY MAP

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	RXLOS	RXOOF	RXAIS	RXIDL	RXLOC	TXLOC	XRX2	XRX1
01	R/W	NOFEBE	TXAIS	ENAIS	TXIDL	M13MODE	SER	3LOOP	XTX
02	R	FEBE / Framing Bit Error Performance Counter (saturating counter, clears when read)							
03	R	C-Bit Parity Error Performance/Number of Frames Counter (saturating counter, clears when read)							
04	R	P-Bit Parity Error Performance Counter (saturating counter, clears when read)							
05	R/W	EMODE	START	FEAC Transmit Data					
06	R	FIDL	NEW	FEAC Receive Data					
07	R(L)	RXLOS	RXOOF	RXAIS	RXIDL	CERR	LOC	X2ERR	X1ERR
08 ***	R/W	FBEC	MBEC	TBLUE	OUTDIS	ITX2	ITX1	RESET	LPTIME
09 ***	R(L)	SEF	Unused**	RBLUE	Unused**	Unused**	Unused**	Unused**	STKOVFL
0A ***	R	F-Bit Error Counter (saturating counter, clears when read)							
0B ***	R	M-Bit Error Counter (saturating counter, clears when read)							
0C ***	R/W	RTPLLEN	RTPLOOP	TESTLOCK	M13DLM	DLCB1	C21	MCB1	CPARINV
0D ***	R/W	Unused**	DFEXEC	Double FEAC Transmit Data					
0E ***	R/W	FEAC10	Unused**	RGCEN	TGCEN	HINTINV	HINTEN	MOOFW	CRDCINV
0F ***	R	MOREFEAC	FEACVLID	RFEAC6	RFEAC5	RFEAC4	RFEAC3	RFEAC2	RFEAC1
10 ***	R(L)	RXLOS	RXOOF	RXAIS	RXIDL	NEWFEAC	RTLOC	SEF	XERR
11 ***	R/W	RXLOSEN	RXOOFEN	RXAISEN	RXIDLEN	NFEACIEN	RTLOCEN	SEFEN	XERREN
12 ***	R	Coding Violation / Excessive Zeros Counter, low order byte (saturating counter, clears when read)							
13 ***	R	Coding Violation / Excessive Zeros Counter, high order byte (saturating counter, clears when read)							
14 ***	R/W	STFREN	STFTGEN	FORCEFEBE	FORCEPP	FORCECP	TSTCNTR	EXZEN	CVEN

* Note: R = Read-only; R(L) = Read-only, latched (clears on read); R/W = Read/Write.
** Note: All unused read-only bits will contain 0. All unused read/write bits are to be set to 0 by the application software.
*** Note: Addresses 08H through 14H are enabled only when control bit EMODE at Address 05H, Bit 7 is set to 1.

MEMORY MAP DESCRIPTIONS

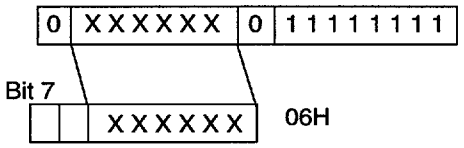
Address	Bit	Symbol	Description
00	7	RXLOS	**Receive DS3 Loss of Signal:** A receive LOS alarm occurs when the incoming DS3 data (D3RD) is stuck low for at least 2048 clock cycles (D3RC). Recovery occurs when two or more ones are detected in the incoming data bit stream.
	6	RXOOF	**Receive DS3 Out of Frame:** A receive OOF occurs when, in a sliding window of 16 F-bits, three F-bits are in error, or when there are M-bit errors in two frames of a window of three (MOOFW=1) or four (MOOFW=0) consecutive frames. Recovery occurs when 16 consecutive error-free F-bits are detected in the repeating 1001 F-bit framing pattern, followed by the M-bit pattern of 010 being detected for two consecutive frames. Recovery takes approximately 0.95 milliseconds, worst case. An OOF also inhibits the performance counters at Addresses 02H, 03H, 04H, 0AH and 0BH. The terminal output during an RXOOF condition is the received data.
	5	RXAIS	**Receive DS3 Alarm Indication Signal (AIS):** A Receive DS3 AIS condition is declared, and the RXAIS bit is set to 1, when RXOOF is 0 and all of the following events have occurred during a frame: the three C-bits in each subframe have been 0 for five consecutive frames, at least 95% of the payload of each subframe has contained a repeating 1010.... bit sequence which begins after each overhead bit for five consecutive frames, and the latest X-bit received is the sixteenth or higher to have arrived with a 1 value in the most recent nineteen X-bits received (i.e., sixteen or more 1 values have occurred since there was an accumulated total of four 0 values). Recovery to 0 occurs during the first subsequent subframe when one of these events could occur but does not. AIS detection conforms to the bit error rate requirement stated in Bellcore document TR-TSY-000191 (Issue 1, May 1986), "Alarm Indication Signal Requirements and Objectives."
	4	RXIDL	**Receive DS3 Idle:** A Receive DS3 Idle condition is declared, and the RXIDL bit is set to 1, when RXOOF is 0 and all of the following events have occurred during a frame: the C7, C8 and C9 bits in subframe 3 are 0, at least 95 per cent of the payload of each subframe contains a repeating 1100.... bit sequence which begins after each overhead bit for a period of one frame, and the latest X-bit received is the sixteenth or higher to have arrived with a 1 value in the most recent nineteen X-bits received (i.e., sixteen or more 1 values have occurred since there was an accumulated total of four 0 values). Recovery to 0 occurs at the end of the first subsequent frame during which not all of these events occur.
	3	RXLOC	**Receive DS3 Loss of Clock:** An alarm occurs when there are no transitions in the receive clock (D3RC) for seven or more XCK clock cycles. XCK clock must be present to count D3RC cycles. Recovery occurs on the first transition of D3RC.
	2	TXLOC	**Transmit DS3 Loss of Clock:** An alarm occurs when there are no transitions in the transmit clock (XCK) for seven or more D3RC receive clock cycles. D3RC clock must be present to count XCK cycles. A failure causes the receive clock to become the transmit clock. This permits the microprocessor interface and transmitter to continue to function. Recovery occurs on the first transition of XCK.

Address	Bit	Symbol	Description
00 (cont.)	1	XRX2	**Receive X-Bit Number 2:** This bit position indicates the receive state of X2. This bit position is updated each frame.
	0	XRX1	**Receive X-Bit Number 1:** This bit position indicates the receive state of X1. This bit position is updated each frame.
01	7	NOFEBE	**FEBE Transmission Disabled:** A one written into this position disables the transmission of a FEBE when an F-bit or M-bit error or C-bit parity error occurs.
	6	TXAIS*	**Transmit DS3 Alarm Indication Signal:** A one written into this bit position causes the DS3F to transmit a DS3 AIS. A one must also be written (if not already written) into bit 0 (XTX) in this register location in order to satisfy the definition of DS3 AIS.
	5	ENAIS	**Enable Transmit DS3 Alarm Indication Signal Automatically:** A one written into this bit position causes the DS3F to transmit DS3 AIS when the RXOOF bit (Register 00, bit 6) is set to 1.
	4	TXIDL*	**Transmit DS3 Idle Signal:** A one written into this bit position causes the DS3F to transmit a DS3 idle signal. A one must also be written (if not already written) into bit 0 (XTX) in this register location, in order to satisfy the definition of DS3 idle.
	3	M13MODE	**M13 Operating Mode:** A one enables the DS3F to operate in the M13 mode as specified in Bellcore TR-TSY-000009, and the ANSI T1.107-1988 standard. The M13 operating mode is available for the bit-serial terminal side interface only. A zero enables the DS3F to operate in the C-bit parity mode that is specified in the ANSI T1.107-1988 T1X1/89-034R2 draft supplement. The C-bit operating mode is available for either a serial or parallel terminal side interface.
	2	SER	**Serial Interface Terminal Side:** A one configures the DS3F terminal side to be a serial interface for both receive and transmit. A zero configures the terminal side to be a nibble interface. The serial interface is operational in either the M13 or C-bit parity mode. The nibble interface is operational for the C-bit parity mode only. In the M13 operating mode, the transmit C-bit interface is disabled and terminal side C-bits are transmitted as user data.
	1	3LOOP	**DS3 Transmit-to-Receive Loopback:** A one written into this bit position disables the receive input and causes the transmit output to be looped back as receive data. Transmit data is provided at the output (D3TD).
	0	XTX	**Transmit X-Bits:** The X-bits may be used to transmit a yellow alarm or as a low-speed signaling channel. A one written into this bit position causes the DS3F to transmit a one for both X1 and X2.

*Note: If both TXAIS and TXIDL are set, TXAIS takes precedence.

Address	Bit	Symbol	Description
02	7-0	FBn	**FEBE / Framing Bit Error Performance Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts the FEBE indications received. A FEBE indication occurs for a received DS3 frame if any one or more of the C10, C11, or C12 bits in the frame is zero. When the DS3F is operating in the M13 mode, this counter counts framing bit error indications. An error indication occurs for each F-bit in a received DS3 frame that has a value different from the expected framing pattern. In the M13 mode, the counter is frozen during a DS3 loss of signal or an out of frame condition.
03	7-0	CPn	**C-Bit Parity Error Performance / Number of Frames Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts C-bit parity error indications. An error indication occurs for each received DS3 frame in which the majority (i.e., two or more) of the C7, C8 and C9 parity bits differ from the parity bit which was calculated by the DS3F over all 4704 received payload data bits of the preceding frame. For each such indication, the DS3F also provides a FEBE indication in the transmit line output, unless control bit NOFEBE is 1. When the DS3F is operating in the M13 mode, this counter counts DS3 frames. It takes approximately 27 milliseconds to count 255 frames. The application's software may use this DS3 frame count in conjunction with the count contained in the framing bit error counter (Address 02H) to determine an approximate bit error rate (BER). In the M13 mode, the counter is frozen during a DS3 loss of signal or an out of frame condition.

Address	Bit	Symbol	Description
04	7-0	PPn	**P-Bit Parity Error Performance Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). This counter counts P-bit parity error indications in either C-bit parity or M13 operating mode. An error indication occurs for each received DS3 frame during which one or both of the P1 and P2 bits differ from the parity bit calculated by the DS3F over all 4704 of the received payload data bits of the preceding DS3 frame. The DS3F does not provide a FEBE indication in the transmit line output for each such indication. The counter is frozen during a DS3 loss of signal or an out of frame condition.
05	7	EMODE	**Extended-features Mode Control Bit:** When this bit is set to 1, the Extended-features mode of the DS3F is activated; control bit positions in memory map addresses above 07H are enabled. When this bit is set to 0, the Normal mode of the DS3F is activated; control bit positions in memory map addresses above 07H are disabled.
	6	START	**Start FEAC Message:** When START is set to 1, the DS3F starts to send repetitively the 16-bit FEAC code word, including the XXXXXX bits in bit positions 5-0, using the third C-bit (C3). If START is 0, then the third C-bit is always zero and the FEAC channel is disabled. (See also FEAC10 at Address 0EH, bit 7.)
	5-0	FEAC Transmit Data	**Transmit FEAC Message:** The third C-bit (C3) is used as a far end alarm and control (FEAC) channel. The FEAC channel uses a 16-bit code word that has the form 0XXXXXX0 11111111 to convey information, where the XXXXXX bits are the FEAC message. Bit 0 corresponds to the right-most bit in the FEAC message. The FEAC word is inserted for the X's and the DS3F inserts the necessary 0's and trailing 1's to complete the 16-bit word. Specific words that are transmitted for alarm or status conditions must be sent for the duration of the condition or a minimum of 10 code repetitions. When the FEAC channel is used for control purposes, the two-word control codes are repeated 10 times. For example, to activate or deactivate a loopback, the first loopback control code word must be transmitted 10 times, followed by 10 repetitions of the second DS3 (or DS1) line code word. The controlling software must set the duration of the FEAC message by setting and clearing bit 6 of this register (START).

Address	Bit	Symbol	Description
06	7	FIDL	**Receive Single FEAC Word:** Bit 7 (FIDL) is the FEAC idle channel indication. It clears whenever a zero C3 bit is received framing the six-bit variable word. Bit 7 cannot be reset by a microprocessor read cycle. Bit 6 (NEW) indicates when a new FEAC word has been detected. NEW is set when the DS3F receives a FEAC message for five consecutive FEAC message intervals (5 x 16 = 80 frames). It clears when the register is read. Bits 5-0 (FEAC receive data) constitute the variable (XXXXXX) field in the FEAC word. A FEAC word is read in the field in the same order of being received as shown below: **16-Bit FEAC Word**  The following table lists possible FEAC combinations: **FIDL** / **NEW** / **Status** 0 / 0 / FEAC channel busy - No message received since last read cycle 1 / 0 / FEAC channel idle - No message received since last read cycle 0 / 1 / New message received - FEAC channel busy 1 / 1 / New message received - FEAC channel idle Note: There is no buffering for the received FEAC message. The latest, validated FEAC message is provided and bit 6 (NEW) is set to one even if the previous message is not read.
	6	NEW	
	5-0	FEAC Receive Data	
07	7-0	RXLOS RXOOF RXAIS RXIDL CERR LOC X2ERR X1ERR	**Latched-Bit Register:** Bits 7-4 in this location are the latched values of the corresponding bits in location 00H. All of the bits in this register latch and are cleared on a read cycle, but RXAIS maintains its value when the DS3F is in TR loopback or no TX terminal input is present. Bit 3 (CERR) latches when the DS3F receives a C1 bit equal to zero. Bit 2 (LOC) latches when either an RXLOC (bit 3 - 00H) or an TXLOC (bit 2 - 00H) occurs. The X2ERR and X1ERR bits (bits 1 and 0) are latched at the inverse of the XRX2 and XRX1 values (normally 1), so they are normally 0, and a value of 1 indicates an error in the corresponding received X-bit.

Address	Bit	Symbol	Description
08	7	FBEC	**Control F-bit Error Counter:** When this bit is set to 1, the error counter in register 0AH will count only F-bit errors. When this bit is set to 0, the error counter will count both F-bit and M-bit errors. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment).
	6	MBEC	**Control M-bit Error Counter:** When this bit is set to 0, the error counter in register 0BH will count only M-bit errors. When this bit is set to 1, the error counter will count both M-bit and F-bit errors. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment).
	5	TBLUE	**Transmit Blue code AIS condition:** When this bit is set to 1, the device will transmit all 1's.
	4	OUTDIS	**Output Disable:** When set to 1, this control bit disables all DS3F output pins except the microprocessor interface address/data bus.
	3	ITX2	**Invert Transmit X2:** When set to 1, the X2 bit is inverted from the state specified by the XTX bit (Address 01H, bit 0), which is 1 for XTX=1 and 0 for XTX=0.
	2	ITX1	**Invert Transmit X1:** When set to 1, the X1 bit is inverted from the state specified by the XTX bit (Address 01H, bit 0), which is 1 for XTX=1 and 0 for XTX=0.
	1	RESET	**Reset:** When set to 1, the transmit frame counter is reset. If left set to 1 for longer than one frame, then a register reset also occurs and this bit is cleared. When a register reset occurs, all bits in registers 02H - 04H and 08H - 14H, and bit 6 of register 05H, will be cleared. If this bit is set from 1 back to 0 before a frame has elapsed then no register reset will occur. If this bit is set to 1 when pin $\overline{\text{XFSI}}$ is low then a register reset occurs immediately.
	0	LPTIME	**Receive Loop Timing:** When set to 1, this control bit disables the transmit clock input (XCK) and causes the DS3 receive clock (D3RC) to become the DS3 transmit clock. XSC and XNC also become the DS3 receive clock. The Transmit Reference Generator does not utilize the DS3 receive clock and should not be used if this mode is to be used. If the DS3 receive clock fails in this mode, the DS3F switches over to the transmit clock.

Address	Bit	Symbol	Description
09	7	SEF	**Severely Errored Frame Indication:** A 1 indicates that a Severely Errored Frame condition (SEF) has been detected. An SEF is defined as 3 out of 16 F-bits in error, utilizing a sliding window of 16 bits. This is a latched bit, and it clears on a microprocessor read cycle. This bit will then relatch if the condition that causes this bit to latch is still present.
	6	Unused	This bit is internally set to 0.
	5	RBLUE	**Receive Blue code AIS condition:** When this bit is set to 1, the device has detected all 1's. This is a latched bit, and it clears on a microprocessor read cycle. This bit will then relatch if the condition that causes this bit to latch is still present.
	4-1	Unused	These four bits are internally set to 0.
	0	STKOVFL	**Stack Overflow indicator for register OFH receive FEAC FIFO:** This bit is set to 1 when the receive FEAC circuit has detected and stored in its stack more than four FEAC words since the last read of register OFH. This is a latched bit, and it clears on a microprocessor read cycle.
0A	7-0		**Counter for errored DS3 F-bits (and M-bits):** An 8-bit saturating counter that counts the number of F-bits that are in error since the last read cycle, if FBEC at Address 08H, bit 7 is set to 1. If FBEC is set to 0, this counter will count both F-bit and M-bit errors. The counter is cleared on a microprocessor read cycle.
0B	7-0		**Counter for errored DS3 M-bits (and F-bits):** An 8-bit saturating counter that counts the number of M-bits that are in error since the last read cycle, if MBEC at Address 08H, bit 6 is set to 0. If MBEC is set to 1, this counter will count both M-bit and F-bit errors. The counter is cleared on a microprocessor read cycle.
0C	7	RTPLLEN	**Receive-to-Transmit Payload Loopback Lock Enable:** To activate receive-to-transmit payload loopback, this bit must first be set to 1 for at least one frame after RTPLOOP (bit 6) has been set to 1 and then be set to 0. This resets the transmit frame counter so that the data will be synchronized to the overhead bits when using the loopback. The loopback commences on the transition to 0 and terminates when RTPLOOP is cleared to 0.
	6	RTPLOOP	**Receive-to-Transmit Payload Loopback:** This bit must be set to 1 to permit RTPLLEN (bit 7) to activate receive-to-transmit payload loopback. This loopback causes the receive output data (payload only) to be internally connected to the transmit side data input, as shown in Figure 1. The loopback condition is terminated by clearing this bit to 0. The $\overline{\text{XFSI}}$ input pulse must not be applied while RTPLOOP is set to 1.
	5	TESTLOCK	**Test Lock:** Test bit to reset the transmit frame counter at a different time with respect to the receive. For test purposes only. Normally set to 0.

Address	Bit	Symbol	Description
0C (cont.)	4	M13DLM	**M13 Data Link Mode:** When this control bit is set to 0, the C-Bit Transmit Data Link Clocks (CXDCC and CRDCC) are gapped clocks provided for clocking in the three data link bits (C13, C14, and C15). When set to 1, then the outputs CXDCC and CRDCC become pulses that identify the location of the three data link C-bits (the same as in the M13 device). See Figures 9 and 10.
	3	DLCB1	**Data Link C-bits Off:** When set to 1, the C-bits used for the data link (C13, C14 and C15) will be set to 1. When set to 0, the values for these bits will be taken from the input pin CXD.
	2	C21	**C2 Off:** When this bit is set to 1, the C2 bit will be 1. When this bit is set to 0, the C2 bit value will be taken from the input pin CXD.
	1	MCB1	**Most C-bits Off:** When set to 1, the C-bits C4 - C6, and C16 - C21 for the data link will all be set to 1. When set to 0, the data for these bits is taken from the input pin CXD.
	0	CPARINV	**Parity and FEBE C-bits Off:** When this control bit is set to 1, the C-bits used for parity (C7, C8, and C9) and the C-bits used for FEBE (C10, C11 and C12) will all be set to the inverse of the state that is calculated for the parity and FEBE. When set to 0, the data for these bits is taken from the calculations for parity and FEBE.
0D	7	Unused	This bit is to be set to 0 by the application software.
	6	DFEXEC	**Execute Double FEAC Transmission:** When set to 1, this control bit causes the DS3F to transmit 10 repetitions of the 16-bit FEAC codeword using data from the Double FEAC Transmit Data field in bits 5-0, followed by 10 repetitions of the 16-bit FEAC codeword using data from the FEAC Transmit Data field in Address 05H, bits 5-0. This bit is cleared upon completion of the transmission.
	5-0		**Double FEAC Transmit FEAC Message:** The third C-bit (C3) is used as a far end alarm and control (FEAC) channel. The FEAC channel uses a 16-bit code word that has the form 0XXXXXX0 11111111 to convey information, where the XXXXXX bits are the FEAC message. Bit 0 corresponds to the right-most bit in the FEAC message. The FEAC word is inserted for the X's and the DS3F inserts the necessary 0's and trailing 1's to complete the 16-bit word. Specific words that are transmitted for alarm or status conditions must be sent for the duration of the condition or a minimum of 10 code repetitions. When the FEAC channel is used for control purposes, the two-word control codes are repeated 10 times. This field is used for the XXXXXX content of the first word of a double word message. Both FEAC words are sent ten times automatically when DFEXEC is set to 1.

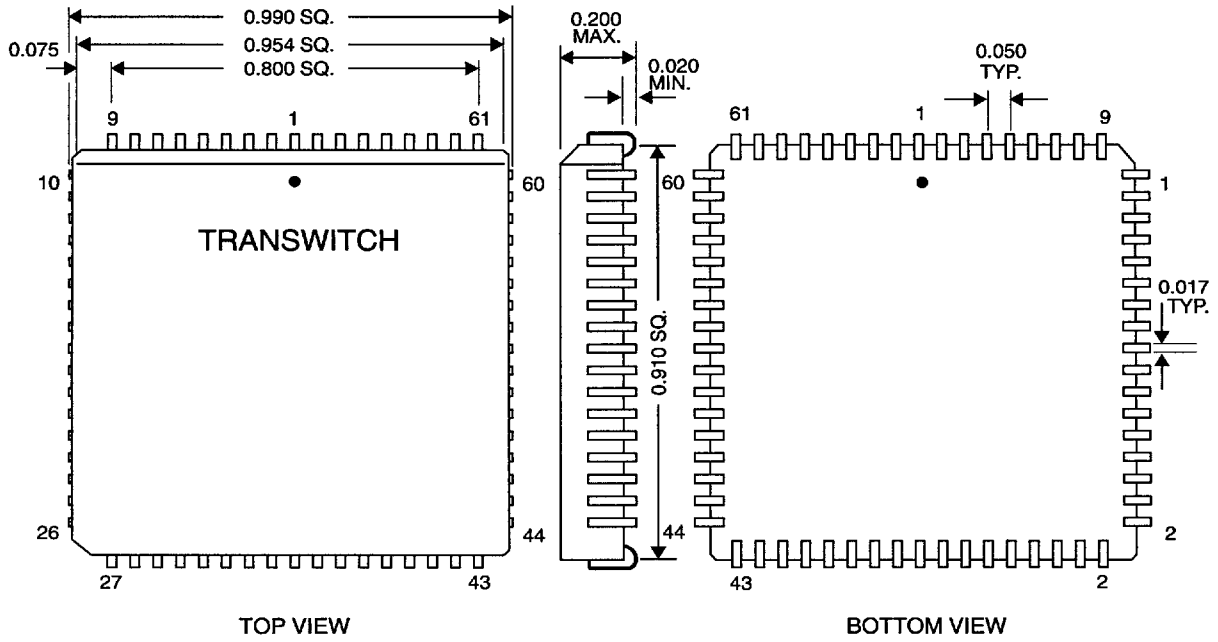
Address	Bit	Symbol	Description
0E	7	FEAC10	**Transmit FEAC Word 10 Times:** When set to 1, the duration of the single FEAC transmission (started by setting to 1 the control bit START in bit 6 of Address 05H) is exactly 10 times. When set to 0, the single FEAC transmission is continuous.
	6	Unused	This bit is to be set to 0 by the application software.
	5	RGCEN	**Receive Gapped Clock Output Enable:** When set to 1 while the SER (Serial) bit is set to 1, a gapped clock signal is generated by the receive circuitry and sent as output on the RNIB3 pin (pin 39).
	4	TGCEN	**Timing Generator Gapped Clock Output Enable:** When set to 1 while the SER (Serial) bit is set to 1, a gapped clock signal sent as output on the XSC/XNC pin (pin 66). This signal is synchronous with bit 1 in each 85-bit group (56 overhead bits) of the DS3 frame.
	3	HINTINV	**Hardware Interrupt Invert:** When set to 1, this control bit inverts the HINT output so that it becomes active low.
	2	HINTEN	**Hardware Interrupt Enable:** When set to 1, this control bit enables the STUFD/HINT output (pin 15) to generate a hardware interrupt to the microprocessor based on the existence of alarm conditions and the state of the interrupt mask register bits at Address 11H.
	1	MOOFW	**M-bit Out Of Frame Window:** When set to 1, this control bit changes from 4 frames to 3 frames the duration of the window for M-bit errors that will cause the Out Of Frame condition to be reported.
	0	CRDCINV	**CRDCC Extended-feature Inversion:** When set to 1 while control bit M13DLM=0, this control bit advances the timing of the three CRDCC pulses by one-half a cycle of CRCK (see Figure 10).
0F	7	MOREFEAC	**MORE Valid FEAC words remain in the stack:** A 1 indicates that there is at least one more valid FEAC word in the stack (bits 5-0).
	6	FEACVLID	**FEAC Word Valid:** A 1 indicates that the FEAC word in bits 5-0 is valid.
	5-0	RFEAC6 RFEAC1	**Receive FEAC Stack:** This field provides access to the top word of a four-word deep push-down FIFO stack (maintained internally) that holds the received FEAC words. If more than four FEAC words have been received since the last read of this register then the STKOVFL bit (Address 09H, bit 0) will be set to 1. The stack will retain the 4 most recent FEAC words.

Address	Bit	Symbol	Description
10	7	RXLOS	**Receive DS3 Loss Of Signal Interrupt:** This latched bit is set to 1 when RXLOS is detected. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	6	RXOOF	**Receive DS3 Out Of Frame Interrupt:** This latched bit is set to 1 when RXOOF is detected. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	5	RXAIS	**Receive DS3 Alarm Interrupt:** This latched bit is set to 1 when RXAIS is detected. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	4	RXIDL	**Receive DS3 Idle Interrupt:** This latched bit is set to 1 when RXIDL is detected. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	3	NEWFEAC	**New FEAC Receive Interrupt:** This latched bit is set to 1 when a new FEAC word has been received 5 times consecutively. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	2	RTLOC	**Receive or Transmit DS3 Clock Failure Interrupt:** This latched bit is set to 1 when either RXLOC or TXLOC occurs. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	1	SEF	**Severely Errored Frame Indication Interrupt:** This latched bit is set to 1 when SEF occurs. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	0	XERR	**Receive X-Bit Error Interrupt:** This latched bit is set to 1 when X1 or X2 is 0. This bit is used to send a hardware interrupt on the STUFD/HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H.
11	7	RXLOSEN	**Alarm Interrupt Enable Mask Bits:** If any of the eight bits in this register is set to 1, a hardware interrupt will be generated at the STUFD/HINT output pin (pin 15) when the corresponding latched alarm bit is set to 1 in the register at Address 10H, provided that the HINTEN bit at Address 0EH, bit 2 is set to 1.
	6	RXOOFEN	
	5	RXAISEN	
	4	RXIDLEN	
	3	NFEACIEN	
	2	RTLOCEN	
	1	SEFEN	
	0	XERREN	

Address	Bit	Symbol	Description
12	7-0	CVEXZ7-CVEXZ0	**Coding Violation 16-Bit Counter, low order byte:** A 16-bit saturating counter that counts the D3RC cycles for which CV is high (and those for which EXZ is low, if EXZEN is set to 1). These signals are outputs from the ART (CV only) and ARTE devices and they are expected to be related to the rising edge of D3RC. There are actually two counters, so that when one counter is being read, the other counter is counting. A read cycle for this register causes this switch to toggle, and the current count data for the low order byte to be provided as output.
13	7-0	CVEXZ15-CVEXZ8	**Coding Violation 16-Bit Counter, high order byte:** A read cycle for this register causes the high order count byte which corresponds to the most recently read low order count byte from the register at Address 12H to be provided as output and then this counter (all 16 bits) is cleared to 00H. It is therefore important to read the register at Address 12H first, followed by a read of this register, to insure that a correct count is obtained.
14	7	STFREN	**Stuff Receive Enable:** When set to 1, the $\overline{RCG}$ output of the receive data circuitry will include the stuff bit locations if 2 out of 3 C-bits in that sub-frame are set to 1, when operating in M13 mode and Serial mode.
	6	STFTGEN	**Stuff Timing Generator Enable:** When set to 1, the $\overline{TCG}$ output of the timing generator will include the stuff bit locations when operating in M13 mode and Serial mode.
	5	FORCEFEBE	**Force FEBE Error:** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a far end block error (FEBE) by setting C10, C11, C12 to 0 in the next available DS3 frame when operating in the C-bit parity mode. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	4	FORCEPP	**Force P-Bit Parity Error:** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a P-bit error by inverting both P-bits in the next available DS3 frame. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	3	FORCECP	**Force C-Bit Parity Error:** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a C-bit parity error (C7, C8 and C9 inverted) in the next available DS3 frame when operating in the C-bit parity mode. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	2	TSTCNTR	**Test Counter:** This bit should be set to 0.
	1	EXZEN	**Excessive Zeros Enable:** When set to 1, the $\overline{EXZ}$ events are counted in the CVEXZ counter.
	0	CVEN	**Coding Violation Counter Enable:** Setting this bit to 1 disables the $\overline{FORCECP}$, $\overline{FORCEPP}$ and $\overline{FORCEFEBE}$ input pins from performing their original force error functions and allows these functions to be performed instead by setting to 1 bits 3, 4 and 5 of this register. The $\overline{FORCECP}$ input pin is then defined as the CV (coding violation) input pin and the $\overline{FORCEPP}$ input pin as the $\overline{EXZ}$ (excessive zeros) input pin to the CVEXZ 16-bit counter in the registers at Addresses 12H and 13H.

PACKAGE INFORMATION

The DS3F device is packaged in a 68-pin plastic leaded chip carrier (PLCC) suitable for socket or surface mounting, as shown in Figure 18.



Note: All dimensions are shown in inches and are nominal unless otherwise indicated.

Figure 18. DS3F TXC-03401B 68-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-03401-BIPL	68-pin plastic leaded chip carrier

RELATED PRODUCTS

TXC-02020 (02021), ART (ARTE) VLSI Device (Advanced DS3/STS-1 Receiver/Transmitter). Performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface. The ARTE is an extended-feature version of the ART, in a larger package.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03303, M13E VLSI Device. Extended feature version of the TXC-03301 (M13).

TXC-05101C, HDLC VLSI Device (HDLC Controller). Provides an interface to packet. Performs flag generation/detection, zero insertion/deletion, abort detection and byte framing.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

TXC-20153D, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog to digital interface serving B3ZS encoded DS3 signals.

TXC-21005, DS3F/XBERT Evaluation Board. A complete, ready-to-use test system that demonstrates the functions and features of the DS3F VLSI device. Includes on-board microprocessor, RS-232 interface, XBERT, and MS-DOS compatible PC software for control and monitor.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331

Tel: 800-7014333 (In U.S.A.)
Tel: 908-981-0060
Fax: 908-981-9667

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated DS3F Data Sheet that have significant differences relative to the previous and now superseded DS3F TXC-03401B Data Sheet:

Updated DS3F Data Sheet: *PRELIMINARY* Edition 3A, March 1997

Previous DS3F Data Sheet: *PRODUCT PREVIEW* Edition 1, July 1995

The page numbers indicated below of this updated data sheet include changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed status to PRELIMINARY, changed edition number and date.
1	Added two items near end of Features list.
2	Updated Table of Contents and List of Figures.
3	Modified Figure 1. Added information on N and E modes.
4	Modified the first, fourth, fifth and sixth paragraphs.
6	Changed Pin 66 from XNC to XSC/XNC and pin 61 from $\overline{\text{FORCFEBE}}$ to $\overline{\text{FORCEFEBE}}$ in Figure 2.
7	Made change to Type column for D3TD.
8	Made changes to Name/Function column for $\overline{\text{XFSI}}$ and XCK.
9	Made changes to Symbol, Type and Name/Function columns for Pin 66. Made changes to Name/Function column for Pins 47 and 52.
11	Made changes to Name/Function column for STUFC.
12	Changed "falling" to "rising" for D3RC edge in Name/Function column for $\overline{\text{EXZCNT}}$ and CVCNT. Changed Symbol for Pin 61 to $\overline{\text{FORCEFEBE}}$.
14	Made changes in the three tables, including reductions in ratings for supply voltage and DC input voltage.
15	Reduced maximum input leakage current for TTLp and changed the note.
16	Deleted Output Parameters For CMOS2mA table.
17	Modified the paragraph. Added timing for $\overline{\text{EXZCNT}}$ and CVCNT to Figure 3.
18	Changed Min and Max columns for Symbol t_{OD}.
19	Modified RNIBn waveform in Figure 5.
20	Changed Min, Typ and Max columns for Symbol t_{OD}.
21	Added RNIB3 waveform to Figure 7 and added a note below the waveforms.
22	Made changes to Figure 8 and the table.

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23	Made changes to second CXDCC waveform in Figure 9.
24	Made changes to Figure 10, added notes below the waveforms, and added CRD set up time to table.
25	Made changes to Figure 11, added a note below the waveforms, and added XSC output delay to the table.
26	Changed Min and Max columns for Symbol t_{OD} in Figure 13, and changed Min column for Symbol $t_{PW(2)}$.
27	Made changes to Figure 14 waveforms, table and notes.
28-29	Modified $t_{W(3)}$ in $\overline{SEL}$ waveform and changed Parameter column for Symbol $t_{W(3)}$. Changed Min column for Symbol $t_{W(4)}$.
31	Made change to Symbol column for Bit 2 of Address 0C (C21).
32	Made changes to Description column for Bits 6, 5 and 4 of Address 00.
33	Made changes to Description column for Bits 7, 3 and 2 of Address 01.
34	Made change to last paragraph of Description column for Addresses 02 and 03 (Address 02H).
36	Changed Description column for Address 06.
37	Made changes to Description column for Bits 7, 6, 1 and 0 of Address 08.
38-39	Made changes to Description column for Bits 7, 6, 3 and 2 of Address 0C and Bits 5-0 of Address 0D ('first word' in last-but-one sentence). Made change to Symbol column for Bit 2 of Address 0C.
40	Made changes to Description column for Bits 4 and 0 of Address 0E.
45	Updated Standards Documentation Sources.
46	Updated List of Data Sheet Changes.
51	Updated Documentation Update Registration Form.