50/100MHz, 6-Bit Monolithic ADC's

AD5010KD/AD6020KD

FEATURES

Scan Frequency to 100MHz (AD5010KD)
Low 450mW Power Dissipation
±1/4LSB Linearity
ECL Logic Compatible
No Sample & Hold Required
Overflow Output for Extended Resolution

APPLICATIONS

Video Data Conversion
High Speed Data Acquisition
Radar/Sonar Data Conversion

GENERAL DESCRIPTION

The AD6020KD is a 6-bit monolithic analog-to-digital converter capable of performing at conversion rates up to 50MHz. Packaged in a 16-pin hermetic ceramic dip, it performs true 6-bit A/D conversions with ±1/4LSB max linearity error. The extremely high scanning rate is ideal for video and other data acquisition applications that require digitizing of high frequency signals.

For other applications where even higher speed can be traded off against price, the AD5010KD represents the latest in state-of-the-art monolithic technology. Capable of performing true 6-bit conversions at rates up to 100MHz, the AD5010KD represents the ultimate in conversion speeds currently available in monolithic form. It is ideal for applications such as radar and X-ray equipment, medical systems such as ultra-sound, and measurement instruments such as digital storage oscilloscopes and transient recorders.

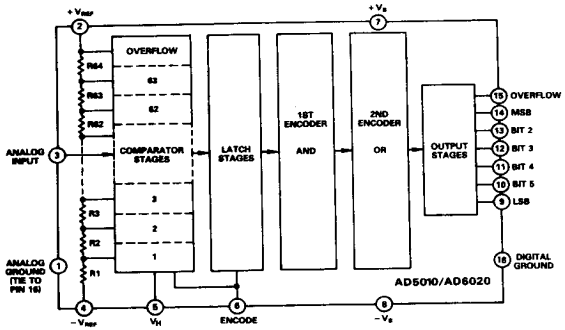
A unique feature of both units is the overflow output which allows the user to cascade two units to achieve 7-bit resolution, or four units for 8-bit resolution. Another salient feature is the power dissipation specification of only 450mW which is almost 50% less than the nearest competitive product.

THEORY OF OPERATION

The low linearity and ultra-high conversion rates are achieved by combining ECL logic and the parallel or "Flash" method of conversion. This consists of 64 comparator stages whose reference is set from an external voltage reference by a linear resistive voltage divider (see Block Diagram). The results of the comparator stage are then transferred to the 64 latches.

This comparison and transfer occurs when the encode input is at a "low" logic level. When the encode input goes "high", the latches are separated from the comparators and their contents encoded and brought to the output as a digital word. Since the latches are separated from the comparators during this cycle, the analog signal is always present at the input which eliminates the need for a track-and-hold.

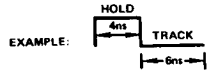
AD5010KD/AD6020KD FUNCTIONAL BLOCK DIAGRAM



TYPICAL CIRCUIT FOR 6-BIT OPERATION

The circuit of Figure 1 may be used for either the AD6020KD or AD5010KD. When the analog input equals or exceeds $+V_{REF}$, the overflow bit goes "high" and bits 1–6 go "low". If it is desirable to latch all bits high in this condition configure a 10197 (or equivalent) as shown to hold all bits including the overflow "high", as long as A_{IN} equals or exceeds $+V_{REF}$.

For applications at lower scan frequencies (below ≈ 50MHz), hysteresis control (V_H) may be left floating. At frequencies approaching 100MHz, the use of a nonsymmetrical encode pulse may enhance the overall performance.



Because of the high frequencies involved, attention to detail becomes most important (circuit layout, power supply decoupling, timing, etc.). A large ground plane is mandatory.

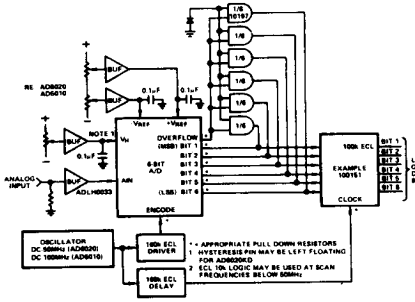


Figure 1. Typical Circuit – 6-Bit Operation

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SPECIFICATIONS (typical at +25°C and nominal power supply unless otherwise noted)

PARAMETER	AD6020KD MIN	AD6020KD TYP	AD6020KD MAX	AD5010KD MIN	AD5010KD TYP	AD5010KD MAX	UNITS
RESOLUTION		6			•		Bits
INPUT RANGE			±2.5			•	V
LINEARITY ERROR[1]		1/4[2]			1/4[3]		LSB
INPUT CURRENT							
Hold	-10		+10	•		•	μA
Sample[4]		200	800		150	500	μA
INPUT CAPACITANCE[5]		35			•		pF
DYNAMIC							
Conversion Time		20			10		ns
Aperture Time (T_D)		2			•		ns
Aperture Jitter (Uncertainty)		25			•		ps
T_{ENCODE}	15	8		10	5		ns
Scan Frequency		50			100		MHz
Signal Transition Time							
T_{HLQ}		12	20		8	15	ns
T_{LHQ}		12	20		8	15	ns
Recovery Time (1V Step)		5			•		ns
DATA INPUTS							
Logic Compatibility		ECL			•		
Encode							
Logic Level "1"	-1.1	-0.9	-0.6	•	•	•	V
Logic Level "0"	-2.0	-1.7	-1.5	•	•	•	V
Encode Current "1"	5	30	100	•	•	•	μA
Encode Current "0"	5	30	100	•	•	•	μA
REFERENCE INPUTS							
Positive Reference Voltage	-2.0		+2.5	•		•	V
Negative Reference Voltage	-2.5		+2.0	•		•	V
Reference Resistance	96	128	256	•	•	195	Ω
DATA OUTPUTS[6]							
Logic Compatibility		ECL			•		
Logic Level "1"	-1.1	-0.9	-0.7	•	•	•	V
Logic Level "0"	-2.0	-1.7	-1.5	•	•	•	V
POWER SUPPLY REQUIREMENTS							
$+V_S$	4.75	5.0	5.25	•	•	•	V
$-V_S$	-5.46	-5.2	-4.94	•	•	•	V
CURRENT[7]							
$+V_S$ = +5.0V		30	60		•	•	mA
$-V_S$ = -5.2V		55	80		•	•	mA
POWER DISSIPATION		450			•		mW
TEMPERATURE RANGE (Ambient)	0		70	•		•	°C

NOTES
[1] Measured with 2V, 1kHz triangular input.
[2] 15ns T_{ENCODE}.
[3] 10ns T_{ENCODE}.
[4] Measured with AIN = $+V_{REF}$ in sample mode.
[5] Measured with AIN > $-V_{REF}$.
[6] Data Outputs terminated to -2V through 100Ω.
[7] $-V_{REF} \leq AIN \leq +V_{REF}$.
*Specifications same as AD6020.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter		Lower Limit	Upper Limit	Unit
Supply Voltage	$+V_S$	-0.3	+6.0	Volts
	$-V_S$	-6.0	+0.3	Volts
Input Voltages				
AIN $+V_{REF}$ $-V_{REF}$		-3.0	+3.0	Volts
Encode		$-V_S$	0.0	Volts
Hysterisis Control		>0	+3.0	Volts
Temperature				
Operating		0	+70	°C
Storage		-55	+125	°C
Lead, Soldering (10sec)			+300	°C

EVALUATION BOARD

An evaluation board is available. The AD6020KD/PCB contains everything needed to verify the performance of the ADC. The effects of changes in the analog input, $+V_{REF}$, $-V_{REF}$, hysteresis, and encode can be monitored by an on-board DAC. Each card is shipped with the ADC and a complete instruction set. The only user requirement is to supply power to the board: +5 ±2% @ 100mA; -5.2 ±2% @ 2000mA; ±15 ±1% @ 100mA each.

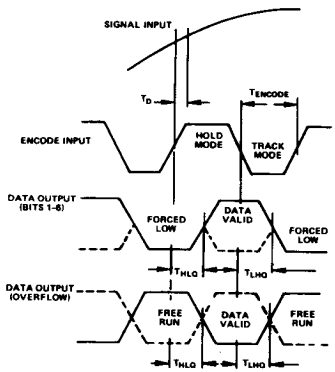
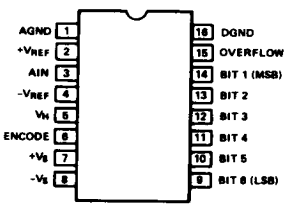


Figure 3. Timing Diagram

ORDERING INFORMATION

Model	Description	Package Option[1]
AD6020KD	6 Bits, 50MHz	D16B
AD6020KD/PCB	AD6020KD ADC with Evaluation Board	D16B
AD5010KD	6 Bits, 100MHz	D16B

[1] See Section 19 for package outline information.



PIN	SYMBOL	FUNCTION
1	GND	GROUND (ANALOG)
2	$+V_{REF}$	POSITIVE VOLTAGE REFERENCE
3	AIN	ANALOG INPUT
4	$-V_{REF}$	NEGATIVE VOLTAGE REFERENCE
5	V_H	HYSTERESIS CONTROL
6	ENCODE	ENCODE INPUT
7	$+V_S$	POSITIVE SUPPLY VOLTAGE
8	$-V_S$	NEGATIVE SUPPLY VOLTAGE
9	BIT 6	LEAST SIGNIFICANT BIT OUTPUT
10	BIT 5	BIT 5 OUTPUT
11	BIT 4	BIT 4 OUTPUT
12	BIT 3	BIT 3 OUTPUT
13	BIT 2	BIT 2 OUTPUT
14	BIT 1	MOST SIGNIFICANT BIT OUTPUT
15	OVERFLOW	OVERFLOW OUTPUT
16	GND	GROUND (DIGITAL)

NOTE: GND PINS (1, 16) SHOULD BE TIED TOGETHER AS CLOSE TO THE UNIT AS POSSIBLE.

Figure 2. Outline & Pin Designations

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