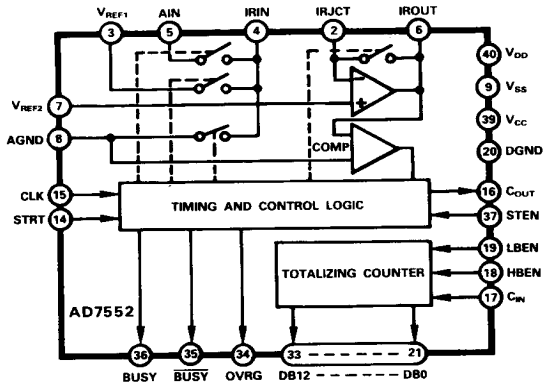
CMOS 12-Bit Plus Sign Monolithic A/D Converter

AD7552

FEATURES
12-Bit Binary with Polarity and Overrange
Accuracy ±1LSB
Microprocessor Compatible
Ratiometric Operation
Low Power Dissipation
Low Cost

AD7552 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7552 is a 12-bit plus sign and overrange monolithic CMOS analog to digital converter. The "Quad Slope" conversion algorithm (Analog Devices patent No. 3872466) converts any offset voltages due to the integrator, comparator etc. to a digital number and subsequently reduces the total system drift error to a second order effect.

The AD7552 parallel output data lines have three-state logic and are microprocessor compatible. Separate enable lines control the lower eight LSBs (low byte enable) and the five MSBs (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N40A)

[1]See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The output data (12-bits plus sign) may be directly accessed under control of two byte enable signals for a simple parallel bus interface. The overrange and converter busy signals are accessed by a status enable signal.
2. The AD7552 conversion time is approximately 160ms with a 250kHz clock.
3. Serial count out available for isolated A/D conversion via opto-isolators.
4. A conversion start can be controlled by an externally applied signal or, with the addition of a capacitor, the converter can be made to self start.
5. For most applications, the AD7552 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

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SPECIFICATIONS (V_{DD} = +12V, V_{CC} = +5V, V_{SS} = −5V, V_{REF1} = +4.25V unless otherwise noted)[1]

Parameter	T_A = +25°C	T_A = 0 to +70°C	Units	Conditions/Comments
ACCURACY				
Resolution	12-bits plus sign	12-bits plus sign		Binary 2's complement coding
Accuracy of Reading (Including Noise)	±1	±1	Counts max	f_{CLK} = 250kHz, R1 = 1.8MΩ, C1 = 0.01μF 95% of conversions meet this specification
Noise (Flicker)	±1	±1	Counts max	From nominal reading, not exceeded 95% of time
	±2	±2	Counts max	From nominal reading, not exceeded 99% of time
ANALOG INPUTS				
AIN (pin 5) Input Resistance[2]	R1	R1	MΩ min	R1 is the external integrating resistor
V_{REF1} (pin 3) Input Resistance[2]	R1	R1	MΩmin	connected between IROUT and IRJCT
V_{REF2} (pin 7) Leakage Current	1	10	nA typ	
DIGITAL INPUTS				
CIN (pin 17), HBEN (pin 18), LBEN (pin 19), STEN (pin 37)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+2.4	+2.4	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}, I_{IH}	1	1	μA max	V_{CC} = +5V to +12V
START (pin 14)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V to V_{DD}
V_{IH}	+3.0	+3.0	V min	
I_{IL}	−5/−50	−5/−50	μA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OL}
I_{IH}	+0.5/+2.0	+0.5/+2.0	mA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OH}
CLOCK (pin 15)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+3.0	+3.0	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}	−0.1/−1.0	−0.1/−1.0	mA typ/max	V_{IN} = V_{IL}; V_{CC} = +5V to +12V
I_{IH}	+0.1/+1.0	+0.1/+1.0	mA typ/max	V_{IN} = V_{IH}; V_{CC} = +5V to +12V
DIGITAL OUTPUTS				
C_{OUT} (pin 16), OVRG (pin 34) $\overline{BUSY}$ (pin 35), BUSY (pin 36) and DB0–DB12 (pins 21–33)				
V_{OL}	+0.8	+0.8	V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OH}	+4.0	+4.0	V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OL}	+1.2	+1.2	V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OH}	+10.8	+10.8	V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance per Pin[3]	5	5	pF typ	Outputs in high impedance state
Leakage per Pin	1	1	μA max	Outputs in high impedance state
DYNAMIC PERFORMANCE				
Conversion Time	160	160	ms typ	R1 = 1.8MΩ, C1 = 0.01μF, f_{CLK} = 250kHz
Propagation Delays[3]				
STEN to BUSY, $\overline{BUSY}$, or OVRG	400	700	ns max	Typically 250ns at +25°C (see next page) Flag load = 20pF
LBEN to DB0–DB7	300	500	ns max	Typically 160ns at +25°C (see next page) DB0–DB7 load = 20pF
HBEN to DB8–DB12	300	500	ns max	Typically 160ns at +25°C (see next page) DB8–DB12 load = 20pF
STRT Pulse Width	300	500	ns min	Typically 220ns at +25°C V_{IN} (STRT) = 0 to +3V
POWER SUPPLIES				
V_{DD}	+10/+12	+10/+12	V min/max	
V_{SS}	−5/−12	−5/−12	V min/max	
V_{CC}	+5/V_{DD}	+5/V_{DD}	V min/max	
I_{DD}	0.8/2	0.8/2	mA typ/max	STRT (pin 14) held HIGH,
I_{SS}	0.3/2	0.3/2	mA typ/max	digital outputs floating.
I_{CC}	0.1/1	0.1/1	mA typ/max	V_{CC} = +5V
	0.5/2	0.5/2	mA typ/max	V_{CC} = +12V

NOTES

[1]Full scale voltage = ±V_{REF1} ÷ 2.125. For V_{REF1} = +4.25V FS voltage is ±2.00V.

[2]The equivalent input circuit is the integrator resistor R1 in series with a voltage source V_{REF2} = V_{REF}/1 ÷ 2, see Figure 1.

[3]Guaranteed but not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +14V
V_{DD} to DGND	0V, +14V
V_{SS} to AGND	0V, −14V
V_{SS} to DGND	0V, −14V
AGND to DGND	0V, +14V
V_{CC} to DGND	0V, V_{DD}
V_{REF1}	V_{SS}, V_{DD}
V_{REF2}	AGND, V_{DD}
AIN	V_{SS}, V_{DD}
IRIN	V_{SS}, V_{DD}
IRJCT	AGND, V_{DD}
IROUT	V_{SS}, V_{DD}
Digital Input Voltage	
HBEN, LBEN, STEN, C_{IN}	DGND, (DGND +27V)
CLK, START	DGND, V_{DD}
Digital Output Voltage	
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT}	DGND, V_{CC}
Operating Temperature Range	0 to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (Package)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

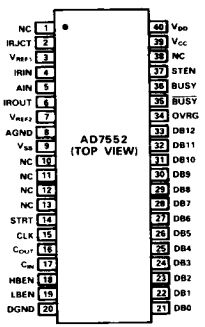
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

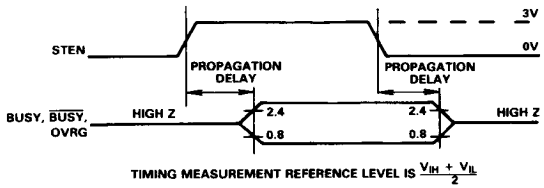
ORDERING INFORMATION

Price Model	Temperature Range	Package[1]
AD7552KN	0 to +70°C	Plastic–N40A

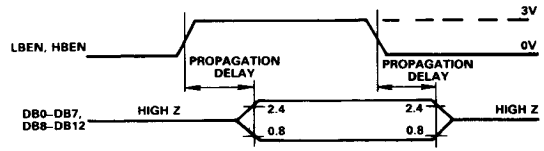
[1]See Section 19 for package outline information.

PIN CONFIGURATION





STEN to BUSY, $\overline{BUSY}$, or OVRG Propagation Delays



LBEN to DB0–DB7, HBEN to DB8–DB12 Propagation Delays

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input (normally +4.25 volts).
4	IRIN	IntegratoR INput. External integrating resistor R1 is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Full scale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input. V_{REF2} is normally obtained by a potential divider circuit as shown in Figure 3.
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (−5V to −12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1", the AD7552's digital logic is set up and BUSY is latched "high". When STRT returns "low", conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 300 nanoseconds to ensure proper set-up of the AD7552 internal logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[\frac{AIN}{V_{REF1}} 2.125 + 1\right] 4096$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8–DB12 data outputs. When HBEN is "low", the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRanGe indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG. When STEN is "high", the three outputs are enabled.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters. The AD7552 utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table I), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.

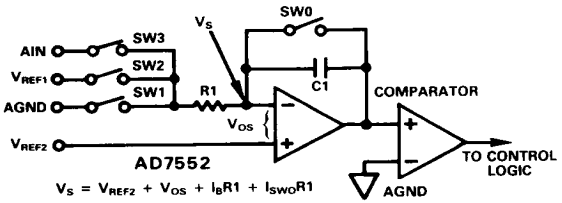


Figure 1. Simplified Quad Slope Integrator Circuit

Phase	Input Voltage	Integration Time
1	AGND–V_S	$t_1 = K_1t$
2	V_{REF1}–V_S	$t_2 = (K_1 + n)t$
3	AIN–V_S	$t_3 = (2K_1 - n)t$
4	V_{REF1}–V_S	$t_4 = (K_3 - 2K_1 + n - 2N)t$

Table I. Integrator Equivalent Input Voltages and Integration Times

where:

t = The CLK period
n = System error count
K_1 = A fixed count equal to 4352 counts
K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
K_3 = A fixed count equal to 25600 counts
N = Digital output count corresponding to the analog input voltage, AIN

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right)\cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal term}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right)\cdot\left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right]\cdot 2K_1}_{\text{error term}}$$

where:

AGND = Voltage at AD7552 pin 8 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

α is an error term equal to $\dfrac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally $\alpha = 0$ when $V_S = 0.5V_{REF1}$.

NOTE:
$V_S = V_{REF2} + V_{OS} + I_B R_1 + I_{SWO} R_1$

WHERE:
$V_{REF2} = 0.5V_{REF1}$ if no error is present
V_{OS} = Offset voltage of integrator amplifier
$I_B R1$ = Equivalent integrator amplifier offset voltage due to bias current of integrator amplifier
$I_{SWO} R1$ = Equivalent integrator amplifier offset voltage due to SW0 leakage current.

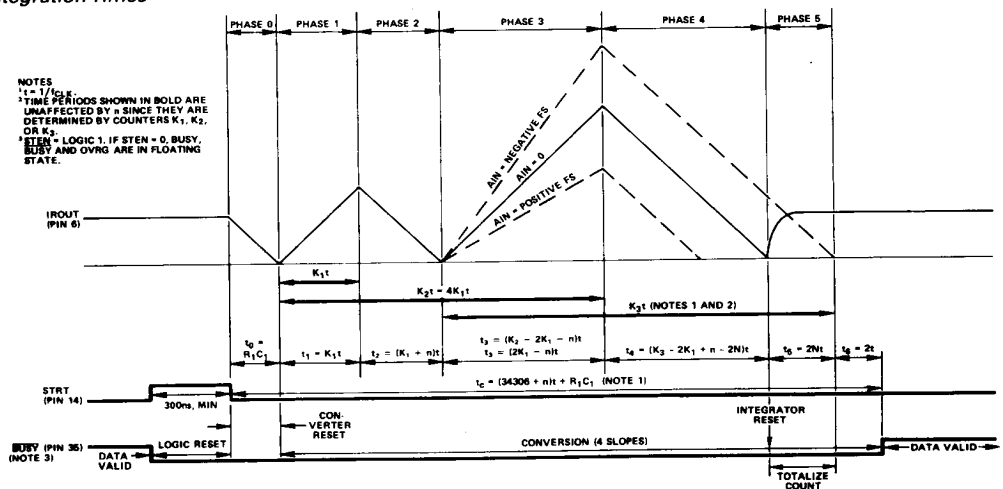


Figure 2. Quad Slope Timing Diagram

The ideal case assumes:

$AGND = 0V$

$V_S = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{FS} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

FS = full scale input voltage = $\frac{V_{REF1}}{2.125}$

Equation 1 shows that only α and AGND generate error terms. Errors due to $\alpha \neq 0$ are strongly reduced because of the α^2 term in equation 1. Errors due to AGND $\neq 0$ will, however, have a first order effect on the system performance. Great care should be taken in any circuit layout to minimize or eliminate ground loops between AGND and signal ground. A recommended grounding system is shown in Figure 5.

OUTPUT CODING

The parallel output (DB0–DB12) of the AD7552 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)			
		OVRG	DB12	DB11	DB0
+Overrange	8191	1	0	1111 1111 1111	
+(FS−1LSB)	8191	0	0	1111 1111 1111	
+1LSB	4097	0	0	0000 0000 0001	
0	4096	0	0	0000 0000 0000	
−1LSB	4095	0	1	1111 1111 1111	
−(FS−1LSB)	1	0	1	0000 0000 0001	
−FS	0	0	1	0000 0000 0000	
−Overrange	0	1	1	0000 0000 0000	

NOTES:
[1] $FS = \frac{V_{REF1}}{2.125}$; 1 Least Significant Bit (LSB) = $FS(2^{-12})$
[2] N = number of counts at C_{OUT} pin
[3] C_{OUT} strapped to C_{IN}; LBEN and HBEN = Logic 1

Table II. Output Coding (Bipolar 2's Complement)

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 3 explain the selection of the various component values required for proper operation.

1. **Determination of V_{REF1}**
   The reference voltage V_{REF1} and the full scale input voltage FS are related by

   $$V_{REF1} = 2.125\ (FS)$$

   V_{REF1} must be positive for proper operation. A typical value of V_{REF1} is +4.25V. An AD584 may be used to provide the reference.

2. **Selection of Integrator Components R1 and C1**
   The integrator time constant should be approximately equal to

   $$R1\,C1 \approx \frac{V_{REF1}(9 \times 10^3)}{f_{CLK}(V_{DD} - 4V)}$$

   The integrating capacitor C1 should be a low leakage, low dielectric absorption type such as Teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C1 should be connected to the output of the integrating amplifier and not to its summing junction.

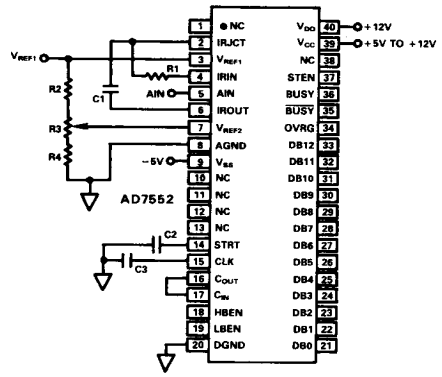


Figure 3. AD7552 Operational Diagram

Improper selection of the integrator time constant (time constant = R1 C1) may cause excessive noise due to the integrator output swing being too low, or may cause nonlinear operation if the integrator output attempts to exceed the rated output voltage of the amplifier.

3. **Determining Conversion Time**
   As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

   $$t_{CONVERT} = t_{STRT} + \frac{34306}{f_{CLK}} + R1\,C1$$

   where:
   t_{STRT} = STRT pulse duration.
   R_1C_1 = Integrator Time Constant.
   f_{CLK} = CLK Frequency at pin 15.

4. **External or Auto STRT Operation**
   The STRT pin can be driven externally, or with the addition of C2, made to self-start.

   The value of C2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

   $t_{DAV} \approx (1.17 \times 10^6\Omega)\ C2 + 20\mu s$

   When first applying power to the AD7552, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation. See APPLICATIONS HINTS No. 5.

5. **Internal Clock Operation**
   The CLK input, pin 15, should normally be driven from an external crystal frequency source, particularly if operation above 250kHz is required. However, for noncritical applications an internal clock oscillator can be activated when a capacitor is connected from pin 15 to DGND. Figure 4 shows a typical curve of clock frequency versus capacitance, C3. Due to process variations the actual operating frequency for a given value of C3 can vary from device to device by up to 100%. Consequently it may be necessary to "tune" C3 to provide the correct clock frequency for a given V_{REF1} and R1C1. For proper operation the clock frequency should be limited to 250kHz. Conversion speeds of up to 80ms can be obtained by increasing the clock frequency to 500kHz. However the flicker due to noise will also increase. See APPLICATIONS HINTS No. 8.

6. **Initial Calibration**
   Trim R3 (Figure 3) so that the voltage on pin 2 (IRJCT) equals $1/2V_{REF1} \pm 0.6\%$. During this trim and measurement cycle apply a logic HIGH to pin 14 (STRT). This will prevent the AD7552 from executing a conversion.

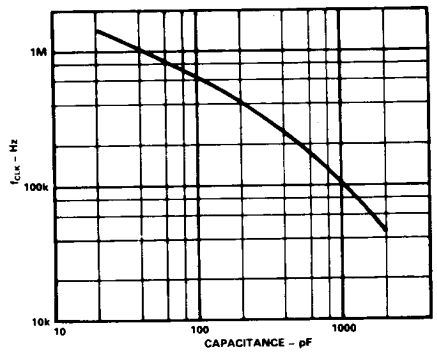


Figure 4. Internal Clock Frequency vs. C3

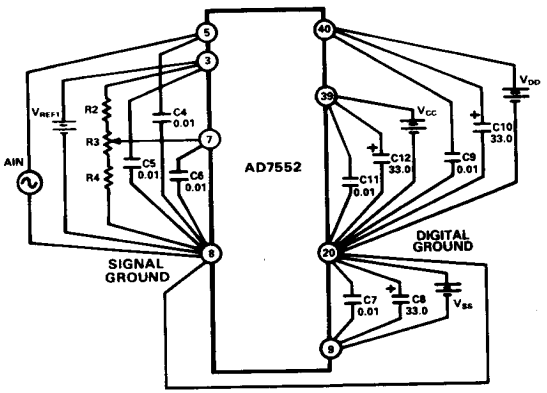
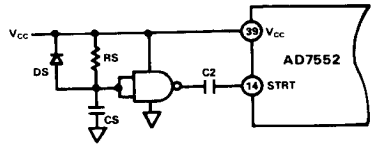


Figure 5. Recommended Grounding System

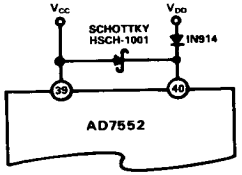
APPLICATIONS HINTS

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01μF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R1 and C1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying STEN to the 1 state and driving HBEN and LBEN with $\overline{BUSY}$. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.
5. To avoid the requirement of providing a positive STRT pulse on power-up to initiate the auto start operation, the following circuit may be used.

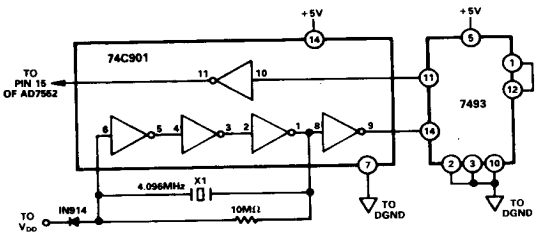


The output of the open collector NAND gate is initially high on power-up. When the charging voltage on CS reaches the input threshold level of the NAND gate, the output goes low and remains low to allow the AD7552 to self start.

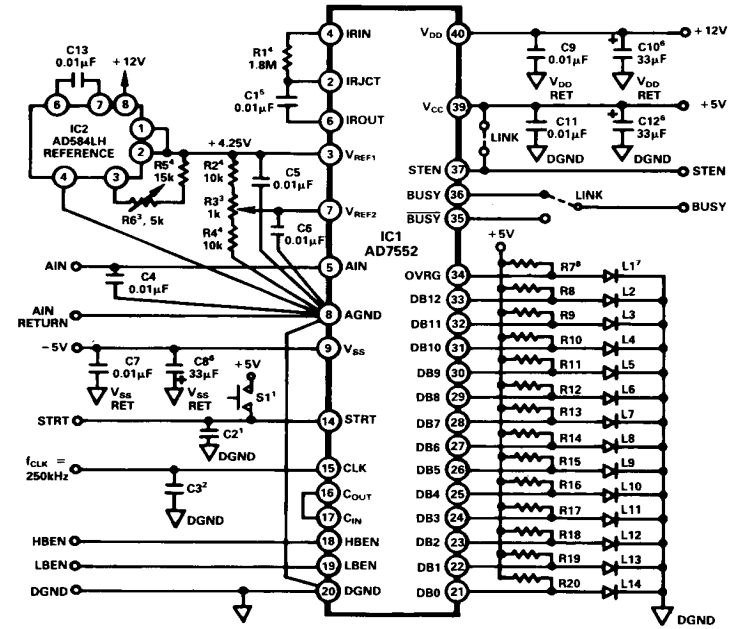
6. Under no circumstances should V_{CC} exceed V_{DD} especially during power-up and power-down. In cases where this situation could occur the following diode protection scheme is recommended.



7. Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects across the integrating capacitor. The user is cautioned to ensure that the manufacturing process for circuits using the AD7552 does not allow such films to remain after assembly. Otherwise the accuracy and noise performance of the device will be affected.
8. A suggested crystal oscillator circuit is shown below for use with a V_{CC} of +5V. It uses a standard 4.096MHz crystal which is divided down by 16 to produce a clock frequency of 256kHz.



9. A printed circuit layout for an evaluation board is shown in Figure 8a and 8b. Figure 6 shows the circuit diagram for this evaluation board with component values for f_{CLK} = 250kHz, V_{REF1} = +4.25V operation. Figure 7 shows the component overlay for Figure 8a. Note that either $\overline{BUSY}$ (pin 35) or BUSY (pin 36) is available at the edge connector via a wire link. Note also that STEN (pin 37) may be tied high via a wire link.



NOTES:
[1]S1 IS A PUSHBUTTON SWITCH TO INITIATE AUTO-START OPERATION. S1 AND C2 ARE NOT REQUIRED FOR EXTERNAL START OPERATION.
[2]C3 IS NOT REQUIRED FOR EXTERNAL CLOCK OPERATION.
[3]FOR CALIBRATION HOLD PIN 14 (STRT) HIGH. ADJUST R6 UNTIL THE VOLTAGE ON PIN 3 (V_{REF1}) IS 4.250V. ADJUST R3 UNTIL THE VOLTAGE ON PIN 2 (IRJCT) IS 2.125 ±0.025V.
[4]R1, R2, R4, R5 1% TOLERANCE, METAL FILM.
[5]C1 MUST BE A LOW LEAKAGE, LOW DIELECTRIC ABSORPTION TYPE SUCH AS TEFLON, POLYSTYRENE OR POLYPROPYLENE.
[6]C8, C10 AND C12 ARE SOLID ELECTROLYTE TANTULUM CAPACITORS.
[7]L1 – L14 ARE LEDS, MONSANTO MV55 OR EQUIVALENT.
[8]R7 – R13 AND R14 – R20 ARE PROVIDED BY TWO THICK-FILM. RESISTOR NETWORKS, EACH IN AN 8-PIN SINGLE-IN-LINE PACKAGE. SUITABLE NETWORKS AVAILABLE FROM BECKMAN INSTRUMENTS INC., 2500 HARBOR BOULEVARD, FULLTERTON, CA 92634, MODEL NO. 764–1–4K7.

Figure 6. Evaluation Board Circuit with Component Values for f_{CLK} = 250kHz, V_{REF1} = +4.25V

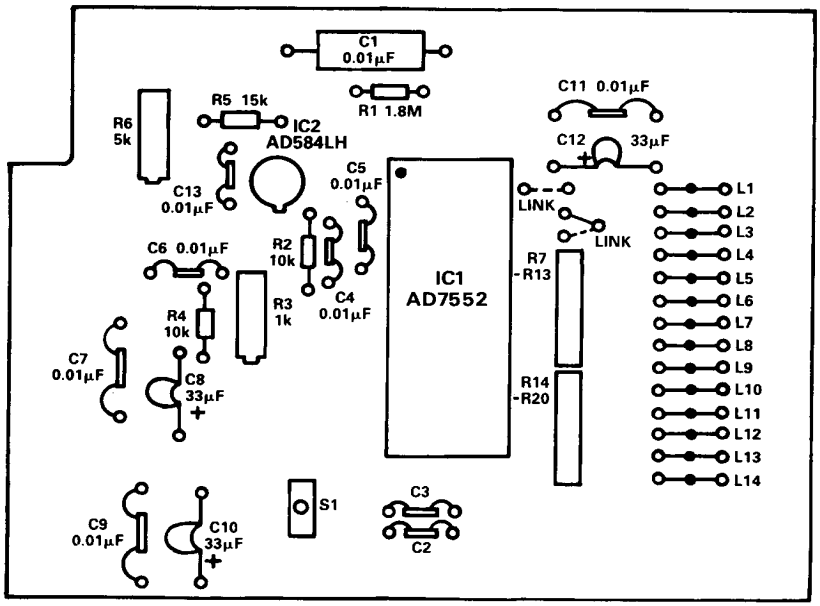


Figure 7. Component Overlay for Figure 8a

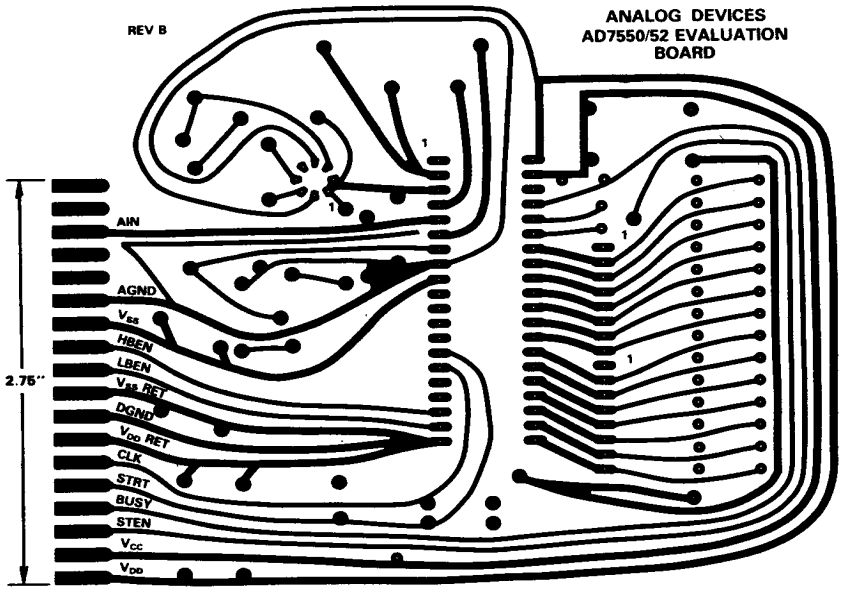


Figure 8a. Component Side

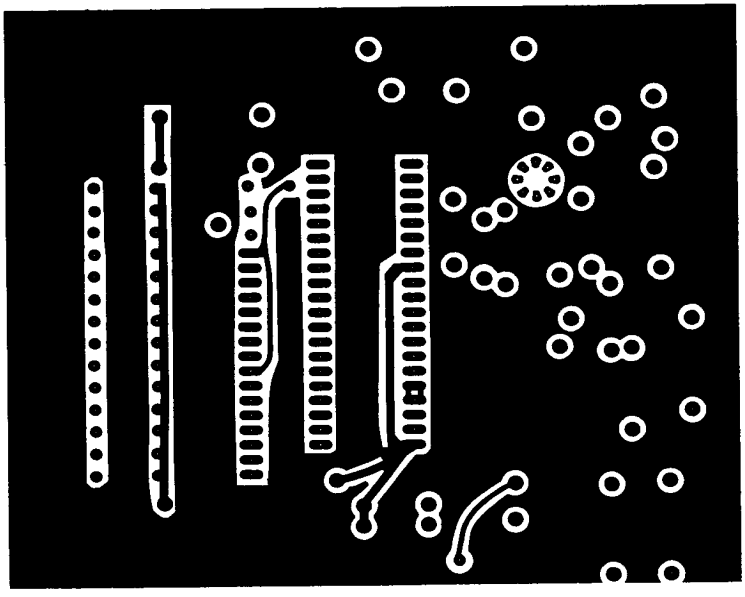


Figure 8b. Foil Side

OBTAINING SIGN-MAGNITUDE 4 DIGIT BCD CODING FROM THE AD7552

Referring to Figure 9 when a convert start pulse is received the four decade presettable up/down counter is loaded with the value 4096. The low level on the up/down count input (Q of X1 = 0) places the CD4029 counters into the count down mode. The contents of the four decade BCD counter are decremented each time a pulse is detected on C_{OUT}. The number of pulses appearing on C_{OUT} is related to both the magnitude and the polarity of the input voltage. If the counter reaches the all 0's state, the flip-flop (X1) is set, placing a high level signal on the up/down count input. The counter will now count up on succeeding C_{OUT} pulses.

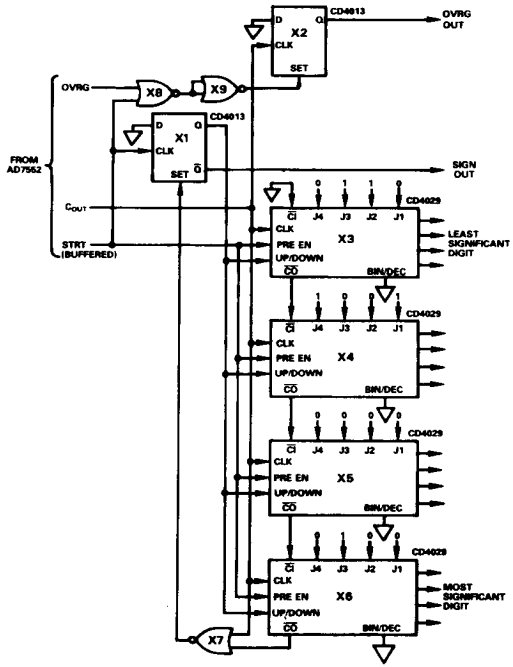


Figure 9. Sign-Magnitude BCD Conversion Circuitry

Analog Input[2]	N[3]	SIGN-MAGNITUDE BCD CODING[1] OVRG	Sign	Digit 4	Digit 3	Digit 2	Digit 1
+ Overrange	8191	1	0	4	0	9	5
+ FS − 1LSB	8191	0	0	4	0	9	5
+ 1LSB	4097	0	0	0	0	0	1
0+	4096	0	0	0	0	0	0
0−	4096	0	1	0	0	0	0
− 1LSB	4095	0	1	0	0	0	1
−(FS − 1LSB)	1	0	1	4	0	9	5
− FS	0	1	1	4	0	9	6
− Overrange	0	1	1	4	0	9	6

NOTES
[1]Using circuit of Figure 9.
[2]FS = $V_{REF1} \div 2.125$; 1 Least Significant Bit (LSB) = $FS(2^{-12})$.
[3]N = number of counts at C_{OUT} pin.

Table III. Sign-Magnitude BCD Coding

Referring to Table III no counts occur on C_{OUT} when the input voltage is either overrange or equal to −FS. Since the most negative value which can be represented in sign-magnitude coding is −(FS − 1LSB) whereas in two's complement coding it is −FS, the X2 flip-flop of Figure 9 ensures that the OVRG output is high if either AIN is overrange or AIN = −FS. Note that there are two codes for zero analog input. This is the result of gating the carry out signal from X6 with the input clock signal C_{OUT}. As mentioned previously, the number of counts at the C_{OUT} terminal is obtained by an internal divide-by-two counter stage. Depending on whether the number of counts to this divide-by-two was odd or even C_{OUT} can remain in either a high or a low state at the end of phase 4. If AIN is negative and less than 1/2LSB (AIN = 0−), C_{OUT} is high after outputting 4096 counts thus preventing the sign flag from changing. If AIN is positive and less than 1/2LSB, C_{OUT} is low after outputting 4096 counts allowing the sign flag to change. If the carry out signal from X6 is directly connected back to X1, then the code for AIN = 0− vanishes leaving one code (the 0 + one) for 0V.

This circuit may be used to provide direct readout of analog input voltage with proper scaling of the reference voltage and serial output C_{OUT}. For instance, dividing C_{OUT} by two and adjusting V_{REF1} = +4.352V gives a FS voltage of 2.048V which will be displayed directly.

Analog Input[2]	N[3]	SIGN-MAGNITUDE CODING[1] OVRG	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
+ Overrange	8191	1	0	1	1	1	1	1	1	1	1	1	1	1	1
+ FS − 1LSB	8191	0	0	1	1	1	1	1	1	1	1	1	1	1	1
+ 1LSB	4097	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	4096	0	0	0	0	0	0	0	0	0	0	0	0	0	0
− 1LSB	4095	0	1	0	0	0	0	0	0	0	0	0	0	0	1
−(FS − 1LSB)	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
− FS	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
− Overrange		1	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTES
[1]Using circuit of Figure 10.
[2]FS = $V_{REF1} \div 2.125$; 1 Least Significant Bit (LSB) = $FS(2^{-12})$.
[3]N = number of counts at C_{OUT} pin.

Table IV. Sign-Magnitude Binary Coding

OBTAINING SIGN-MAGNITUDE BINARY CODING FROM THE AD7552

The circuit of Figure 10 converts the two's complement coding from the AD7552 into sign-magnitude coding. It does this by complementing the AD7552 data and adding 1LSB whenever DB12 is high. In sign-magnitude coding the most negative value that can be represented is −(FS − 1LSB); in two's complement coding it is −FS. The OR gate in Figure 10 ensures only valid output codes are produced (see Table IV). Note that there is only one code for zero scale.

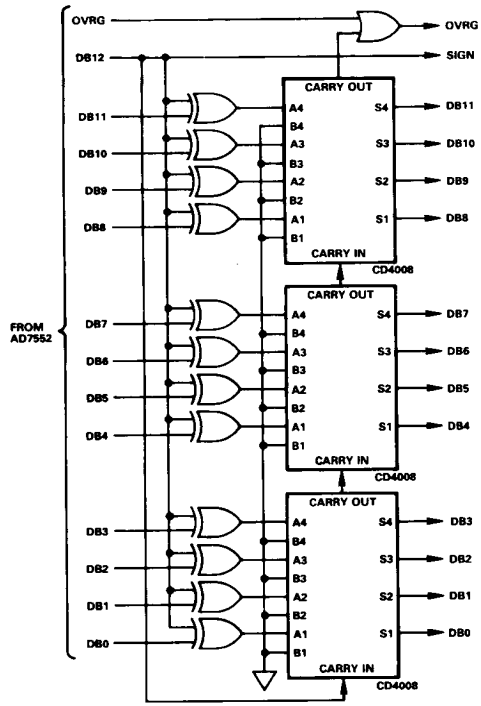


Figure 10. Sign-Magnitude Binary Conversion Circuitry

MICROPROCESSOR INTERFACING

The three-state output capability of the AD7552 allows the multiplexing of the data and status lines onto a single 8-bit wide bus. Figure 11 shows the AD7552 directly interfaced to the 6800 with convert start, data read, etc., all under program control. Note that the two status lines OVRG and BUSY are connected to the data bus in the MSB and LSB positions so that they can easily be interrogated by reading the status word to the microprocessor accumulator, rotating right or left through carry and then checking the carry flag.

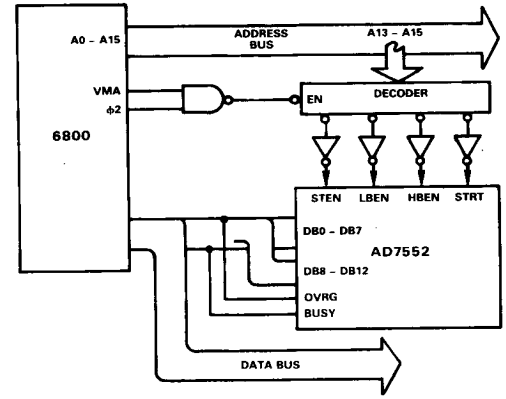


Figure 11. AD7552-6800 Direct Interface

Care should be taken when using fast-access memory or operating at high temperatures to ensure that the AD7552 output drivers relinquish the data bus in time to avoid any possible bus conflict with the following instruction. In any situation where bus conflict is likely, the interfacing technique of Figure 12 is recommended.

10

AD7552–8085A INTERFACE

Figure 12 shows the AD7552 interfaced to the 8085A. In this application the two status lines share the data bus with the data high byte (DB8–DB12) since the STEN and HBEN inputs are driven simultaneously from a single decoded address. The 8282 data latch which buffers the AD7552 three state drivers from the microprocessor bus ensures that the bus is relinquished promptly at the end of a data read instruction.

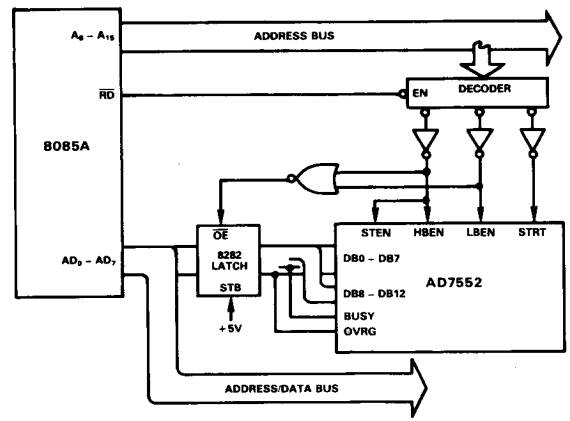


Figure 12. AD7552-8085A Direct Interface

CONTINUOUS CONVERSION MODE

Figure 13 shows the AD7552 connected for continuous conversion. The conversion STRT signal is synchronized with the ALE signal of the 8085A. The $\overline{BUSY}$ signal is used to update the 8-bit data latches at a time when the microprocessor is not attempting a read operation. Thus the AD7552 appears to the microprocessor as memory which can be read at any time although scrambled data can result if a data update occurs between reading the high byte and low byte data. One method of avoiding this is to read data only after an update has occurred. The microprocessor can be interrupted to perform a data read by tying the AD7552 STRT input to one of the RST inputs on the 8085A.

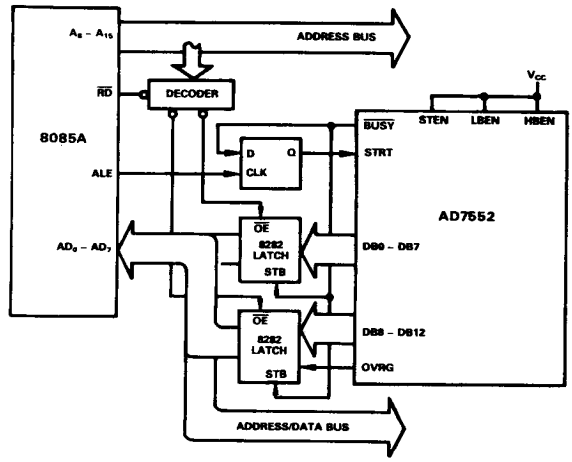


Figure 13. AD7552 in Continous Conversion Mode

OPTO–ISOLATED SERIAL INTERFACE

Figure 14 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign and/or overrange information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{BUSY}$ is used to cause an interrupt on the RST 7.5 line. The value ($2^{14} - C_{OUT}$) in the 8155 timer should now be read. When $\overline{BUSY}$ returns low, the 8155 counter is reset to FF_H. The falling edge of $\overline{BUSY}$ also latches the sign and overrange data into port B. This is indicated by a rising edge on BF (buffer full) which can be used to call the 8085 CPU to read port B data.

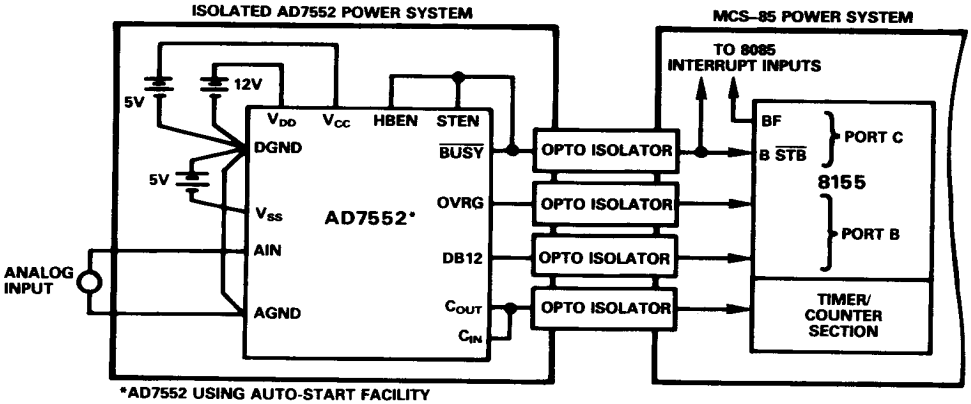


Figure 14. Optically Isolated Serial AD7552/MCS-85 Interface