ICM7240/ICM7250
ICM7260
Programmable Timer

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICM8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for the time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

FEATURES

- **Replaces 8240/50/60, 2240 in Most Applications**
- **Timing From Microseconds to Days**
- **May Be Used As Fixed or Programmable Counter**
- **Programmable With Standard Thumbwheel Switches**
- **Select Output Count From**
  1_{RC} to 255_{RC} (ICM7240)
  1_{RC} to 99_{RC} (ICM7250)
  1_{RC} to 59_{RC} (ICM7260)
- **Monostable or Astable Operation**
- **Low Supply Current: 115μA @ 5 Volts**
- **Wide Supply Voltage Range: 2-16 Volts**
- **Cascadeable**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-25°C to +85°C	16 Lead CERDIP
ICM7250IJE	-25°C to +85°C	16 Lead CERDIP
ICM7260IJE	-25°C to +85°C	16 Lead CERDIP
ICM7240/D	—	DICE**
ICM7250/D	—	DICE**
ICM7260/D	—	DICE**

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

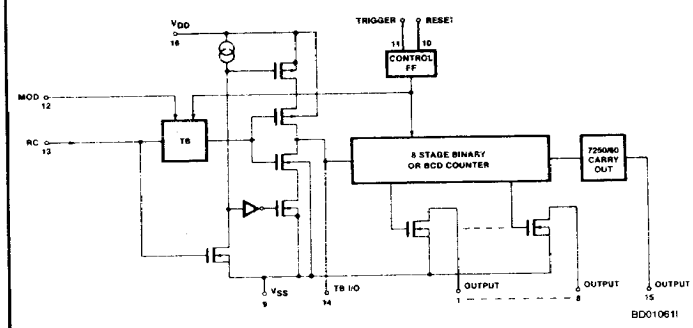


Figure 1: Functional Diagram
ICM7240/50/60

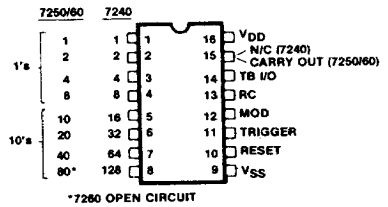


Figure 2: Pin Configuration
(Outline dwg JE)
ICM7240/7250/7260

203403-002

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}–V_{SS}) 18V
Input Voltage[1]
Terminals 10,11,12,13,14 ..... V_{SS} −0.3V to V_{DD} + 0.3V
Maximum continuous output
current (each output) 50mA

Power Dissipation[2] 200mW
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.

2. Derate at −2mW/°C above 25°C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

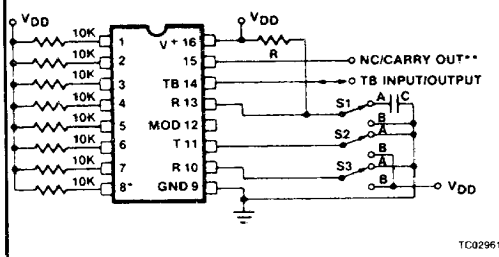
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = +25°C, R = 10kΩ, V_{DD} = 0V C = 0.1μF, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Guaranteed Supply Voltage (V_{DD}-V_{SS})		2		16	V
I_{DD}	Supply Current	Reset Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to GND		125 300 120 125	 800 600	μA μA μA μA
	Timing Accuracy			5		%
$\Delta f/\Delta T$	RC Oscillator Frequency Temperature Drift	(Exclusive of RC Drift)		250		ppm/°C
V_{OTB}	Time Base Output Voltage	I_{SOURCE} = 100μA I_{SINK} = 1.0mA		3.50 0.40		V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{MOD}	Mod Voltage Level	V_{DD} = 5V V_{DD} = 15V		3.5 11.0		V V
V_{TRIG}	Trigger Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.6 3.5	2.0 4.5	V V
V_{RST}	Reset Input Voltage	V_{DD} = 5V V_{DD} = 15V		1.3 2.7	2.0 4.0	V V
f_t	Max Count Toggle Rate 7240	V_{DD} = 2V V_{DD} = 5V V_{DD} = 15V } Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}	2	1 6 13		MHz MHz MHz
f_t	Max Counter Toggle Rate 7250, 7260	V_{DD} = 5V (Counter/Divider Mode)	2	5		MHz
f_t	Max Count Toggle Rate 7240, 7250, 7260	Programmed Timer — Divider Mode			100	kHz
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output V_{DD} = 5V, I_{OUT} = 3.2 mA		0.22	0.4	V
I_{OLK}	Output Leakage Current	V_{DD} = 5V, per Output			1	μA
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	$V_{DD} \leq$ 5.5V $V_{DD} \leq$ 16V	1K 1K		12M 12M	Ω Ω

NOTE: 1. For Design only, not 100% tested.

Note: All typical values have been guaranteed by characterization and are not tested.



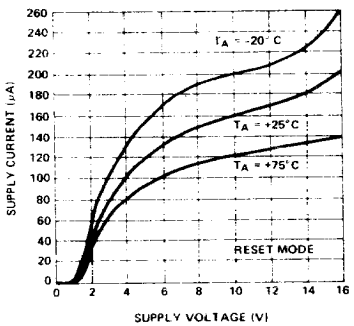
S1-A = RC RUN S2-A = INACTIVE S3-A = INACTIVE
B = T.B. INPUT RUN B = TRIGGER B = RESET

NOTE: S1-B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
** TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

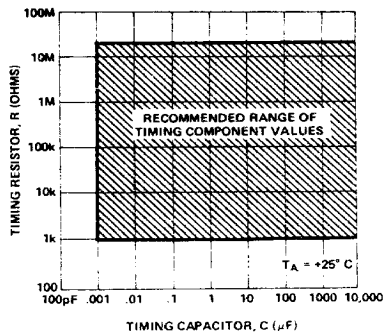
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

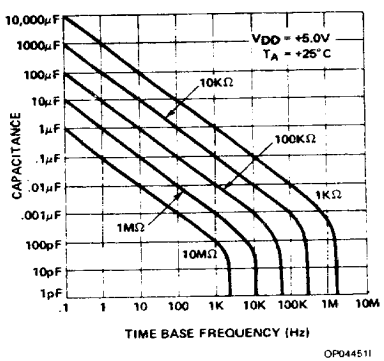
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



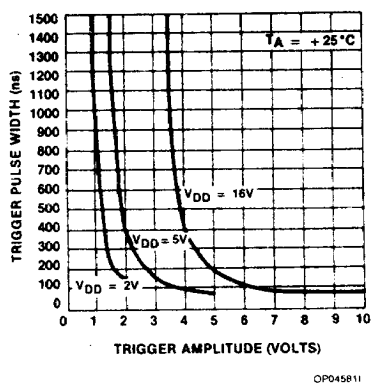
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



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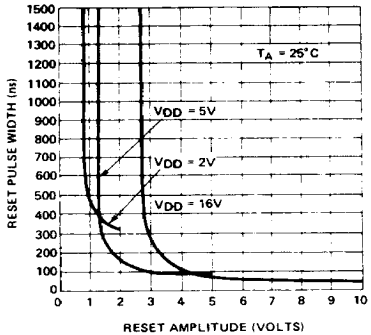
Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

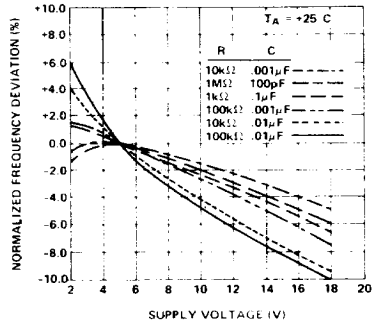
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



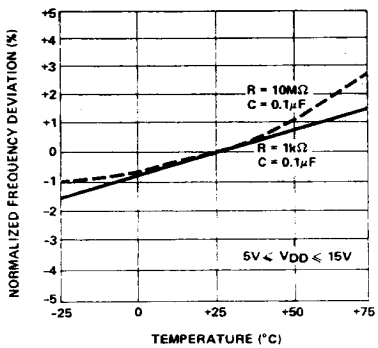
OP04461

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



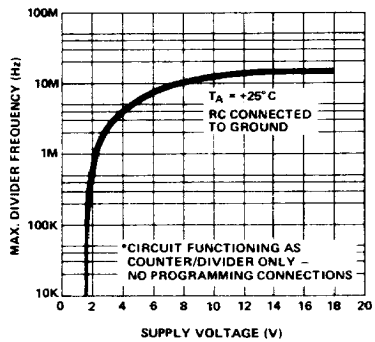
OP04490

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



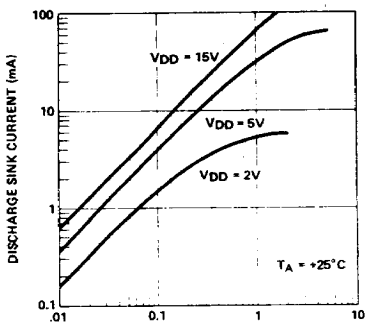
OPD4501

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



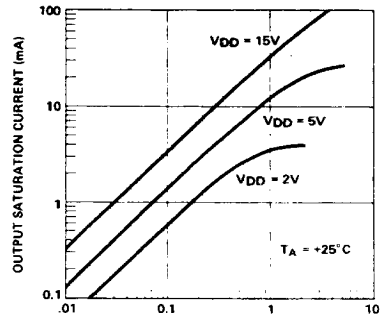
OP04520

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OP04531

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



OP04511

Note: All typical values have been guaranteed by characterization and are not tested.

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of V_{DD}–V_{SS}, generating a timing waveform with period t, equal to 1_{RC}. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive level is applied to RESET. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carry-out is also HIGH. Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

In most timing applications, one or more of the counter outputs are connected back to RESET the circuit will start timing when a TRIGGER is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the RESET (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

DESCRIPTION OF PIN FUNCTIONS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 4). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

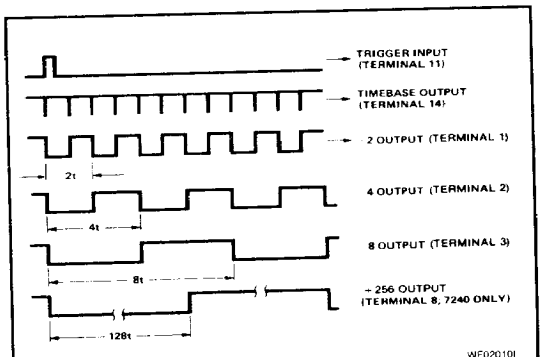


Figure 4: Timing Diagram for ICM7240/50/60

V_{SS} (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by a positive level applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period, t, of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

TIMEBASE INPUT/OUTPUT PIN (PIN 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input if the RC pin is connected to V_{SS}.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

CARRY OUTPUT (PIN 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive level on the RESET terminal (if TRIGGER is low), a positive level on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. (See Figure 6.)

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈5mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_0 would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins, 1, 5, and 6 were shorted to the output bus, the total time delay would be $t_0 = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$1t \leq t_0 \leq 255t$ (7240)

$1t \leq t_0 \leq 99t$ (7250)

$1t \leq t_0 \leq 59t$ (7260)

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Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

Note that for the 7250 and 7260, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see Figure 5. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 5, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 4, which shows the phase relations between the counter outputs. Figure 6 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1_{RC} to 99_{RC}. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999_{RC}. For a ICM7260, there are standard BCD thumbwheel switches for the 0 through 5 digit (twelve position 0 to 5 repeated).

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100kHz or less (with V_{DD} equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the RESET/TRIGGER signal.

b. There must be a delay of the positive going output to RESET, (pin 10) and TRIGGER (pin 11). The RESET signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The TRIGGER overrides RESET.

The delay between TRIGGER and RESET is generated by the signal RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter ripple delays can be as long as 2μs (5 volt supply), and the delay between RESET and TRIGGER should be at least 2μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 7 and 8.

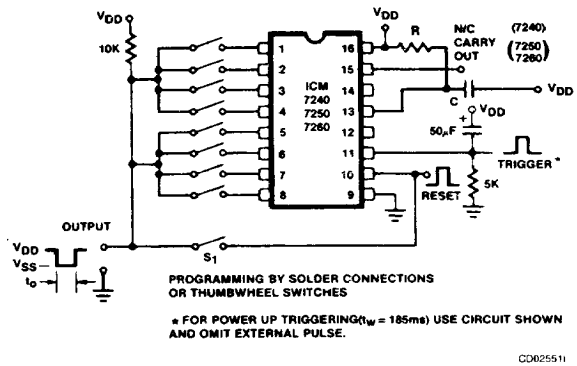

Figure 5: Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

Note: All typical values have been guaranteed by characterization and are not tested.

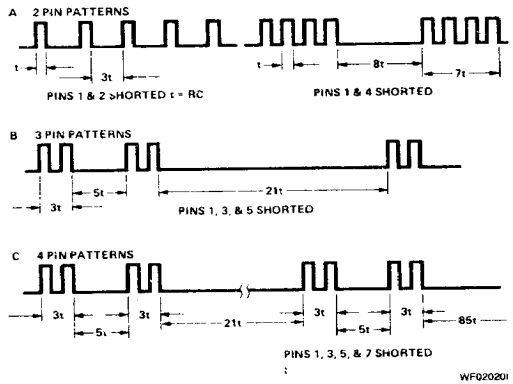

Figure 6: Pulse Patterns Obtained by Shorting Various Counter Outputs

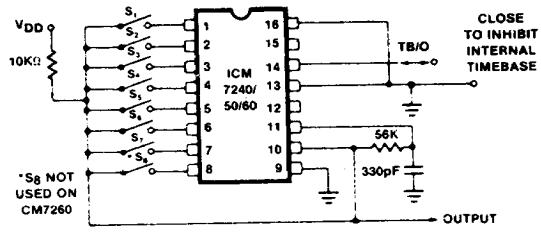

Figure 7: Programming the Counter Section of the ICM7240/50/60

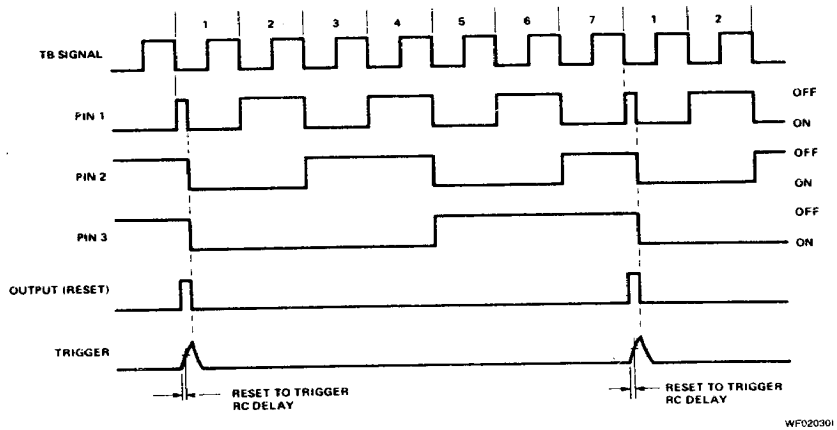

Figure 8: Waveforms for Programming the Counter Section

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7240/ICM7250/ICM7260

APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time $\leq 1\mu s$); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

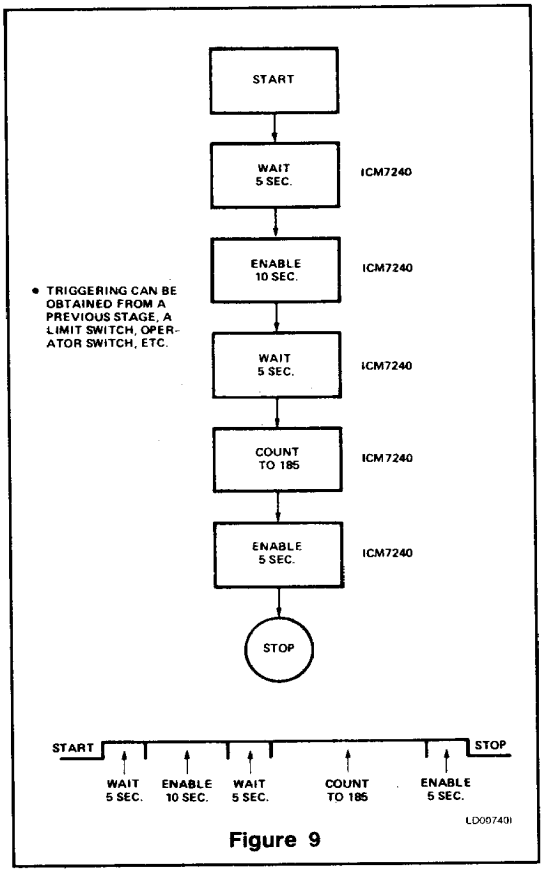

Figure 9

Note: All typical values have been guaranteed by characterization and are not tested.

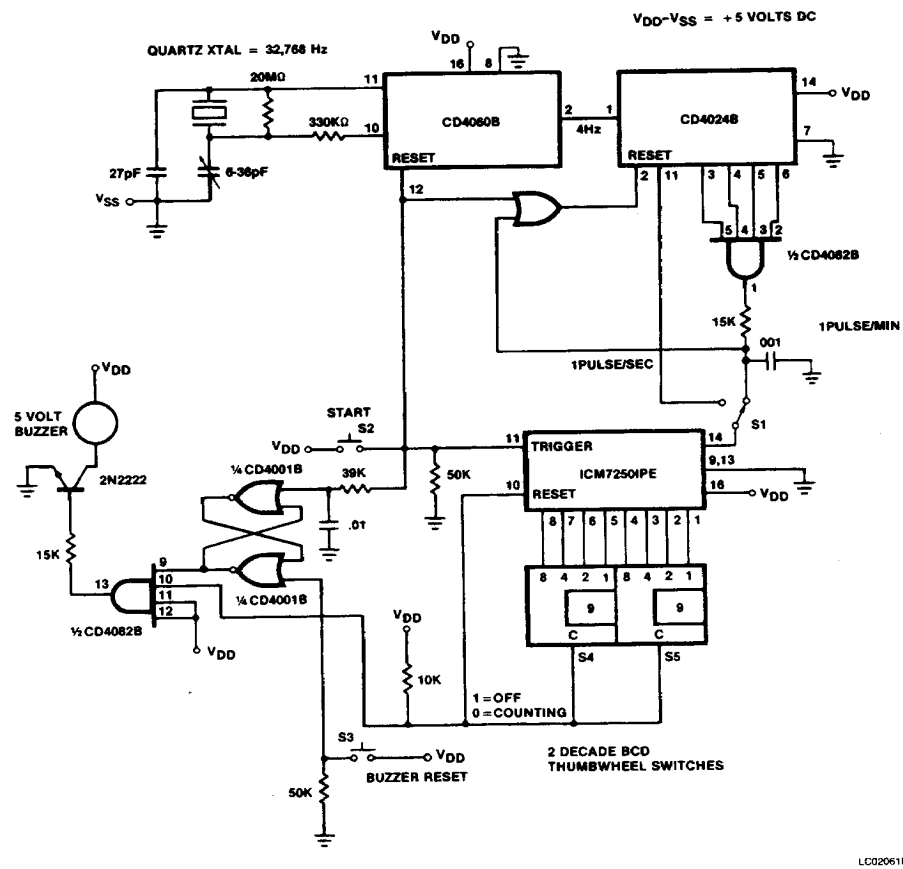

Figure 10

CMOS PRECISION PROGRAMMABLE 0–99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown in Figure 10, the timer can accurately measure preselected time intervals of 0–99 seconds or 0–99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0–99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the preprogrammed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

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Note: All typical values have been guaranteed by characterization and are not tested.

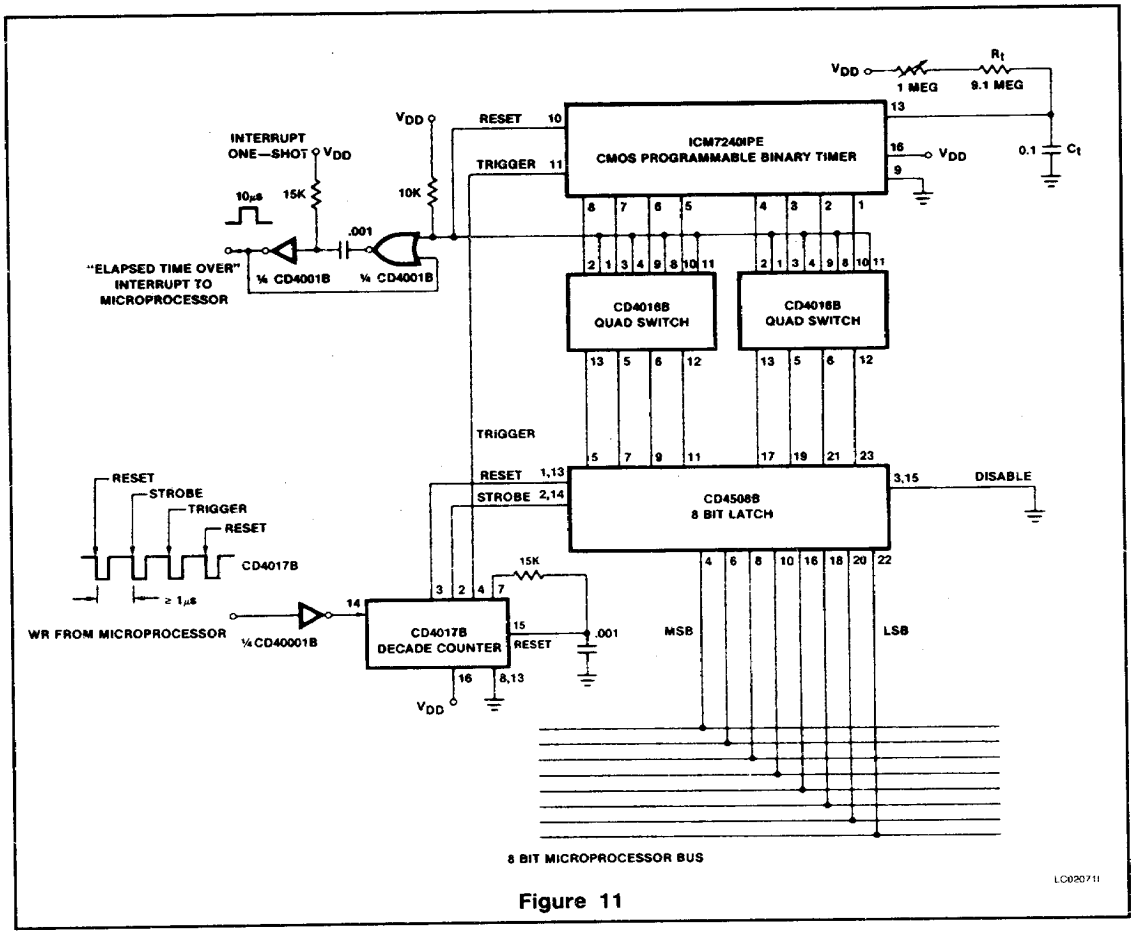

Figure 11

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown in Figure 11, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four $\overline{\text{WRITE}}$ pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately 10MΩ and capacitor of 0.1μF, the time base of the ICM7240 is one second. Thus, a time of 1–255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

Note: All typical values have been guaranteed by characterization and are not tested.