

## FEATURES

- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- $\pm 1\%$  Bandgap Reference
- Undervoltage Lockout
- External Shutdown
- Dual 200mA Totem Pole Outputs
- Double Pulse Suppression
- Soft-Start Capability

## APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

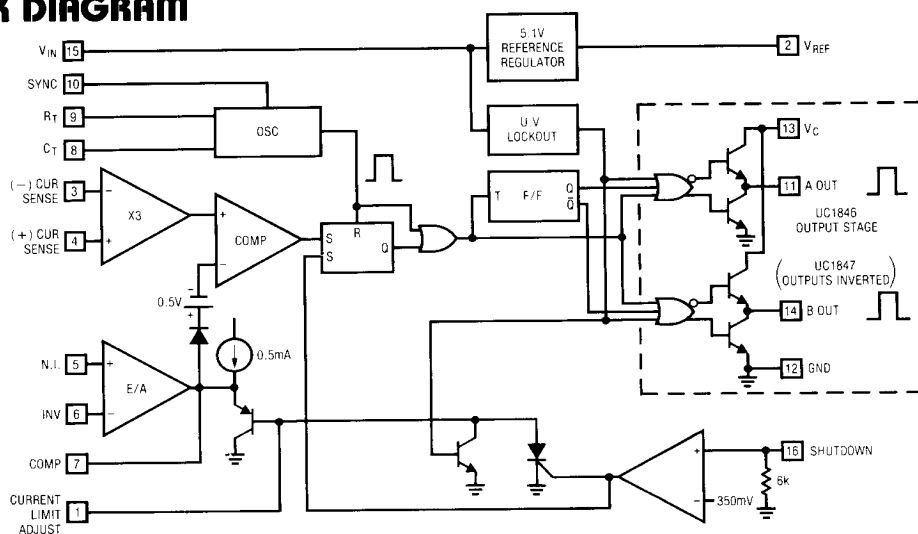
## DESCRIPTION

The UC1846 family of control ICs contains all necessary circuitry to implement fixed frequency, fixed output voltage, current mode control schemes. Current mode control loops are easy to design and compensate, and provide superior transient line regulation, inherent pulse-by-pulse current limiting, and automatic symmetry correction for push-pull converters. In addition, the UC1846 has built-in undervoltage lockout with hysteresis to prevent oscillations near the threshold, soft-start capability, and can be shut down instantaneously by an external logic level. Internal logic prevents double-pulsing and output overlap.

The oscillator circuitry of the UC1846 allows the user to adjust output deadtime as well as frequency and also provides a bidirectional sync pin to allow paralleling power modules.

Both the internal error amplifier and current sense amplifiers operate over a wide common-mode range to allow design flexibility. The dual outputs provide active pull up/pull down, ideal for driving bipolar or FET switches. The internal reference regulator provides excellent stability for changes in line, load, and temperature. The UC1846 outputs are low in the off state while the UC1847 outputs are high in the off state.

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Supply Voltage (Pin 15)..... +40V  
 Collector Supply Voltage (Pin 13)..... +40V  
 Output Current, Source or Sink (Pins 11, 14)..... 500mA  
 Analog Inputs (Pins 3, 4, 5, 6, 16)..... -0.3V to + $V_{IN}$   
 Reference Output Current (Pin 2)..... -30mA  
 Sync Output Current (Pin 10)..... -5mA  
 Error Amplifier Output Current (Pin 7)..... -5mA  
 Soft Start Sink Current (Pin 1)..... 50mA  
 Oscillator Charging Current (Pin 9)..... 5mA  
 Operating Temperature Range

UC1846/1847..... -55°C to +125°C

UC3846/3847..... 0°C to 70°C

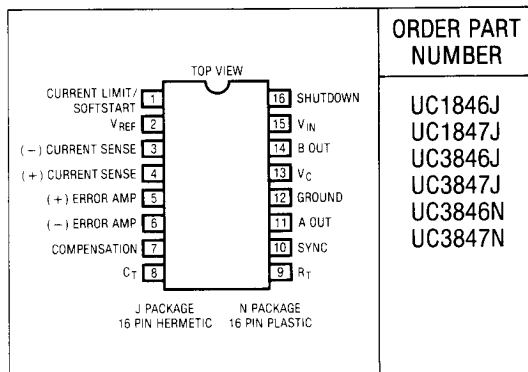
Power Dissipation at  $T_A = 25^\circ\text{C}$  (Note 2)..... 1000mWPower Dissipation at  $T_C = 25^\circ\text{C}$  (Note 3)..... 2000mW

Thermal Resistance, Junction to Ambient..... 100°C/W

Thermal Resistance, Junction to Case..... 60°C/W

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (Soldering, 10sec)..... +300°C

**PACKAGE/ORDER INFORMATION****ELECTRICAL CHARACTERISTICS** (Note 4)

PARAMETER	CONDITIONS	UC1846/UC1847			UC3846/UC3847			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Reference Voltage									
Output Voltage	T <sub>J</sub> = 25°C, I <sub>O</sub> = 1mA		5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V <sub>IN</sub> = 8V to 40V	●		5	20		5	20	mV
Load Regulation	I <sub>L</sub> = 1mA to 10mA	●		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 5)	●		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 5)	●	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T <sub>J</sub> = 25°C (Note 5)			100			100		μV
Long Term Stability	T <sub>J</sub> = 125°C, 1000Hrs., (Note 5)			5			5		mV
Short Circuit Output Current	V <sub>REF</sub> = 0V	●	-10	-45		-10	-45		mA
Oscillator Section									
Initial Accuracy	T <sub>J</sub> = 25°C		39	43	47	39	43	47	kHz
Voltage Accuracy	V <sub>IN</sub> = 8V to 40V	●		-1	±2		-1	±2	%
Temperature Stability	Over Operating Range (Note 5)	●		-1			-1		%
Sync Output High Level		●	3.9	4.35		3.9	4.35		V
Sync Output Low Level		●		2.5	2.7		2.5	2.7	V
Sync Input High Level	Pin 8 = 0V	●	3.9	3.0		3.9	3.0		V
Sync Input Low Level	Pin 8 = 0V	●		3.0	2.7		3.0	2.7	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	●		0.7	1.5		0.7	1.5	mA
Error Amp Section									
Input Offset Voltage		●		0.5	5		0.5	10	mV
Input Bias Current		●		-0.6	-1		-0.6	-2	μA
Input Offset Current		●		40	250		40	250	nA
Common-Mode Range	V <sub>IN</sub> = 8V to 40V	●	0		V <sub>IN</sub> - 2V	0		V <sub>IN</sub> - 2V	V

**ELECTRICAL CHARACTERISTICS** (Note 4)

PARAMETER	CONDITIONS		UC1846/UC1847			UC3846/UC3847			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Error Amp Section (Cont.)									
Open Loop Voltage Gain	$\Delta V_O = 1.2V$ to $3V$	●	80	105		80	105		dB
Unity Gain Bandwidth		●	0.7	1.0		0.7	1.0		MHz
CMRR	$V_{CM} = 0V$ to $38V$ , $V_{IN} = 40V$	●	75	100		75	100		dB
PSRR	$V_{IN} = 8V$ to $40V$	●	80	105		80	105		dB
Output Sink Current	$V_{ID} = -15mV$ to $-5V$ , $V_{Pin7} = 1V$	●	2	6		2	6		mA
Output Source Current	$V_{ID} = 15mV$ to $5V$ , $V_{Pin7} = 2.5V$	●	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	$R_L$ (Pin 7) = $15k\Omega$	●	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	$R_L$ (Pin 7) = $15k\Omega$	●		0.7	1		0.7	1	V
Current Sense Amplifier Section									
Amplifier Gain	$V_{Pin3} = 0V$ , Pin 1 Open (Notes 6 & 7)	●	2.5	3.0	3.15	2.5	3.0	3.15	V
Maximum Differential Input Signal ( $V_{Pin4} - V_{Pin3}$ )	Pin 1 Open (Note 6) $R_L$ (Pin 7) = $15k\Omega$	●	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{Pin1} = 0.5V$ Pin 7 Open (Note 6)	●		5	25		5	25	mV
CMRR	$V_{CM} = 1V$ to $12V$	●	60	83		60	83		dB
PSRR	$V_{IN} = 8V$ to $40V$	●	60	84		60	84		dB
Input Bias Current	$V_{Pin1} = 0.5V$ , Pin 7 Open (Note 6)	●		-2.5	-10		-2.5	-10	$\mu A$
Input Offset Current	$V_{Pin1} = 0.5V$ , Pin 7 Open (Note 6)	●		0.08	1		0.08	1	$\mu A$
Input Common-Mode Range		●	0		$V_{IN} - 3$	0		$V_{IN} - 3$	V
Delay to Outputs	$T_J = 25^\circ C$ , (Note 5)			200	500		200	500	ns
Current Limit Adjust Section									
Current Limit Offset	$V_{Pin3} = 0V$ $V_{Pin4} = 0V$ , Pin 7 Open (Note 6)	●	0.4	0.5	0.55	0.4	0.5	0.55	V
Input Bias Current	$V_{Pin5} = V_{REF}$ , $V_{Pin6} = 0V$	●		-10	-30		-10	-30	$\mu A$
Shutdown Terminal Section									
Threshold Voltage		●	250	350	400	250	350	400	mV
Input Voltage Range		●	0		$V_{IN}$	0		$V_{IN}$	V
Minimum Latching Current ( $I_{Pin1}$ )	(Note 8)	●	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching ( $I_{Pin1}$ )	(Note 9)	●		1.5	0.8		1.5	0.8	mA
Delay to Outputs	(Note 5), $T_J = 25^\circ C$			300	600		300	600	ns
Output Section									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	$V_C = 40V$ (Note 10)	●			200			200	$\mu A$
Output Low Level	$I_{SINK} = 20mA$	●		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 100mA$	●		0.4	2.1		0.4	2.1	
Output High Level	$I_{SOURCE} = 20mA$	●	13	13.5		13	13.5		V
	$I_{SOURCE} = 100mA$	●	12	13.5		12	13.5		
Rise Time	(Note 5), $C_L = 1nF$ , $T_J = 25^\circ C$			50	300		50	300	ns
Fall Time	(Note 5), $C_L = 1nF$ , $T_J = 25^\circ C$			50	300		50	300	ns
Undervoltage Lockout Section									
Start-Up Threshold		●		7.7	8.0		7.7	8.0	V
Threshold Hysteresis		●		0.75			0.75		V
Total Standby Current									
Supply Current	(Note 11)	●		17	21		17	21	mA

The ● denotes the specifications that apply over the full operating temperature range.

**Note 1:** All voltages are with respect to Ground, pin 12. Currents are positive into, negative out of the specified terminal.

**Note 2:** Derate at 10mW/°C for  $T_A$  above 50°C.

**Note 3:** Derate at 16mW/°C for  $T_C$  above 25°C.

**Note 4:** Unless otherwise stated  $V_{IN} = 15V$ ,  $R_T = 10k$ ,  $C_T = 4.7nF$ .

**Note 5:** These parameters, although guaranteed over the recommended operating conditions are not 100% tested in production.

**Note 6:** Parameter measured at trip point of latch with  $V_{Pin5} = V_{REF}$ ,  $V_{Pin6} = 0V$ .

**Note 7:** Amplifier gain defined as

$$G = \frac{\Delta V_{Pin7}}{\Delta V_{Pin4}}, \Delta V_{Pin4} = 0V \text{ to } 1.0V$$

**Note 8:** Current into pin 1 guaranteed to latch circuit in shutdown state.

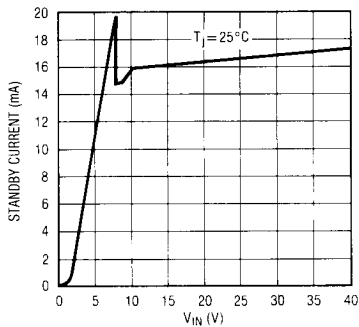
**Note 9:** Current into pin 1 guaranteed not to latch circuit in shutdown state.

**Note 10:** Applies to UC1846/3846 only due to polarity of outputs.

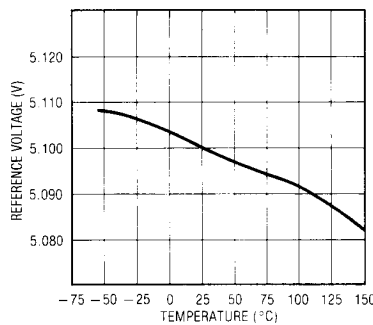
**Note 11:** Standby current does not include oscillator charging current, error and current limit dividers, and the outputs are open circuit.

## TYPICAL PERFORMANCE CHARACTERISTICS

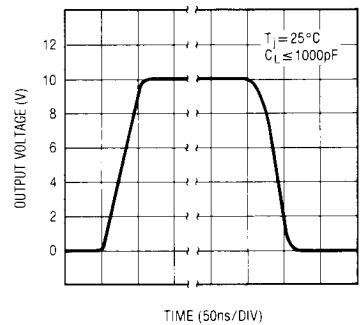
Standby Current vs  $V_{IN}$



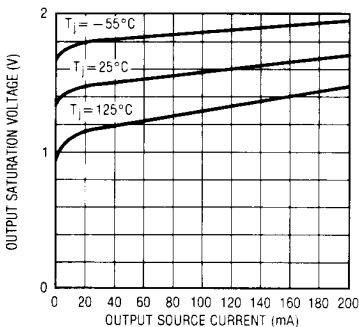
Reference Voltage vs Temperature



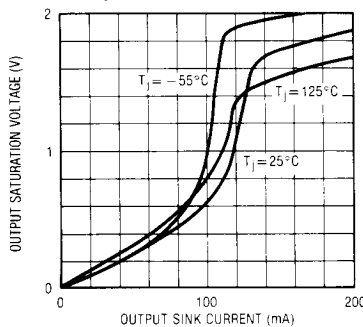
Output Rise and Fall Time



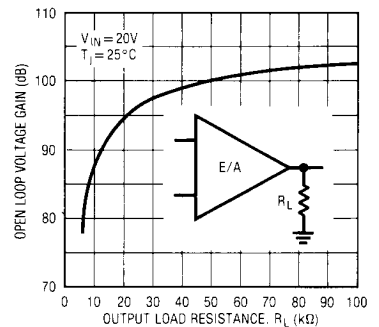
Output High Level Saturation Voltage vs Output Source Current



Output Low Level Saturation Voltage vs Output Sink Current

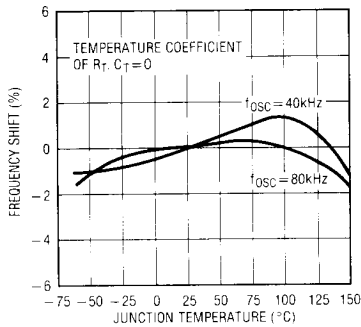


Error Amp Open-Loop DC Gain vs Load Resistance

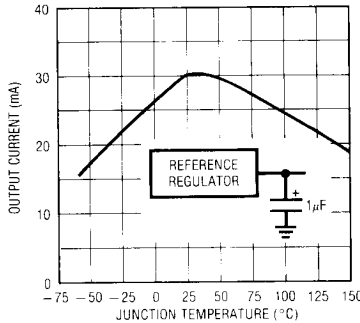


## TYPICAL PERFORMANCE CHARACTERISTICS

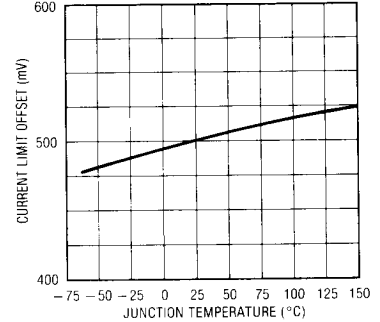
**Oscillator Frequency vs Temperature**



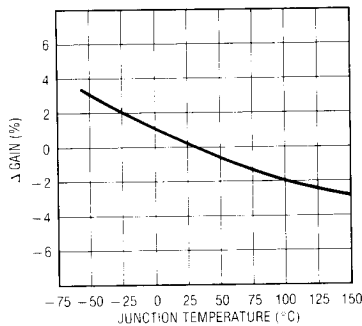
**Reference Current Limit**



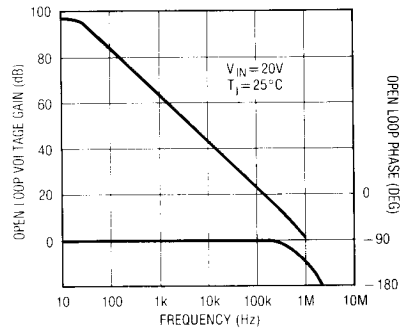
**Current Limit Offset vs Temperature**



**Current Sense Amplifier Gain vs Temperature**



**Error Amplifier Gain and Phase vs Frequency**



## APPLICATIONS INFORMATION

### Current Mode Control

Current mode controllers directly control peak inductor current with the error signal rather than controlling the duty cycle of the PWM as conventional controllers do. There are several inherent advantages in this type of control.

Current mode controllers are easier to frequency compensate. Peak inductor current is forced to follow the error signal and can change only if the error signal changes. This forces the inductor to act like a constant current source at mid frequencies and the order of the system can be reduced by one, eliminating 90° of phase shift.

Peak current on a pulse-by-pulse basis can be limited by simply limiting the positive swing of the error amplifier.

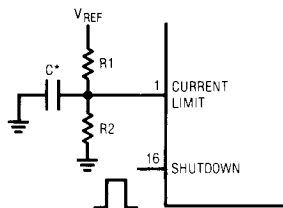
Transient line regulation is greatly improved. A change in the line voltage causes a change in the slope of the inductor current. This means that the time it takes for the inductor current to reach the peak control value automatically changes, and requires very little change in the output of the error amp. Since transient response is limited by the integrator response of the error amplifier, excellent line transient response is obtained if the error amplifier output does not have to change.

## APPLICATIONS INFORMATION

With current mode control, some amount of slope compensation is required to prevent oscillations for duty cycles greater than 50%. Slope compensation can also be used to decrease noise sensitivity for low values of inductor current ripple, and to prevent subharmonic oscillations in the inductor current.

### Shutdown/Soft Start

A logic high at pin 16 will initiate a shutdown cycle. During a shutdown cycle, both outputs are held off and pins 1 and 7 are pulled low. If pin 1 current ( $I_{P1} = V_{REF}/R_1$ ) is less than the latch threshold current, typically 1.5mA (see Electrical Characteristics), the device will restart at the end of the shutdown pulse. If pin 1 current is greater than the latch threshold current, the device will latch off until power is recycled.

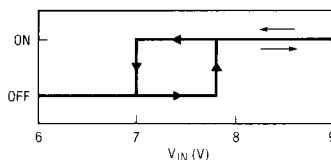


Soft start is accomplished by the addition of a capacitor from pin 1 to ground. This forces the peak value of the switch current to come up slowly. Pin 16 can be left floating if the shutdown function is not used.

### Undervoltage Lockout

The purpose of the undervoltage lockout is to prevent the device from switching until the internal circuitry is operating properly. Built-in hysteresis prevents the circuit from oscillating at the threshold point. Pin 1 (current limit adjust) and pin 7 (comp) are held low during undervoltage lockout, and outputs are low (UC1846) or high (UC1847).

Output Switches



### Oscillator Section

The frequency of the oscillator is set by an external resistor ( $R_T$ ) from pin 9 to ground, and an external capacitor ( $C_T$ ) from pin 8 to ground.  $C_T$  is charged by a constant current  $I_{RT} = V_{Pin 9} (\approx 3.6V)/R_T$ , and is discharged by a constant current  $8mA - I_{RT}$ . Upper and lower trip levels are determined by the internal circuitry, such that the oscillator frequency is approximated by the formula

$$f_T \approx \frac{2.2}{R_T(\Omega)C_T(F)}$$

In addition, output deadtime, which is equal to the capacitor discharge time, is a function of the size of  $C_T$  and can be calculated according to the formula:

$$T_d = 145C_T \left( \frac{8mA}{8mA - \frac{3.6V}{R_T}} \right)$$

For large values of  $R_T$  (small  $I_{RT}$ ):  $T_d \approx 145C_T$ .

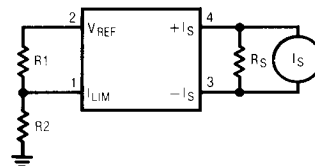
### Current Limit

Peak switch current on a pulse-by-pulse basis is a function of the voltage level set at pin 1 and the current sense resistor  $R_S$ , and can be determined by the formula:

$$I_S = \frac{R_2 V_{REF}}{R_1 + R_2} - 0.5V$$

$$G \bullet R_S$$

$$G = I/A \text{ GAIN} = 2.75 \text{ TYP}$$

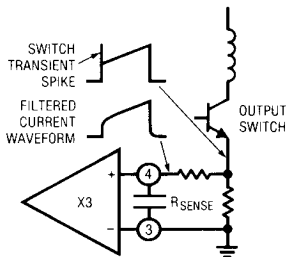


## APPLICATIONS INFORMATION

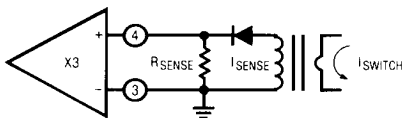
### Current Sensing

The current sense amplifier is a differential amplifier with a gain of 3 and a common-mode range of 0 to  $V_{IN} - 3V$ . Maximum differential input signal is 1.2V. Several sensing schemes are possible. Direct resistive sensing is the simplest, but power losses in the resistor may not be acceptable. The use of a current sense transformer will increase efficiency for higher current levels, but will increase circuit complexity. In configurations where switch current is sensed, a small RC may be necessary to keep switch turn on transients from tripping the current sense latch. Without this filter, erratic operation will result especially at lower values of output current. Minimum on-time of the output switch during a short circuit is equal to the delay from the current sense amplifier to the output, typically 200ns. This delay will be longer if a filter for switch transients is added. For best noise immunity, the signal at the current sense amplifier inputs should be as large as possible.

#### Resistive Sensing of Switch Current with RC Filter



#### Transformer Sensing Gives Isolation and Improved Efficiency



### Error Amplifier

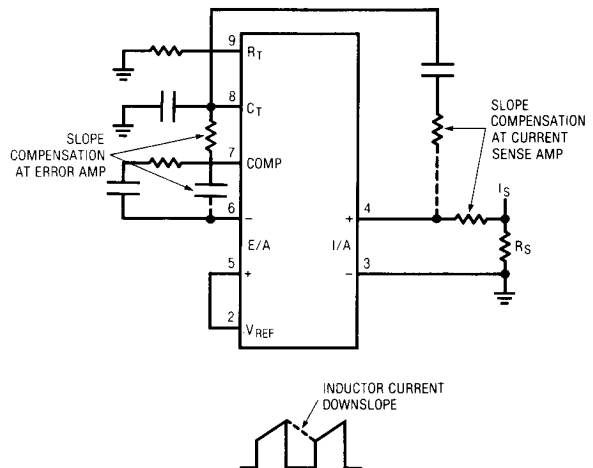
The error amplifier of the UC1846 can operate over a common-mode range of 0 to  $V_{IN} - 2V$ . The output stage consists of an NPN Darlington pull-down and a 0.5mA current source pull-up. See Typical Performance Characteristics for gain and phase characteristics.

### Reference Regulator

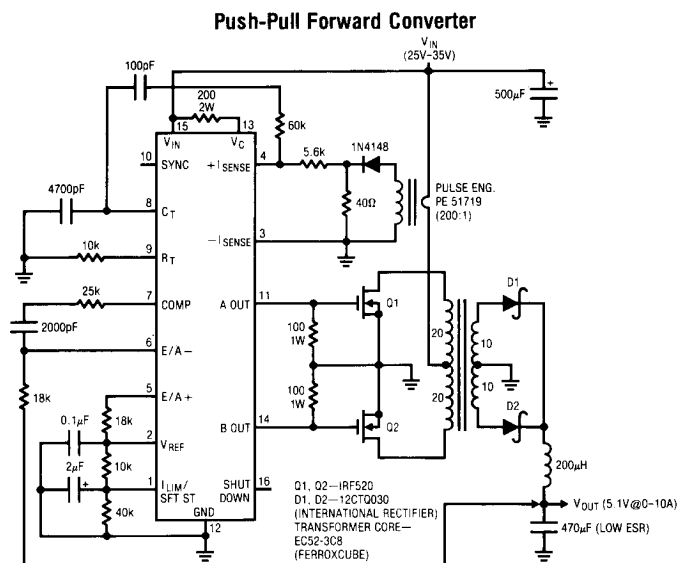
The reference regulator provides a fixed 5.1V for internal circuitry as well as up to 20mA of output current for external circuitry such as the current limit divider. A small bypass capacitor (0.1–1.0μF) from the reference pin (pin 2) to the ground pin (pin 12) is recommended. This capacitor should be located as close as possible to the device.

### Slope Compensation

Slope compensation can be accomplished by summing a triangle wave derived from the oscillator waveform, with the inductor current waveform at the current sense amplifier input or the summing node of the error amplifier as shown below. Slope compensation should be greater than 1/2 of the downslope of the inductor current waveform.

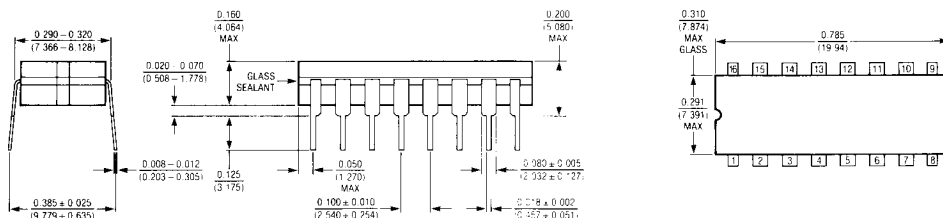


## TYPICAL APPLICATIONS CIRCUIT



## PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

## 16 Pin Cavity DIP (J)



	$T_{max}$	$\theta_{JA}$	$\theta_{JC}$
UC1846	150°C	100°C/W	60°C/W
UC1847			
UC3846	105°C	100°C/W	60°C/W
UC3847			

## 16 Pin Molded DIP (N)

