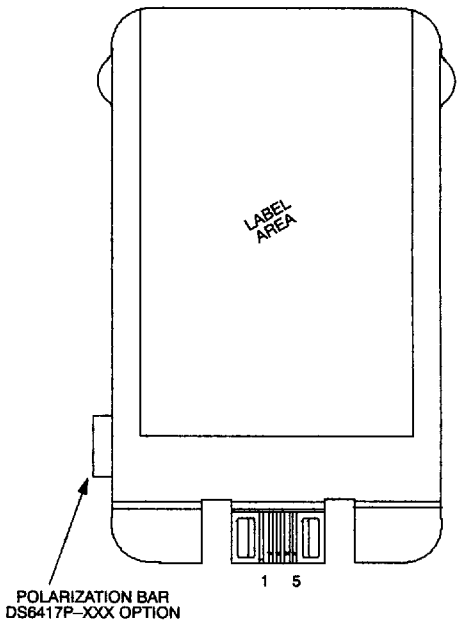
DALLAS SEMICONDUCTOR

DS6417
CyberCard EV 4M-Bit NV SRAM

FEATURES

- Greater than 50,000 insertion connector life
- Durable and rugged
- Ground pin makes first and breaks last
- User-insertable memory
- Capacities from 256K bits to 4M bits of nonvolatile memory
- Up to 1 million bits per second transfer rate
- Automatic write protection circuitry safeguards against data loss
- Cyclic redundancy check monitors serial data transmission for errors
- Compact size and shape
- Wide operating temperature range of -20°C to +70°C

PIN ASSIGNMENT



PIN DESCRIPTION

Pin 1	–	Ground
Pin 2	–	Clock
Pin 3	–	Data
Pin 4	–	$\overline{RST}$
Pin 5	–	V_{CC}

DESCRIPTION

The DS6417 CyberCard EV is a nonvolatile serial access RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 256K bits to 4M bits. Data is transferred to and from the RAM through a standard 3-wire serial interface which is comprised of DQ, $\overline{RST}$, and CLK signals. The serial port requires a 7-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmissions for errors.

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PIN DESCRIPTION OVERVIEW

$\overline{RST}$ – This pin controls all communication to the DS6417. When this signal is LOW, all communication to the serial port is inhibited. When high, data can be clocked into or out of the serial port.

CLK – This input signal is used to input or extract data from the serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven onto the 3-wire bus after a falling edge during a read cycle and latched into the port on the rising edge during a write cycle.

DQ – This signal is the bidirectional data signal for the 3-wire port.

OPERATION

The block diagram of Figure 1 illustrates the main elements of the DS6417. As shown, the DS6417 has two major sections: the static RAM array and the 3-wire to bytewide converter. The 3-wire to bytewide converter controls the static RAM through the use of the control/address/data latches and multiplexer.

The 3-wire to bytewide converter uses a 56-bit protocol to determine the action to be taken and the starting address in RAM to be used. Data is entered while $\overline{RST}$ is high on the low to high transition of the CLK signal provided the data is stable on the DQ line for the proper setup and hold times.

The last 8 bits of the 56-bit protocol contain the cyclic redundancy check byte that ensures all bits of the protocol have been transmitted correctly. If the 56 bits of protocol have not been received properly, the transaction will be aborted. The CRC check byte can catch up to three bit errors within the 56-bit protocol and can also be used on incoming and outgoing data streams to check the integrity of the data being read or written.

PROTOCOL

The 3-wire bus protocol can cause six different actions to be taken by the DS6417 (see Table 1).

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action to be taken involves a read or a write. A read function is defined by the binary pattern [11101000]. This pattern is applicable to commands 1,3,5, and 6 of Table 1. A write function is defined by the binary pattern [00010111]. This pattern is applicable to commands 2 and 4 of Table 1. Any other pattern which is entered into this read/write field will cause the transaction to be terminated. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of protocol referred to as the command field. The command field bits are shown as the binary values in Table 1.

BURST READ

A burst read uses a 19-bit address field which consists of the second byte, third byte, and the first three bits of the fourth byte of the protocol to determine the starting address of the information to be read from the RAM. The byte of data that has been accessed is transferred to the 3-wire bus a bit at a time, LSB first, by driving the DQ line on the falling edge of the next eight clocks.

BURST WRITE

A burst write uses the same 19 bit address field to determine the starting address of information to be written in RAM. Data is shifted from the DQ line into an eight bit shift register on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte by byte basis automatically incrementing the selected address by one location for each successive byte.

PROTOCOL COMMANDS Table 1

1) [00110 binary] burst read
2) [10001 binary] burst write
3) [00101 binary] read protocol select bits
4) [01110 binary] write protocol select bits
5) [11XXX binary] burst read masking portions of the protocol select bits
6) [00011 binary] read the CRC register

Termination of a current transaction will occur at any time the $\overline{RST}$ signal is taken low. If a byte of data has been loaded into the shift register a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when the $\overline{RST}$ signal goes low, no writing occurs. Reads can be terminated at any point since there is no potential for the corruption of RAM data.

READ CRC

The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the 56-bit protocol. The 8-bit CRC value is valid for both the 56-bit protocol and also all data that is read or written from the RAM. After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in an internal register of the DS6417. If a read CRC register command is issued, the stored CRC value is driven onto the DQ signal line by the first eight clock cycles after the 56-bit protocol is received. The CRC value generated by the DS6417 should match the value generated by the host system which is transmitting or receiving data on the other end of the 3-wire bus.

It should be noted that the CRC for a previous transaction can only be obtained if a read CRC command is issued immediately after the $\overline{RST}$ signal goes low to reset the DS6417, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever the $\overline{RST}$ signal goes low again.

Three commands are used to set the select bits in the protocol. Once the select bits are set to a binary value, they must be matched when protocol is sent or further activity is prevented. The bits allow for up to 65,536 different binary combinations. Therefore, multiple DS6417s can be connected on the same 3-wire bus and only the selected device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field. To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have a large number of DS6417s in use and uniquely identify each one. A read can occur successfully without knowing the select bits, but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS6417 in the presence of many DS6417s. A read in the read/write field and a [11000 binary] in the command field will execute a mask read that ignores all select bits to determine the presence of any DS6417s. With the detection of at least one device, a search can begin by masking all but a single pair of DS6417 select bits. A read in the read/write field and a [11001 binary] in the command field will unmask the first two LSB's of byte 4 of the select bits (Figure 3). With these two select bits unmasked, only an exact match of four possible combinations (00, 01, 10, or 11) of these two select bits will now allow access through the 3-wire port to RAM. Therefore, repeating the unmasking of the two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of the four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will yield an exact match of the one DS6417 out of the possible 65,536 in no more than 32 attempts.

CRC GENERATION

The logic involved in the CRC generation is shown in Figure 4. Basically, the scheme is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQ IN to the CRC generator while each byte is being assembled and at the same time, output data to the output (DQOUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire bus.

The reset signal (RSB) must be high while the CRC generator is being used as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS6417 CRC requirements.

However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Microcontroller. The assembly language procedure DO_CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to cal-

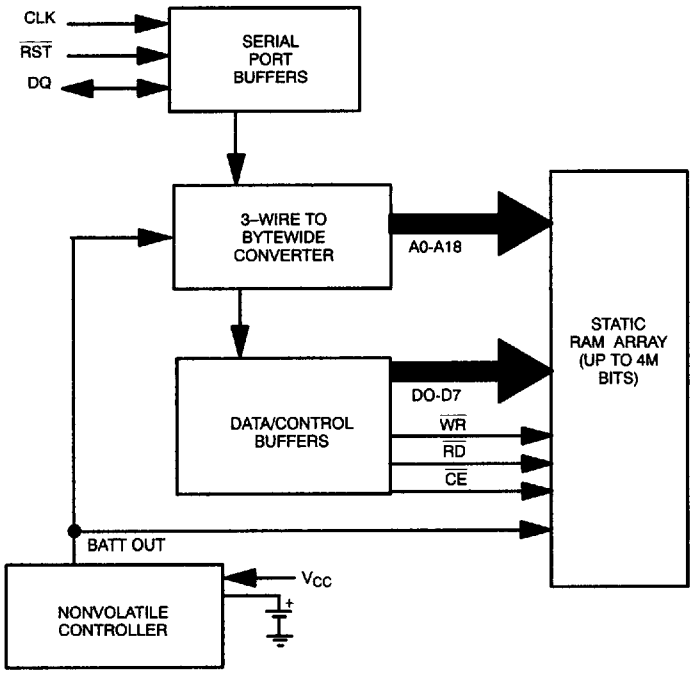
culate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO_CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

3-WIRE BUS

The 3-Wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the $\overline{RST}$ is low and the DQ pin goes to a high impedance state. When data transfers to the DS6417 are terminated by the $\overline{RST}$ signal going low, the transition of the $\overline{RST}$ going low must occur during a high level of the CLK signal. Failure to insure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figures 5 and 6 for normal modes of operation.

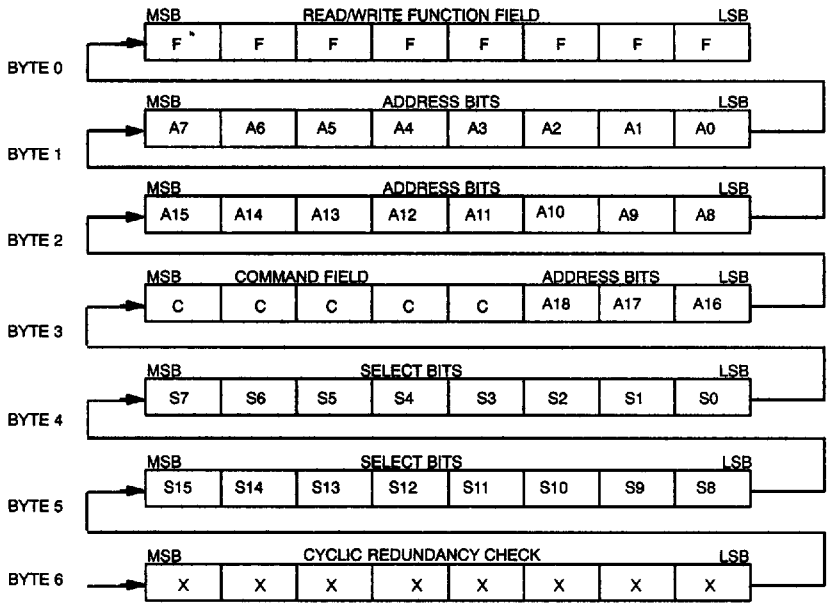
BLOCK DIAGRAM Figure 1



CRC CODE Table 2

```
DO_CRC:
        PUSH    ACC                     ;Save the Accumulator
        PUSH    B                       ;Save the B register
        PUSH    ACC                     ;Save bits to be shifted
        MOV     B,      #8              ;Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC             ;Calculate DQIN xor CRCTO
        RRC     A                       ;Move it to the last
        MOV     A,      CRC             ;Get the last CRC value
        JNC     ZERO                    ;Skip if DQIN xor CRCTO=0
ZERO:   XRL     A,      0CCH            ;Update the CRC value
        RRC     A                       ;Position the new CRC
        MOV     CRC,    A               ;Store the new CRC
        POP     ACC                     ;Get the remaining bits
        RR      A                       ;Position next bit in LSB
        PUSH    ACC                     ;Save the remaining bits
        DJNZ    B,      CRC_LOOP        ;Repeat for eight bits
        POP     ACC                     ;Clean up the stack
        POP     B                       ;Restore the B register
        POP     ACC                     ;Restore the Accumulator
        RET                             ;Return
```

PROTOCOL Figure 2



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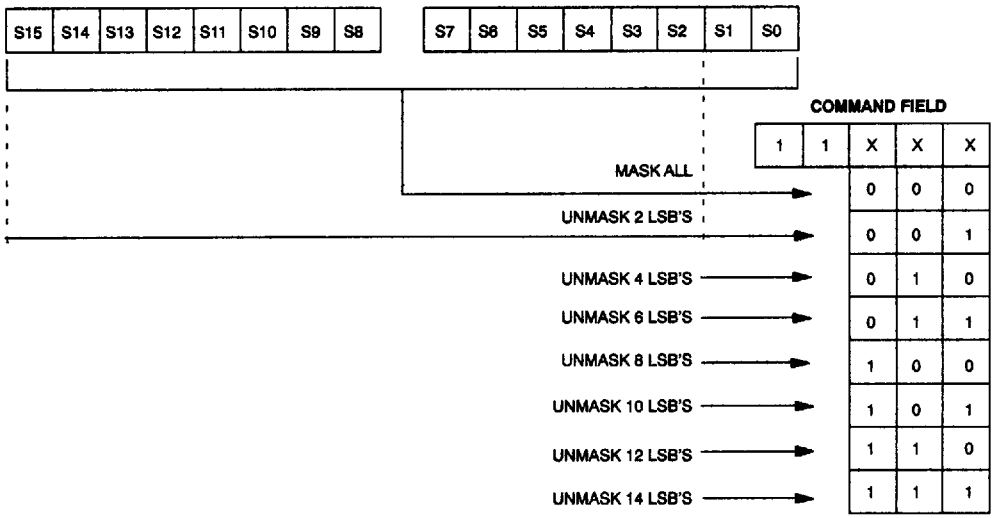
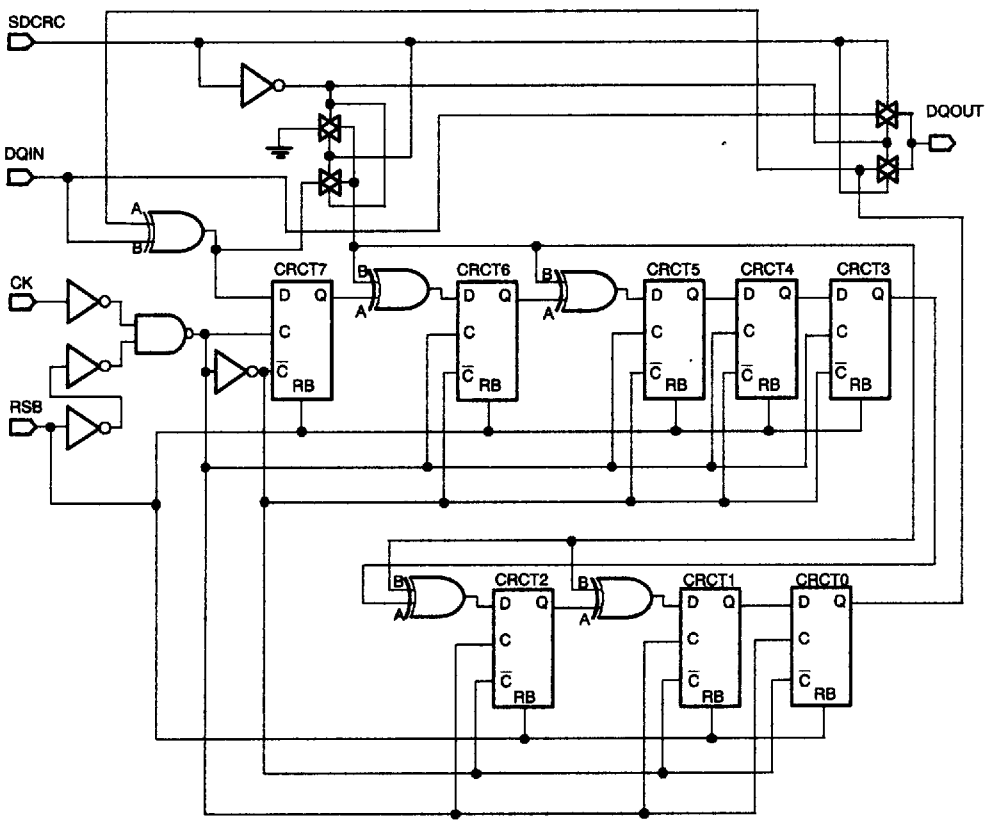
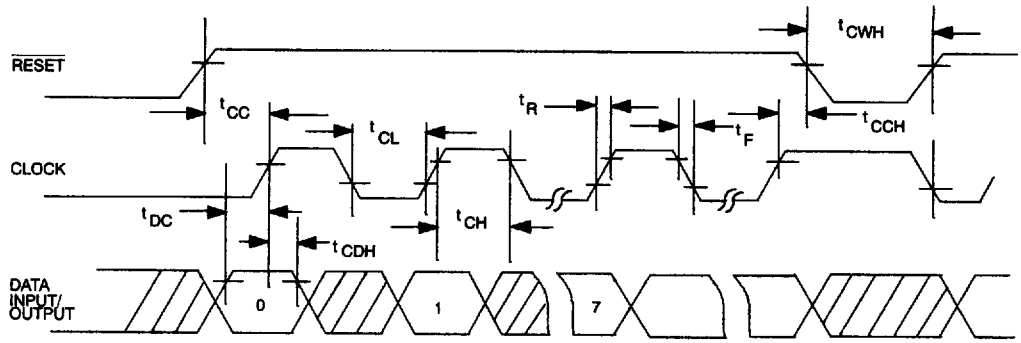
SELECT BITS MASK Figure 3



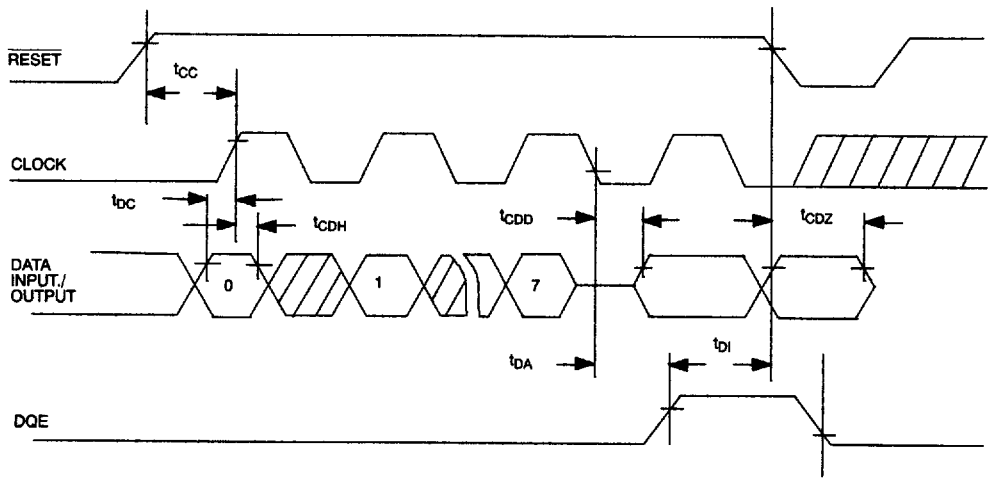
CRC GENERATION Figure 4



TIMING DIAGRAM: WRITE DATA Figure 5



TIMING DIAGRAM: READ DATA Figure 6

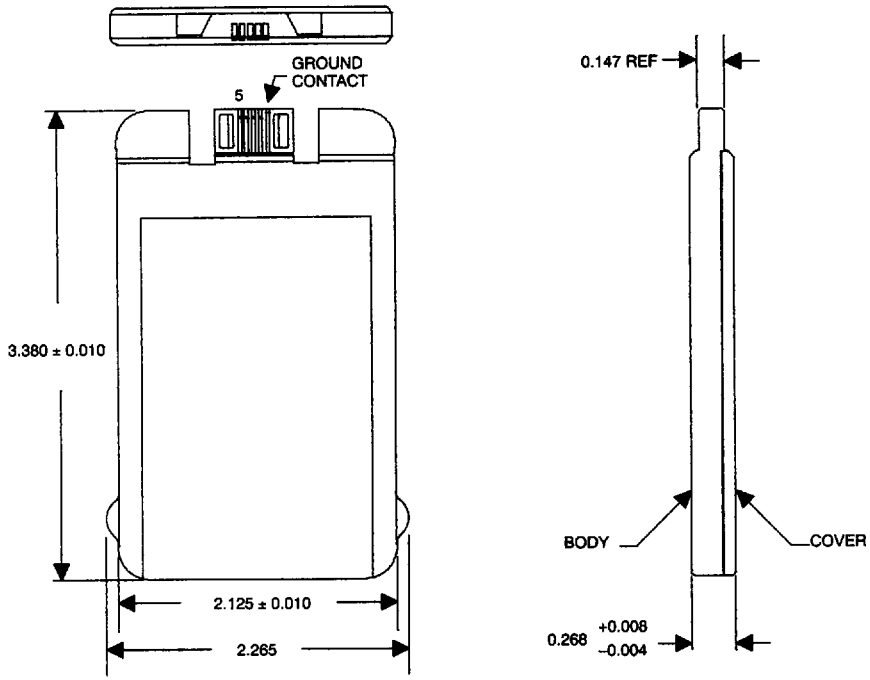


PACKAGING

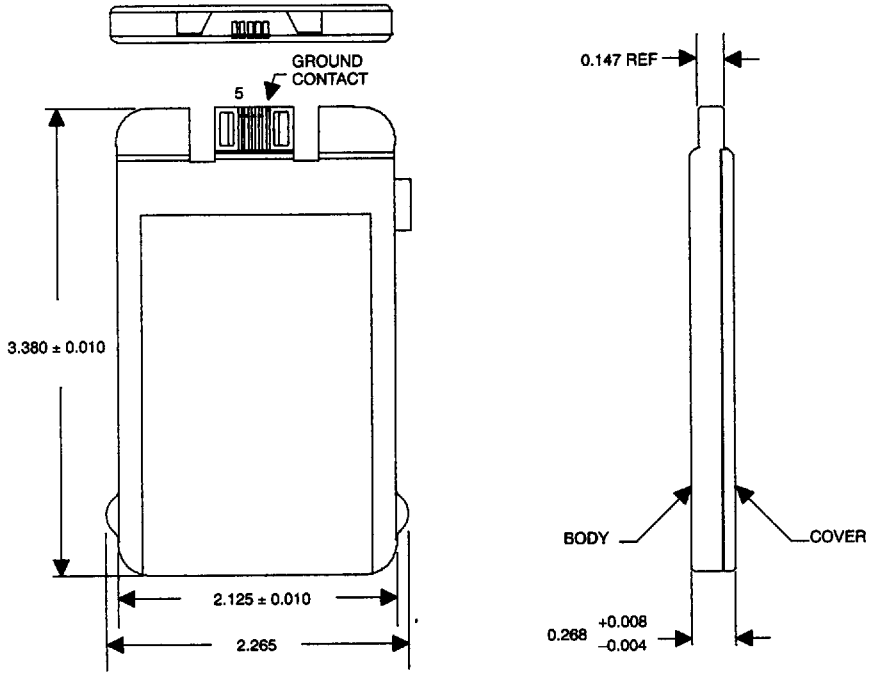
The DS6417 is offered in two standard packages. These include the DS6417O–XXX and DS6417P–XXX options. The DS6417O–XXX package is available in beige color only, and has a wrap–around label area and body grips. The DS6417P–XXX package is black in color, and has a wrap–around label area, body grips, and a polarization strip or bar for insertion alignment with the DS9084X–001 recessed receptacle. Both packages are shown in Figure 7.

DS6417 PACKAGE OPTIONS Figure 7

CyberCard Package, Non–Polarized



CyberCard Package, Polarized



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	-4.5	5.0	5.5	Volts	1
Input High Voltage	V_{IH}	2.2		V_{CC}	Volts	1
Input Low Voltage	V_{IL}	0.0		+0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-60		+60	µA	
I/O Leakage	I_{LO}	-10		+10	µA	
Output Current	I_{OH}	-1.0	-2.0		mA	2
Output Current	I_{OL}	2.0	3.0		mA	3
Operating Current	I_{OP}		10	20	mA	
Input Capacitance	C_{IN}		5		pF	
I/O Capacitance	C_{IB}		5		pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	4
V_{CCI} Slew Rate	t_R	1			µs	4
Power Down to $\overline{PF}$	t_{PF}	0			µs	4
$\overline{PF}$ Recovery	t_{REC}			100	µs	4

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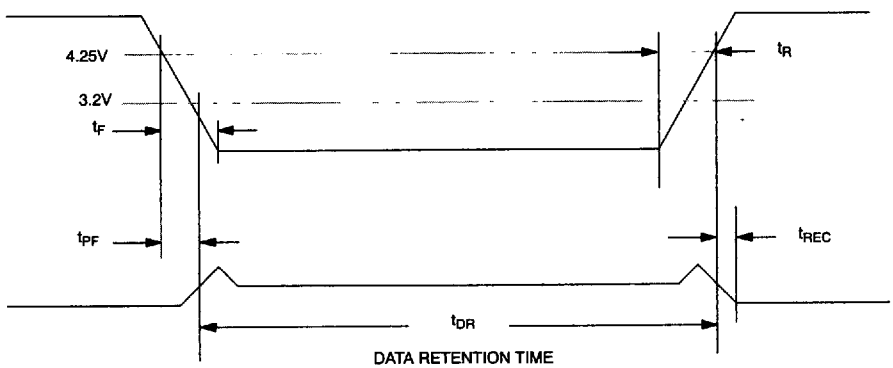
AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V ± 10%; 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
Data to CLK Hold	t_{CDH}	40			ns	2
Data to CLK Delay	t_{CDD}			125	ns	2,3,5
CLK Low Time	t_{CL}	500			ns	2
CLK High Time	t_{CH}	500			ns	2
CLK Frequency	f_{CLK}	DC		1	MHz	2
CLK Rise & Fall Time	t_R t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	2

NOTES:

1. All voltages are referenced to ground.
2. @ 2.4 volts.
3. @ 0.4 volts.
4. See Figure 8.

POWER-DOWN/POWER-UP CONDITION Figure 8