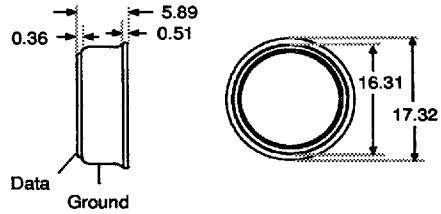
DALLAS SEMICONDUCTOR

DS1494L-F5
Time-In-a-Can

FEATURES
- Miniature timekeeping system sealed in a 16mm MicroCan
- Snaps into a surface-mounted printed circuit board retainer
- Self-powered with greater than 10 years of lithium
- Keeps precise time in 1/256 second increments
- Quartz accuracy of ±2 minutes per month (at 25°C) can be improved by storing calibration bits in nonvolatile SRAM
- Interval timer measures duration of an activity
- Number of power on/off cycles detected and stored in cycle counter
- Programmable alarms generate interrupts for real time, interval timer and/or cycle count
- 4096 bits of nonvolatile SRAM organized in 16 pages of 256 bits
- Data integrity assured by verifying data in a scratchpad before transferring to memory
- 1-wire interface shares only one I/O pin for 16K bits per second communication
- Unique 48-bit, factory-lasered serial number for identification and traceability
- Tamper-proof lock bits prevent alteration of timers and cycle counter
- Operating temperature range -40 to 70°C
- Applications include computer real-time clock, run time meter, sequence timer, event recorder, warranty information, maintenance records, configuration, and calibration data

TIME IN A CAN



DS9098 Surface Mount Snap-In Retainer

ACTUAL SIZE

DESCRIPTION
The DS1494L-F5 Time-In-a-Can (TIC) supplies accurate time-of-day information, measures run time, schedules activities, and records vital data. Its one and only signal communicates through the lid of a sealed MicroCan. Dallas Semiconductor's development of this minimal signalling technique for integrated circuits, called 1-wire, made it possible to seal a silicon chip, quartz, and a lithium energy source in an inexpensive stainless steel enclosure, not significantly larger than the battery would have been by itself. Furthermore, the solo data signal simplifies mounting to the printed circuit board and lowers the cost of electrical interface. TIC is a full-feature timekeeping system including a unique, lasered serial number, real-time clock, run-time meter, cycle

counter, programmable interrupts, 256-bit scratchpad, and 4096 bits of nonvolatile SRAM.

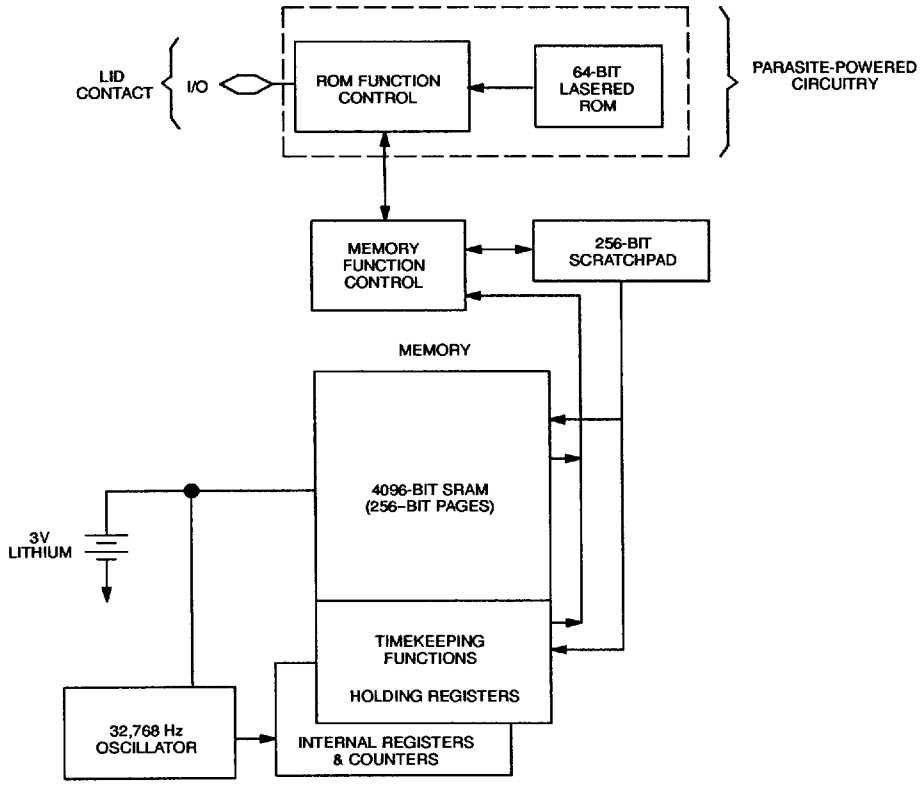
The unalterable serial number is registered for absolute traceability. TIC surface mounts to a printed circuit board by a snap-in retainer (DS9098) or thru-hole mount (DS9094F). Using a contact probe, data can be read or written even when the printed circuit board is without power. All data is nonvolatile for greater than 10 years.

OVERVIEW

The DS1494L-F5 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands (Figure 6).

DS1494L-F5 BLOCK DIAGRAM Figure 1



PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for any reason, the ROM may still be read normally.

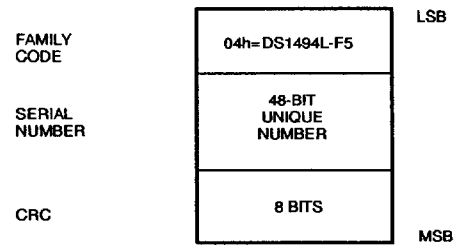
64-BIT LASERED ROM

Each DS1494L-F5 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

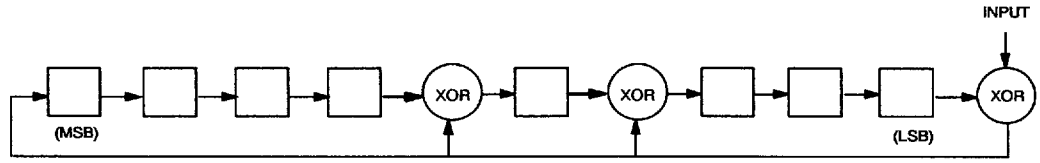
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Appendix S4 in the Book of Touch Memory Standards.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

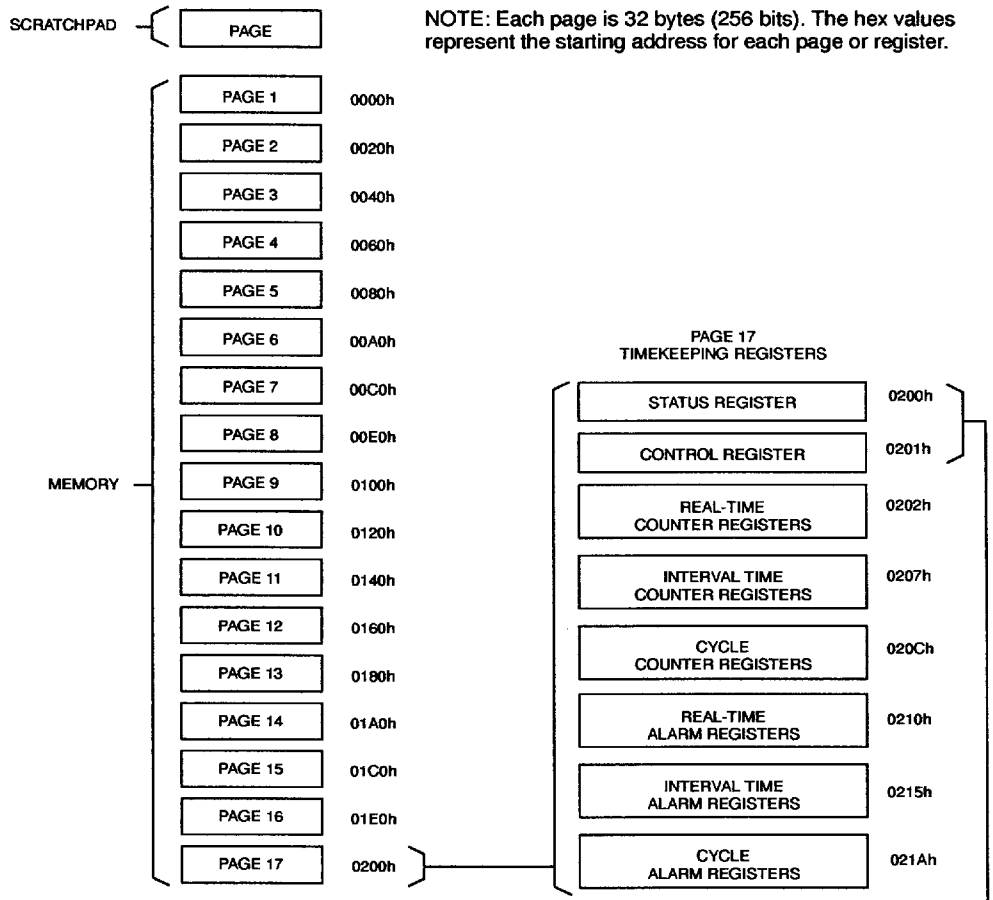
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



DS1494L-F5 MEMORY MAP Figure 4



MEMORY

The memory map in Figure 4 shows a 32-byte page called the scratchpad and additional 32-byte pages called memory. Pages 1 through 16 make up the 4096-bit SRAM and page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer and cycle counter to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

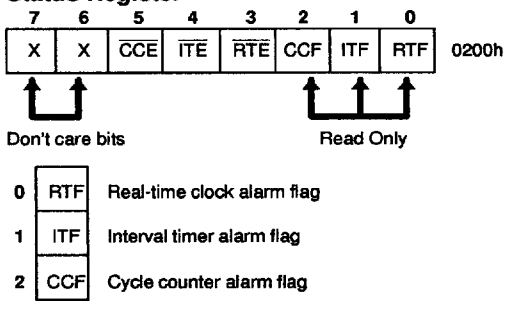
Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register



When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3 $\overline{\text{RTE}}$ Real-time interrupt enable

4 $\overline{\text{ITE}}$ Interval timer interrupt enable

5 $\overline{\text{CCE}}$ Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{\text{START}}$	AUTO/$\overline{\text{MAN.}}$	OSC	RO	WPC	WPI	WPR	0201h

0 WPR Write protect real-time clock/alarm registers

1 WPI Write protect interval timer/alarm registers

2 WPC Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3 RO Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1494L-F5 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4 OSC Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5 AUTO/$\overline{\text{MAN}}$ Automatic/$\overline{\text{Manual}}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{\text{START}}$ bit.

6 STOP/$\overline{\text{START}}$ Stop/$\overline{\text{Start}}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7 DSEL Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

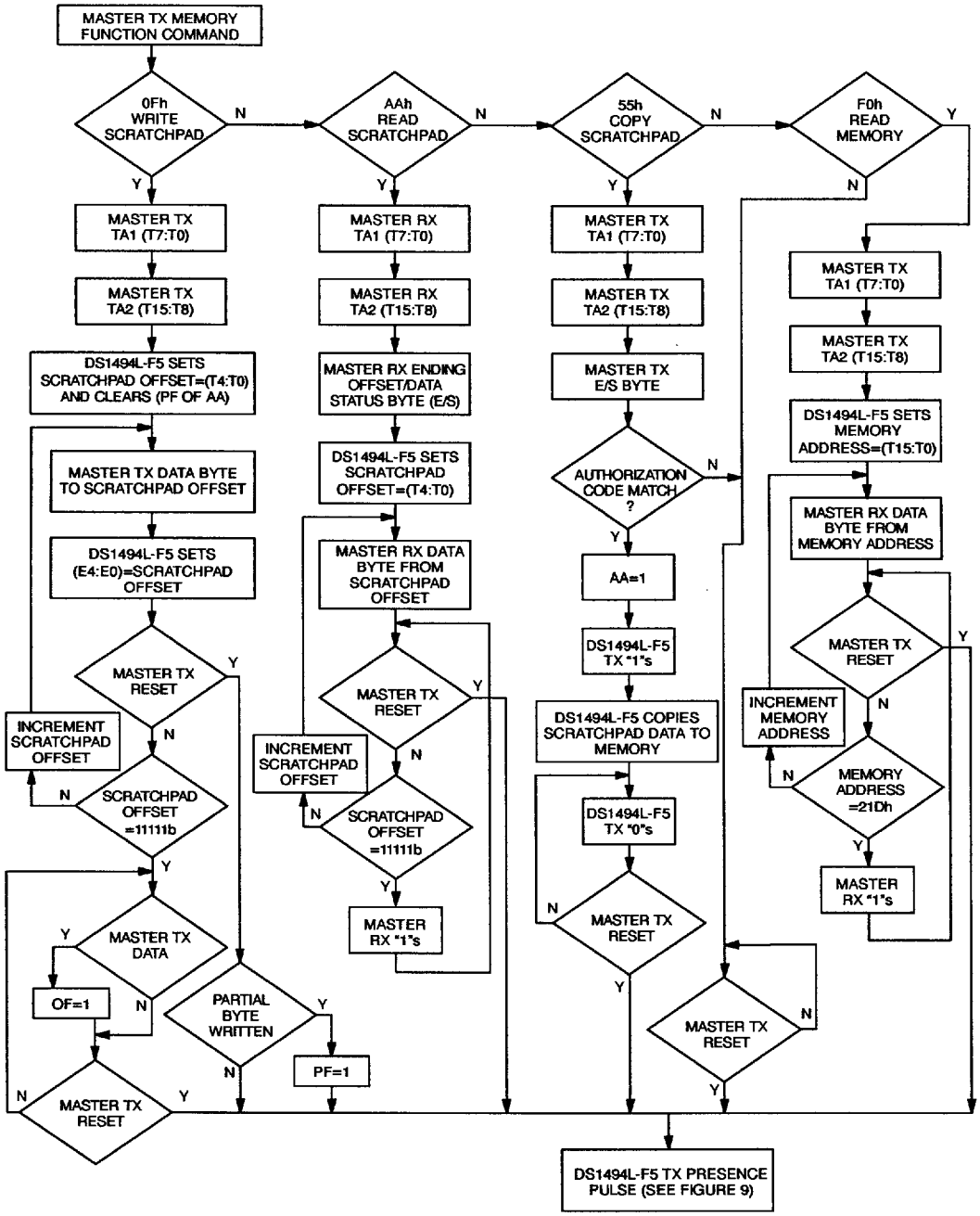
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the user. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

WRITE PROTECT/PROGRAMMABLE EXPIRATION (DS1494L-F5)

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1494L-F5 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".
** Forced to a logic "0".

1-WIRE BUS SYSTEM

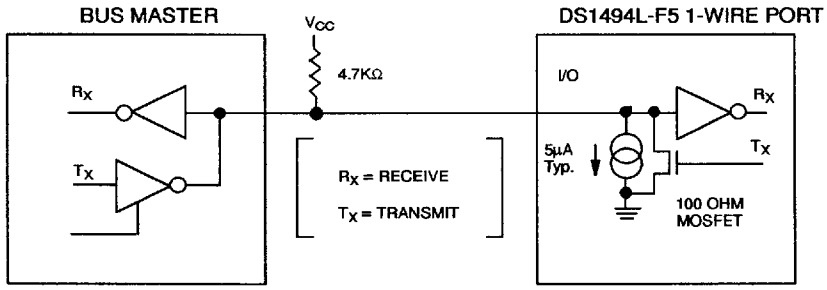
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS1494L-F5 behaves as a slave. The exception is when the DS1494L-F5 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS1494L-F5 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus has a maximum data rate of 16.3K bits per second and requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS1494L-F5 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1494L-F5 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS1494L-F5's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1494L-F5 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mis-match of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1494L-F5 on a multidrop bus. Only the DS1494L-F5 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Search Interrupt [ECh]

This command works exactly as the normal ROM search, but it will identify only devices with interrupts that have not yet been acknowledged.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
2. The bus master will then issue the search ROM command on the 1-wire bus.
3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

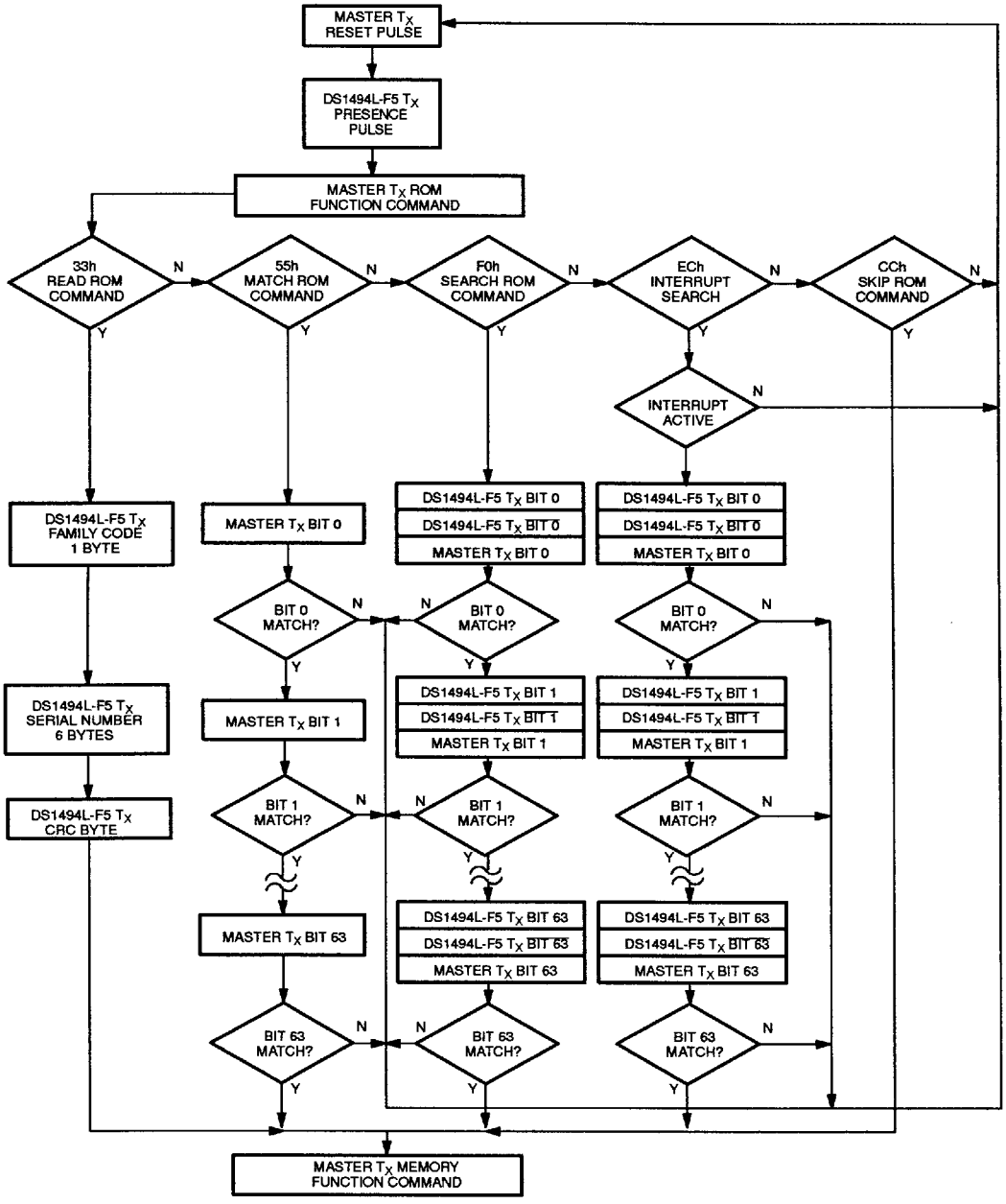
   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.
10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
13. The bus master starts a new ROM search by repeating steps 1 through 3.
14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
15. The bus master executes two read time slots and receives two zeros.
16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.
17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

ROM FUNCTIONS FLOW CHART Figure 9



18. The bus master starts a new ROM search by repeating steps 13 through 15.
19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

At this point, the bus master repeats the process described above to determine the ROM code of the remaining devices on the 1-wire bus.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

I/O SIGNALLING

The DS1494L-F5 requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse (DS1494L-F5). All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

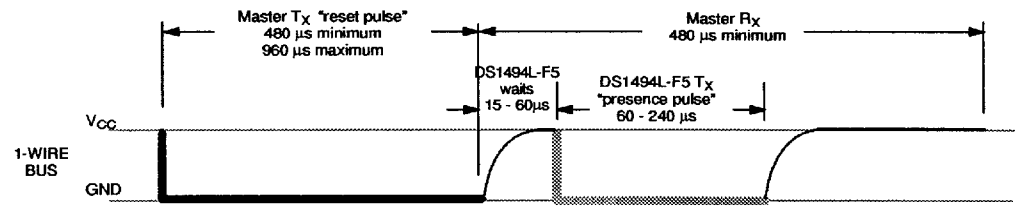
The initialization sequence required to begin any communication with the DS1494L-F5 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1494L-F5 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS1494L-F5 waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

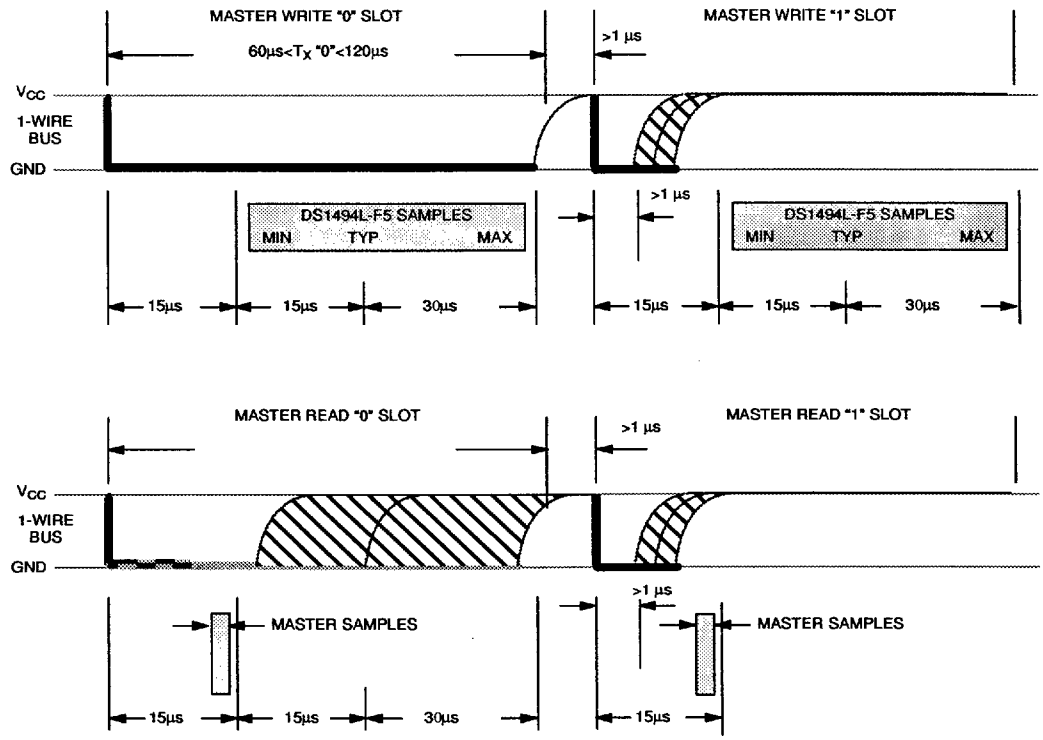
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS1494L-F5 to the master by triggering a delay circuit in the DS1494L-F5. During write time slots, the delay circuit determines when the DS1494L-F5 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS1494L-F5 will hold the I/O line low.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



READ/WRITE TIMING DIAGRAM Figure 11



DETAILED MASTER READ "1" TIMING Figure 12

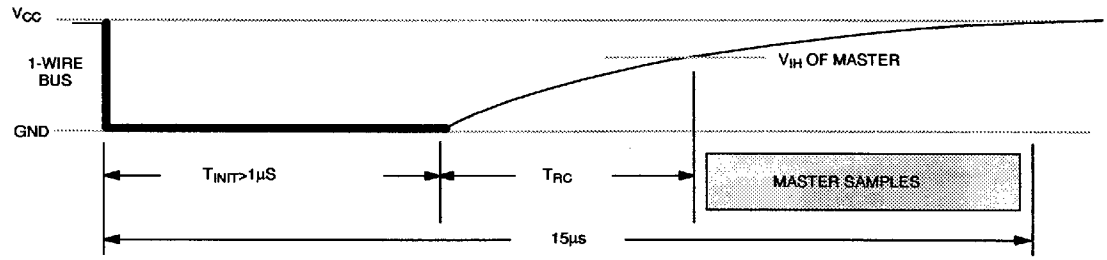
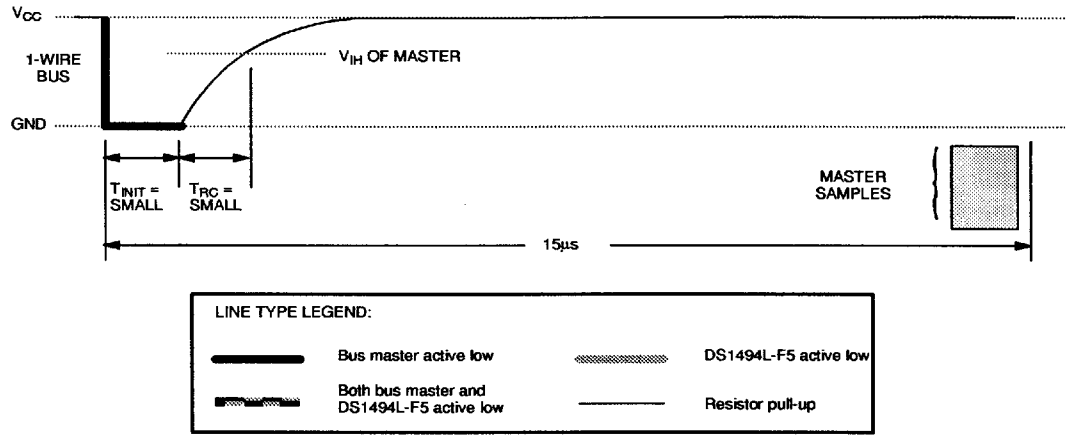


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 13



Interrupts (DS1494L-F5)

If the DS1494L-F5 detects an alarm condition, it will automatically set the corresponding alarm flag in the Status Register. An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the Status Register) or if the corresponding interrupt enable bit is disabled.

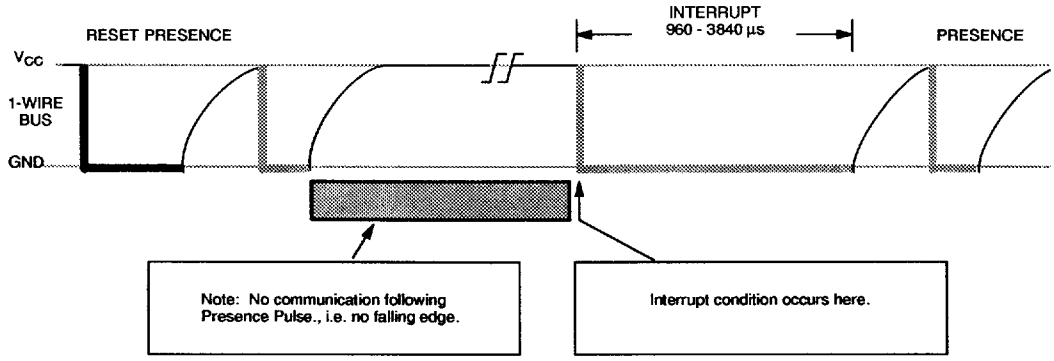
The DS1494L-F5 can produce two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts, type 2. Spontaneous interrupts need to be armed by a Reset Pulse after all communication on the 1-wire bus has finished. A single falling slope on the 1-wire bus will disarm this type of interrupt. If an alarm condition occurs while the device is disarmed, type 2 interrupts will be produced.

Spontaneous interrupts are signalled by the DS1494L-F5 by pulling the data line low for 960 to 3840 µs as the interrupt condition begins (Figure 14). After this long low pulse a Presence Pulse will follow. If the alarm condition occurs just after the master has sent a Reset Pulse, i.e., during the reset high time, the DS1494L-F5 will not assert its Interrupt Pulse until the Presence Pulse is finished (Figure 15).

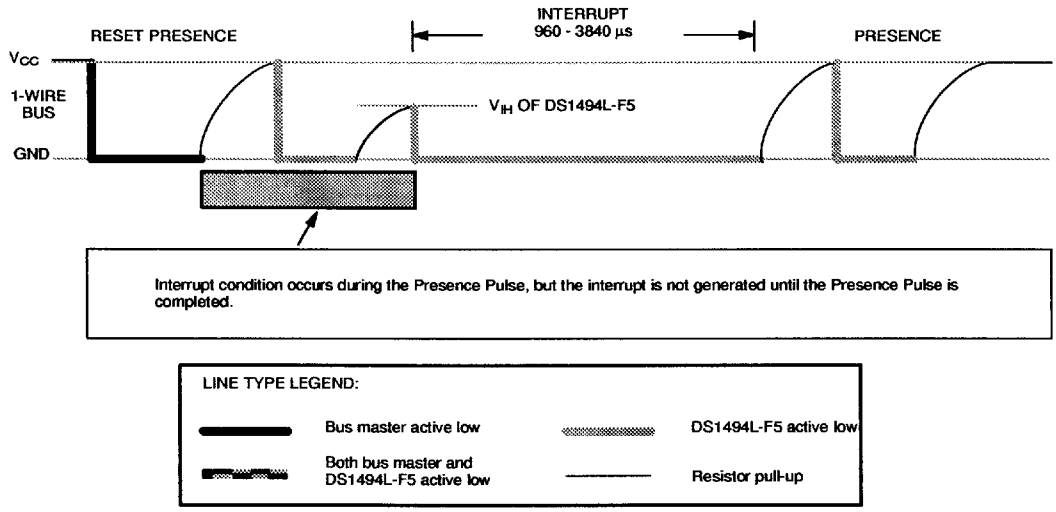
If the DS1494L-F5 cannot assert a spontaneous interrupt, either because the data line was not pulled high, communication was in progress, or the interrupt was not armed, it will extend the next and every subsequent

Reset Pulse to a total length of 960 to 3840 µs (delayed interrupt). If the alarm condition occurs during the reset low time of the Reset Pulse, the DS1494L-F5 will immediately assert its interrupt pulse; thus the total low time of the pulse can be extended up to 4800 µs (Figure 16). If a DS1494L-F5 with an active alarm detects a power-on cycle on the 1-wire bus, it will send a Presence Pulse and wait for the Reset Pulses to signal a delayed interrupt (Figure 17). As long as an interrupt has not been acknowledged by the master, the DS1494L-F5 will continue sending type 2 interrupts.

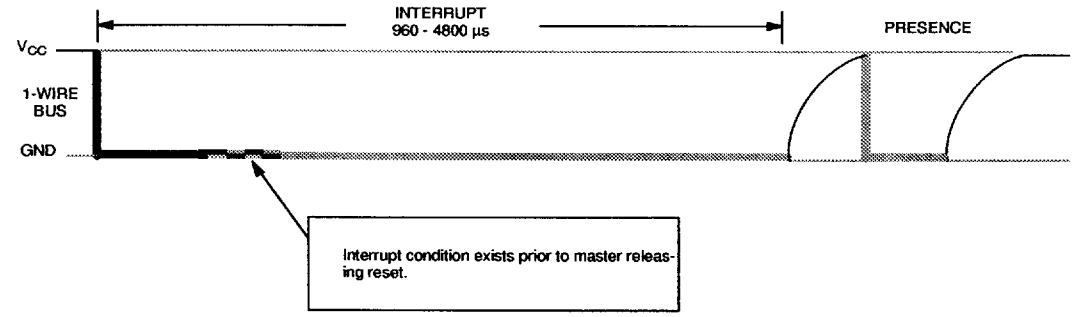
TYPE 1 INTERRUPT Figure 14



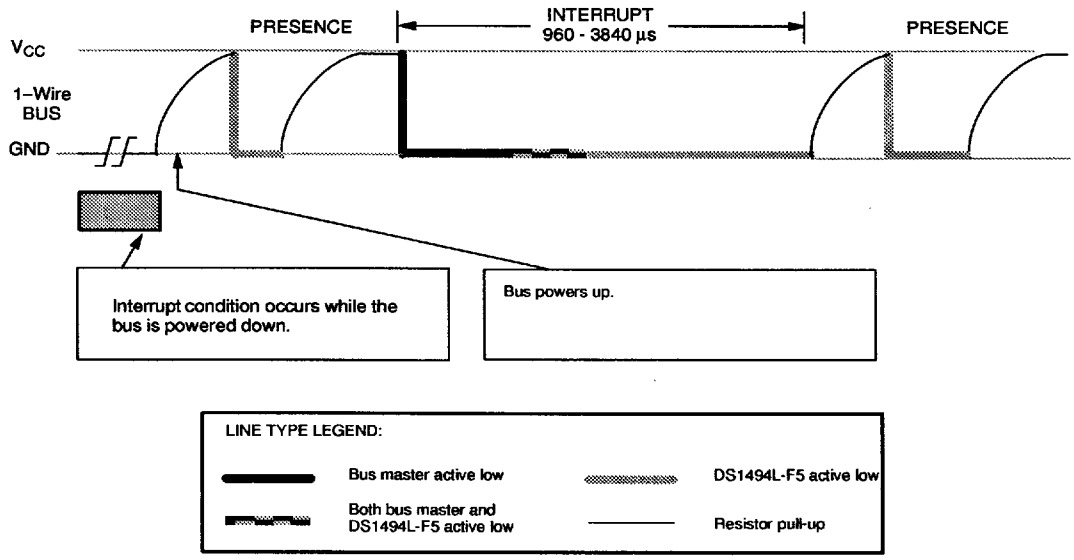
TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15



TYPE 2 INTERRUPT Figure 16



TYPE 2 INTERRUPT (SPECIAL CASE) Figure 17



PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	The DS1494L-F5 contains a small battery which is a lithium type. These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium-powered devices.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8V to 6.0V, -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @ 1 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

AC ELECTRICAL CHARACTERISTICS

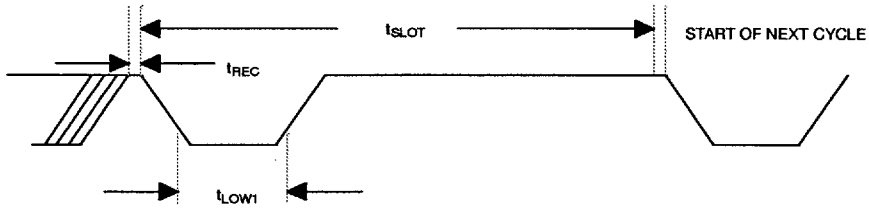
(-40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}	15			µs	
Read Data Setup	t_{SU}			1	µs	5
Interrupt	t_{INT}	960		4800	µs	
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

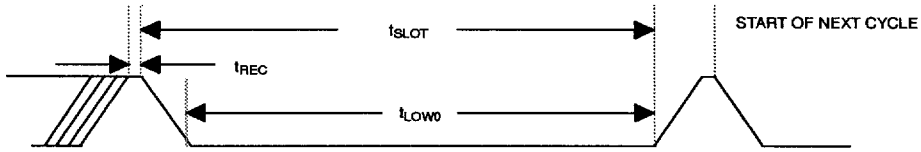
NOTES

1. All voltages are referenced to ground.
2. V_{PUP} = external pull-up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1-wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1-wire bus.)
6. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signalling, otherwise, it could mask or conceal interrupt pulses.

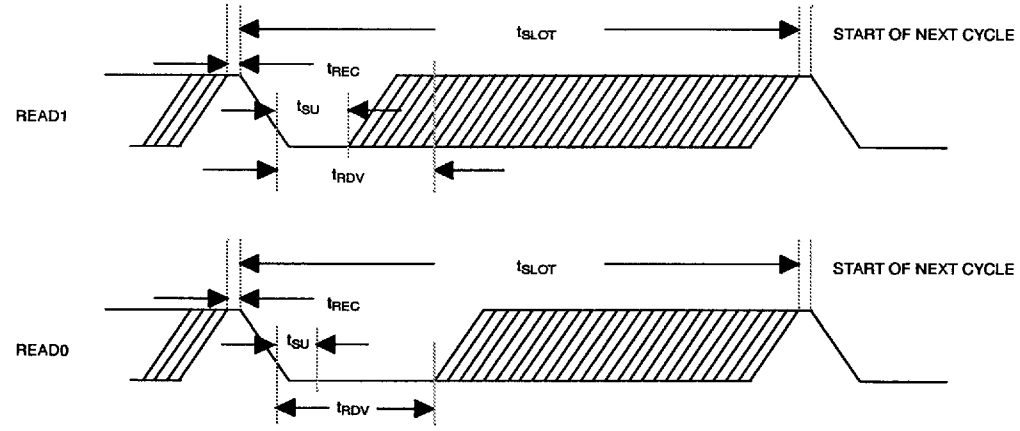
1-WIRE WRITE ONE TIME SLOT Figure 18



1-WIRE WRITE ZERO TIME SLOT Figure 19



1-WIRE READ TIME SLOTS Figure 20



1-WIRE PRESENCE DETECT Figure 21