MOTOROLA

MCM68364

64K-BIT READ ONLY MEMORY

The MCM68364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and is TTL compatible. The addresses are latched with the Chip Enable input — no external latches required.

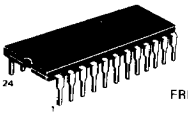
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ±10% 5-Volt Power Supply
- Automatic Power Down
- Low Power Dissipation
  - 150 mW active (typical)
  - 35 mW standby (typical)
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time
  - 200 ns — MCM68364-20
  - 250 ns — MCM68364-25
  - 300 ns — MCM68364-30
- Pin Compatible with 8K — MCM68A308, 16K — MCM68A316E, and 32K — MCM68A332 Mask-Programmable ROMs
- Pin Compatible with 24-pin 64K EPROM MCM68764

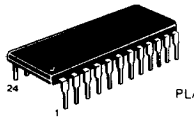
MOS

(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT
READ ONLY MEMORY

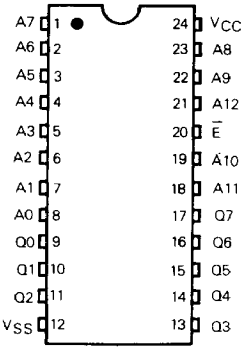


C SUFFIX
FRIT-SEAL PACKAGE
CASE 623



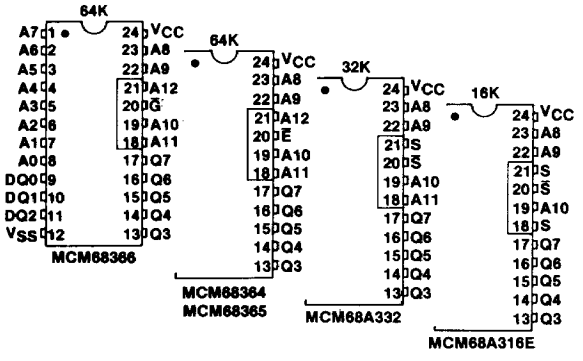
P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT



PIN NAMES	
A0-A12	Address
$\overline{E}$	Chip Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

MOTOROLA'S PIN COMPATIBLE ROM FAMILY

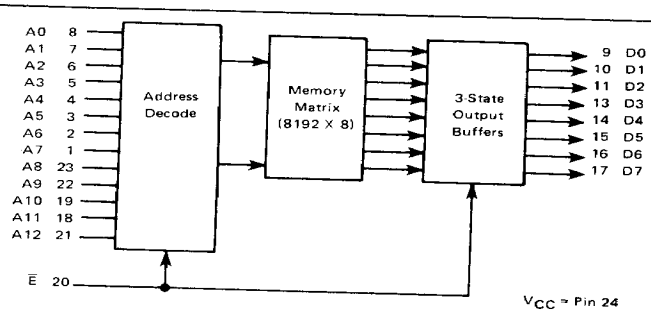


INDUSTRY STANDARD PIN-OUTS

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ROM

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved, $\overline{E} = V_{IH}$)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	—	10	μA
Output High Voltage (I_{OH} = −220 μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0 V to 5.5 V)	I_{LO}	−10	—	10	μA
Supply Current — Active* (Minimum Cycle Rate)	I_{CC}	—	25	40	mA
Supply Current — Standby ($\overline{E}$ = V_{IH})	I_{SB}	—	7	10	mA

*Current is proportional to cycle rate.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

ROM

AC OPERATING CONDITIONS AND CHARACTERISTICS

Read Cycle

RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with $t_r = t_f$ = 20 ns, loads of Figure 1)

Parameter	Symbol		MCM68364-20		MCM68364-25		MCM68364-30		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Chip Enable Low of Next Cycle (Cycle Time)	t_{ELEL}	t_{CYC}	300	–	375	–	450	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	200	–	250	–	300	–	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	200	–	250	–	300	ns
Chip Enable High to Output High Z (Off Time)	t_{EHQZ}	t_{EHZ}	10	60	–	60	–	75	ns
Chip Enable Low to Address Don't Care (Hold)	t_{ELAX}	t_{AH}	60	–	60	–	75	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable Precharge Time	t_{EHEL}	t_{EP}	100	–	125	–	150	–	ns

TIMING DIAGRAM

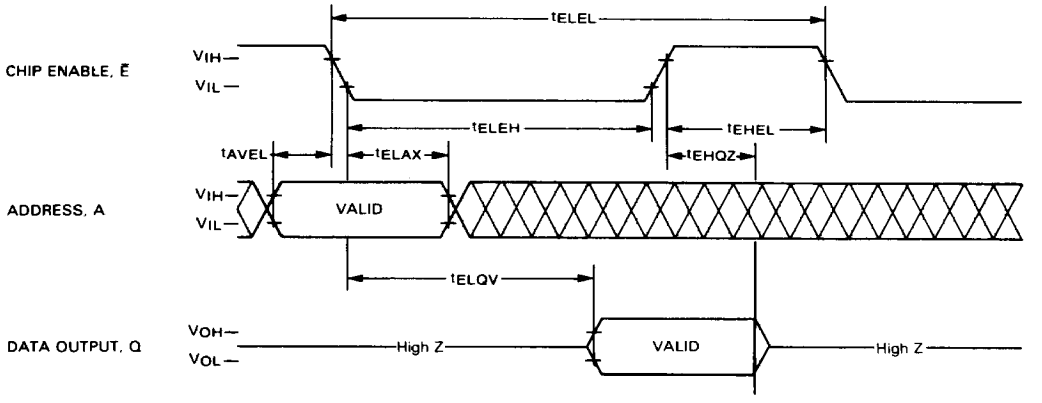
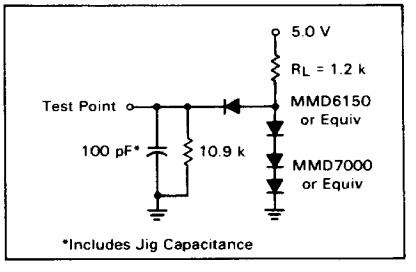


FIGURE 1 – AC TEST LOAD



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
———		
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

ROM

PRODUCT DESCRIPTION

This Motorola MOS Read Only Memory (ROM), the MCM68364, is a clocked or edge enabled device. It makes use of virtual ground ROM cells and clocked peripheral circuitry, allowing a better speed-power product.

The MCM68364 has a period during which the non-static periphery must undergo a precharge. Therefore, the cycle time is slightly longer than the access time. It is essential that the precharge requirements are met to ensure proper address latching and avoid invalid output data. Once the address hold time has been met, new address information can be supplied in preparation for the next cycle.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68364, the customer may specify the contents of the memory.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K (MCM68764), two 32K, or four 16K (MCM2716 or TMS2716).
2. Magnetic Tape — 9 Track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.

PRE-PROGRAMMED MCM68364P25-3

The −3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most significant digit.

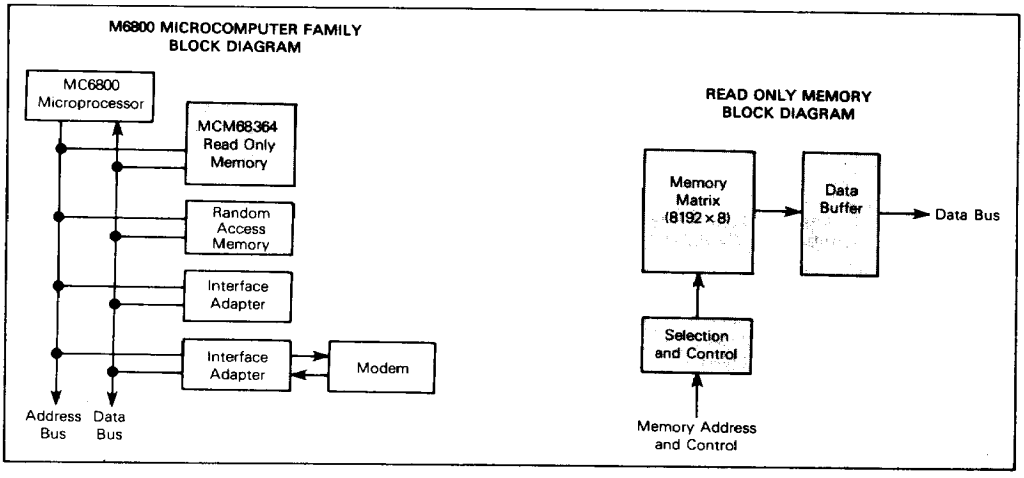
Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example:
$\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111



ROM