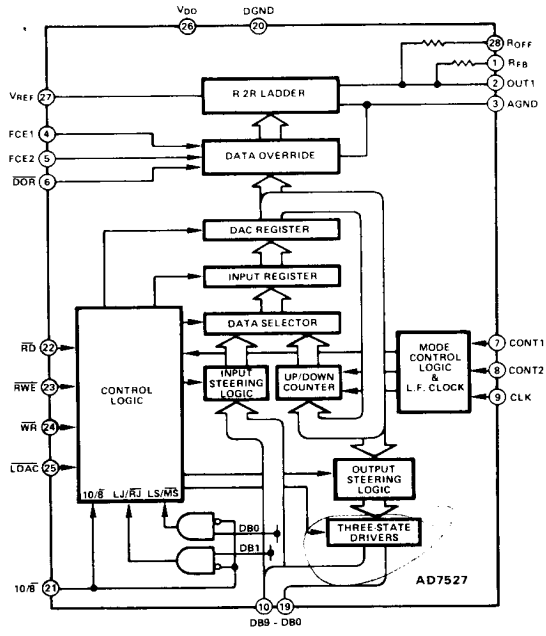
CMOS 10-Bit (Systems) DAC

AD7527

FEATURES
- Double Buffer Latches/Counter
- Data Readback
- 8- and 16-Bit Bus Compatible
- ±1LSB max Gain Error ("G" version)
- Easy Calibration Features
- Latch Proof (No Schottky Protection Required)

TYPICAL APPLICATIONS
- 4-20mA Loop Control
- Tracking ADCs
- S/D Converters
- Intelligent Instruments
- A.T.E.

AD7527 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7527 is a 10-bit monolithic CMOS systems DAC with extensive pin programmable logic functions. It interfaces directly with 8- or 16-bit data busses. The contents of the internal register can be written into and read from in left or right hand justified format.

The internal register data can be incremented or decremented using three control pins. The device includes an on-chip oscillator which may be used for incrementing or decrementing: alternatively an external clock can be used. System initialization and calibration is facilitated by a data override function which forces the DAC logic inputs to one of three override values for a zero, half or full scale output.

Two equal and matched feedback resistors are included on the die to facilitate 4-20mA circuits and other applications requiring matched resistors. The device has a low gain temperature coefficient of typically 2ppm/°C with a maximum of 5ppm/°C.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error +25°C	Temperature Range and Package 0 to +70°C	-25°C to +85°C	-55°C to +125°C
±1LSB	±10LSB	AD7527KN	AD7527BD	AD7527TD
±1/2LSB	±5LSB	AD7527LN	AD7527CD	AD7527UD
±1/2LSB	±1LSB	AD7527GLN	AD7527GCD	AD7527GUD

Analog Devices is offering the AD7527 in chip carriers. For information contact the factory.

PACKAGE IDENTIFICATION[1]

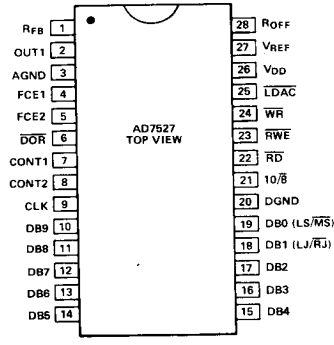
Suffix D: Ceramic DIP – (D28B)
Suffix N: Plastic DIP – (N28A)

[1] See Section 20 for package outline information.

Ceramic parts are available screened to MIL-STD-883, Method 5004 Para. 3.1.1 through 3.612 for a Class B device. To order add /883B to part number.

28-PIN DIP

PIN CONFIGURATION (NOT TO SCALE)



10

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V unless otherwise noted)

Parameter	Limit[1] at T_A = +25°C	Limit[1] at 0, +70°C and -25°C, +85°C	Limit[1] at -55°C, +125°C	Units	Conditions/Comments
STATIC PERFORMANCE					
Resolution	10	10	10	Bits	
Relative Accuracy[2]					
AD7527KN, BD, TD	±1	±1	±1	LSB max	
AD7527LN, CD, UD	±0.5	±0.5	±0.5	LSB max	
AD7527GLN, GCD, GUD	±0.5	±0.5	±0.5	LSB max	
Differential Nonlinearity[2]					
AD7527KN, BD, TD	±2	±2	±2	LSB max	Guaranteed 9-Bit Monotonic, T_{min} to T_{max}
AD7527LN, CD, UD	±1	±1	±1	LSB max	Guaranteed 10-Bit Monotonic, T_{min} to T_{max}
AD7527GLN, GCD, GUD	±1	±1	±1	LSB max	Guaranteed 10-Bit Monotonic, T_{min} to T_{max}
Gain Error[2]					Using internal R_{FB} only. Gain Error can
AD7527KN, BD, TD	±10	±10	±10	LSB max	be trimmed to zero using circuits of
AD7527LN, CD, UD	±5	±5	±5	LSB max	Figures 11, 12 and 13.
AD7527GLN, GCD, GUD	±1	±1	±2	LSB max	
R_{FB} to R_{OFF} Resistance Match	±0.2	±0.2	±0.2	% max	
Average Gain Temperature Coefficient, ΔG/ΔT					
T_{min} to +25°C	–	5	5	ppm/°C max	
+25°C to T_{max}	–	5	5	ppm/°C max	
dc Supply Rejection[2] ΔGain/ΔV_{DD}	0.005	0.005	0.005	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current[2] OUT1 (pin 2)	10	10	200	nA max	DAC Register Loaded with All 0s.
DYNAMIC PERFORMANCE					
DAC Register Propagation Delay[2,3]	950	950	950	ns max	OUT1 Load = 100Ω‖13pF Measured from Leading Edge of $\overline{WR}$ to 90% of Final Output Current for Full Scale Change.
Digital Charge Injection[2,3]	300	300	300	nV sec typ	Measured with ADLH0032CG as Output Amplifier. C1 of Figure 11 is 33pF. Pin 28 to AGND.
Multiplying Feedthrough Error[2,3]	2	2	4	mV p-p max	V_{REF} = ±10V, 10kHz Sine Wave. (See Application Hint Number 4). Pin 28 to AGND.
Small Signal Bandwidth	100	100	100	kHz typ	Using Circuit of Figure 11.
Input Resistance at V_{REF}, R_{FB}, R_{OFF} (pins 27, 1, 28 Respectively)	7 20	7 20	7 20	kΩ min kΩ max	Typical Input Resistance is 13kΩ.
Input Resistance Temperature Coefficient	-300	-300	-300	ppm/°C typ	
Analog Output Capacitance C_{OUT1} (pin 2)[3]	230	230	230	pF max	DAC Register Loaded with 1111111111
C_{OUT1} (pin 2)[3]	75	75	75	pF max	DAC Register Loaded with 0000000000
DIGITAL CONTROL INPUTS					Excluding CLK (pin 9) and DATA Bus (pins 10–19)
Input HIGH Voltage, V_{IH}	3.0	3.0	3.0	V min	
Input LOW Voltage, V_{IL}	0.8	0.8	0.8	V max	
Input Leakage Current, I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance, C_{IN}[3]	8	8	8	pF max	
CLOCK INPUT (PIN 9)					
Input HIGH Voltage, V_{IH}	3.8	3.8	3.8	V min	Input is a Schmitt Trigger.
Input LOW Voltage, V_{IL}	0.5	0.5	0.5	V max	
Input HIGH Current, I_{IH}	1.5	1.5	1.5	mA max	V_{IN} = +5V
Input LOW Current, I_{IL}	±1	±1	±1	μA max	V_{IN} = 0V
DATA BUS (PINS 10–19)					
Input HIGH Voltage, V_{IH}	3.0	3.0	3.0	V min	
Input LOW Voltage, V_{IL}	0.8	0.8	0.8	V max	
Output HIGH Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
Output LOW Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
Leakage Current per pin	±1	±10	±10	μA max	Outputs in high impedance state.
Capacitance per pin[3]	10	10	10	pF max	Outputs in high impedance state.
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V	
I_{DD}	5	5	5	mA max	V_{IN} = V_{IL} or V_{IH}; Data bus in high impedance state.
	500	500	500	μA max	V_{IN} = 0 or V_{DD}; Data bus in high impedance state.

NOTES:
[1] Temperature Ranges as follows: KN, LN, GLN versions, 0 to +70°C
BD, CD, GCD versions, -25°C to +85°C
TD, UD, GUD versions, -55°C to +125°C
[2] See Terminology
[3] Guaranteed but not tested.
[4] Logic inputs are MOS gates. Typical input current at +25°C is less than 1nA.
[5] Sample tested at +25°C to ensure compliance.
[6] For write timing, data bus reference levels are 0.8V (V_{IL}) and 3.0V (V_{IH}), see Figure 3. For read timing, data bus reference levels are 0.4V (V_{OL}) and 2.4V (V_{OH}), measured with a 10kΩ pull-down resistor.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[5] (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V unless otherwise noted)

Parameter	Limit[1] at T_A = +25°C	Limit[1] at 0, +70°C and -25°C, +85°C	Limit[1] at -55°C, +125°C	Units	Conditions/Comments
DATA WRITE[6]					
t_{DS}	300	360	450	ns min	Data valid setup time for 10-bit bus mode & 8-bit bus mode, right justified data.
t_{DS}	425	520	570	ns min	Data valid setup time for 8-bit bus mode, left justified data.
t_{DH}	0	0	0	ns min	Data valid hold time.
t_{WS}	240	275	325	ns min	Write control setup time.
t_{WH}	0	0	0	ns min	Write control hold time.
t_{WP}	180	220	250	ns min	Write pulse width.
DATA READ[6]					
t_{RS}	0	0	0	ns min	Read control setup time.
t_{RH}	0	0	0	ns min	Read control hold time.
t_{RP}	175	240	265	ns min	Read pulse width, C_L = 20pF
	300	400	450	ns min	C_L = 100pF
t_{RAD}	175	240	265	ns min	Data access time, C_L = 20pF
	300	400	450	ns min	C_L = 100pF
t_{RHD}	50	70	100	ns min	Data hold time.
	120	140	150	ns max	

See notes on Specifications page

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . 0, +7V
V_{DD} to AGND . . . . . 0, +7V
AGND to DGND . . . . . 0, V_{DD}
DGND to AGND . . . . . 0, V_{DD}
Digital Input Voltage to DGND
(pins 4-9, 21-25) . . . . . -0.3V, +17V
Digital Bus Voltage to DGND
(pins 10-19) . . . . . -0.3V, V_{DD} +0.3V
V_{PIN2} to AGND . . . . . -0.3V, +17V
V_{PIN1}, V_{PIN27}, V_{PIN28} to AGND . . . . . ±25V

Operating Temperature Range
KN, LN, GLN . . . . . 0 to +70°C
BD, CD, GCD . . . . . -25°C to +85°C
TD, UD, GUD . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Package)
Plastic (Suffix N)
To +50°C 1200mW
Derate above +50°C by . . . . . 12mW/°C
Ceramic (Suffix D)
To +50°C 1000mW
Derate above +50°C by . . . . . 10mW/°C

10

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	RFB	Feedback Resistor. Used for normal unity gain (at full scale) D/A conversion.
2	OUT1	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
3	AGND	Analog Ground.
4	FCE1	Force 1 Input. See pin 6 description.
5	FCE2	Force 2 Input. See pin 6 description.
6	$\overline{DOR}$	Data Override Input. This function allows the user to force the DAC logic inputs to one of three override values for calibration and reset. The value which the DAC output assumes is determined by the logic levels on the Forcing inputs, FCE1 and FCE2.

$\overline{DOR}$	FCE2	FCE1	DAC INPUT
1	X	X	DAC Register Contents
0	0	0	0000000000
0	0	1	1000000000
0	1	X	1111111111

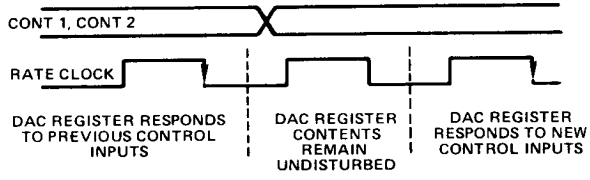
X = Don't Care

Data in the input and DAC registers are not affected in any way by the data override. They may be written to or read from as in normal operation. When the override signal is removed the DAC output returns to reflect the value in the DAC register.

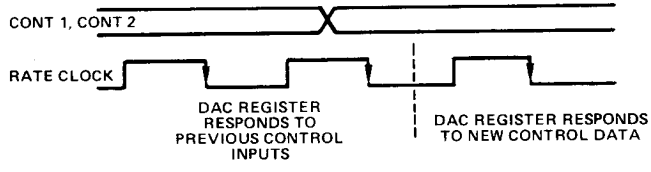
7	CONT1	Control Input 1. See pin 8 description.
8	CONT2	Control Input 2. This signal, in combination with CONT1 (pin 7) is used to determine the AD7527 operating mode, either *load* or *count* mode. In the *load* mode all AD7527 data WRITE, READ and LOAD operations are via the data bus and control inputs. In the *count* mode external data on the data bus cannot be written into the AD7527, the $\overline{WR}$ and $\overline{LDAC}$ signals are ignored; however, the contents of the DAC register can still be read. In this mode the input and DAC registers are driven as an internal up/down counter. The up/down counter operation is controlled by the CONT1, CONT2 signals. CONT1, CONT2 encoding is as follows:

CONT1	CONT2	MODE	FUNCTION
0	0	*Load*	Control is via data bus and control inputs
0	1	*Count*	Increment input and DAC Registers
1	0	*Count*	Decrement input and DAC Registers
1	1	*Count*	Input and DAC Register contents frozen

End stop logic prevents the up/down counter from being incremented beyond all 1s or decremented below all 0s. The increment/decrement rate is controlled by the rate frequency on the CLK input (pin 9). The response of the AD7527 to a change in the control inputs depends on the state of the rate clock (HIGH or LOW) at the time the change occurs.



Case 1. Rate Clock LOW When Controls Change



Case 2. Rate Clock HIGH When Controls Change

A status flag is available via the data bus to indicate whether the AD7527 is in the *load* mode (flag HIGH) or *count* mode (flag LOW).

9	CLK	Clock Input. Controls the input and DAC registers increment/decrement rate when the AD7527 is in the *count* mode. Connecting an external resistor to V_{DD} and capacitor to ground completes an internal low frequency clock circuit, see Figure 4. Alternatively CLK may be driven by an external clock frequency of up to 1MHz.
10	DB9	Data Bit 9. Most Significant Bit (MSB).
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.

18	DB1 (LJ/$\overline{RJ}$)	Pin function is dependent upon the 10/$\overline{8}$ (pin 21) input. Pin 21 HIGH; pin 18 is Data Bit 1 (DB1) input. Pin 21 LOW; pin 18 is left-justified/right-justified (LJ/$\overline{RJ}$) control input.
19	DB0 (LS/$\overline{MS}$)	Pin function is dependent upon the 10/$\overline{8}$ (pin 21) input. Pin 21 HIGH; pin 19 is Data Bit 0 (DB0) input. Pin 21 LOW; pin 19 is Least Significant Byte/Most Significant Byte (LS/$\overline{MS}$) control input.
20	DGND	
21	10/$\overline{8}$	10/8-Bit Control Input. When 10/$\overline{8}$ is HIGH the AD7527 data port is 10-bits wide (DB9–DB0). This allows single byte (10-bit) write and read operations when using 16-bit data busses. When 10/$\overline{8}$ is LOW the AD7527 data port is reduced to 8-bits wide (DB9–DB2). This mode simplifies interfacing to 8-bit data busses and data is loaded or read in two bytes. In this double byte mode LJ/$\overline{RJ}$ (pin 18) and LS/$\overline{MS}$ (pin 19) pass data format information to the AD7527.
22	$\overline{RD}$	READ Input. This active low signal, in combination with $\overline{RWE}$ (pin 23), is used to enable the three-state drivers which place the DAC register contents on the external data bus. The data output format is dependent upon control input 10/$\overline{8}$ and is shown in Figure 3. The contents of the DAC register can be read in either of the AD7527 operating modes—*count* mode or *load* mode.
23	$\overline{RWE}$	READ WRITE ENABLE Input, Active Low. When the AD7527 is in the *load* mode a LOW on $\overline{RWE}$ enables data transfers to or from the AD7527 via the external data bus. When $\overline{RWE}$ is HIGH the external data bus is locked out. Data present in the input register can still be transferred to the DAC register.
24	$\overline{WR}$	WRITE Input. This active low signal, in combination with others, is used in loading external data into the AD7527 registers and in transferring data from the input register to the DAC register. The data is latched into its destination register (input register, DAC register or both) when $\overline{WR}$ returns high. The $\overline{WR}$ input has no effect when the AD7527 is in the *count* mode.
25	$\overline{LDAC}$	Load DAC input, active low. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus. The $\overline{LDAC}$ input has no effect when the AD7527 is in the *count* mode.
26	V_{DD}	+5V Supply Input.
27	V_{REF}	Reference Voltage Input.
28	R_{OFF}	Offset Bias Resistor, $R_{OFF} = R_{LAD} = R_{FB}$. If not used, it is recommended that this pin be connected to AGND to minimize noise injection.

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7527, ideal full-scale output is V_{REF} (1023/1024). Gain error is adjustable to zero.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with the DAC register loaded to all 0s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

POWER SUPPLY REJECTION
Power supply rejection is a measure of the sensitivity of the DAC full-scale output to the effect of power supply changes.

PROPAGATION DELAY
This is a measure of the internal circuit delays and is defined as the time from the leading edge of $\overline{WR}$ to the analog output current reaching 90% of its final value for a full scale change.

LSB
This is an abbreviation for Least Significant Bit. For an n-bit converter, $1LSB = V_{REF}/2^n$.

FSR
This is an abbreviation for Full Scale Range. For a 10-bit converter with a reference input of 10V the FSR is 10 X (1023/1024) volts.

DIGITAL CHARGE INJECTION
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs. Digital charge injection is measured with V_{REF} = AGND.

GENERAL CIRCUIT INFORMATION

D/A CONVERTER SECTION

The AD7527 10-bit multiplying D/A converter section consists of a highly stable thin-film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

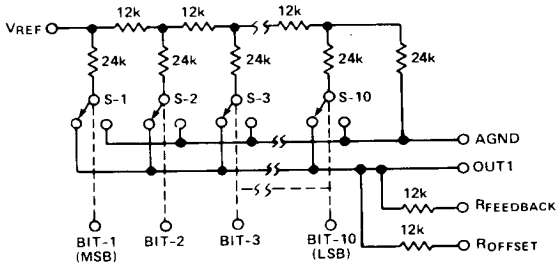


Figure 1. AD7527 Functional Diagram

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 75pF (all switches to AGND) to 230pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

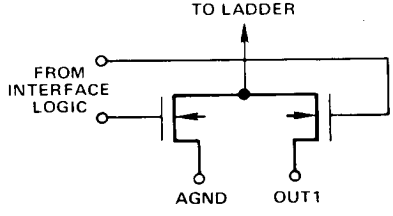
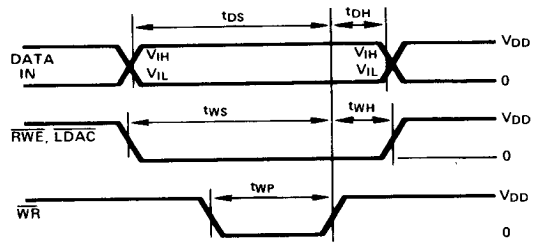


Figure 2. N-Channel Current Steering Switch

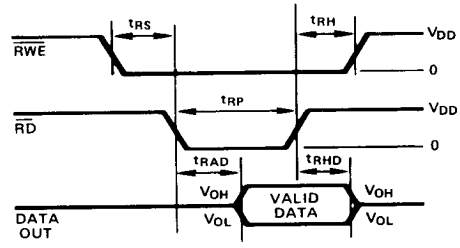
CONTROL INPUT INFORMATION

READ/WRITE

Figure 3 shows generalized WRITE and READ timing diagrams for the AD7527. Dynamic specifications are included on specifications page. A typical setup time of 250ns is required by the AD7527 when changing from the 10-bit bus mode to the 8-bit bus mode or vice versa.



a. Write Timing



b. Read Timing

NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. DATA OUT TIMING MEASUREMENTS ARE FROM $V_{OH} = 2.4V$, $V_{OL} = 0.4V$.

Figure 3. AD7527 Timing Diagrams

DATA TRANSFER

A truth table for the data transfer control inputs is shown in Table 1. When the AD7527 is in the 10-bit communications mode (10/$\overline{8}$ HIGH) each write and read function of Table 1 can be executed in a single byte operation. When the AD7527 is in the 8-bit communications mode (10/$\overline{8}$ LOW) 10-bit data write and read functions are two byte operations.

$\overline{LDAC}$	$\overline{RD}$	$\overline{WR}$	$\overline{RWE}$	Function
X	X	X	1	External Data Transfer does not take place
1	1	0	0	Write Data from input bus to Input Register
0	1	0	0	Write Data from input bus to Input Register and DAC Register
X	0	1	0	Read Data to input bus from DAC Register
0	1	0	1	Transfer Data from Input Register to DAC Register

X = "Don't Care" States

Table 1. AD7527 Data Transfer Truth Table (Reading and Writing Data)

INTERNAL CLOCK

Figure 4 shows typical internal oscillator frequency versus R and C. Due to process variations the actual operating frequency for a given RC from Figure 4 can vary from device to device by up to ±10% from the calculated value. The internal oscillator frequency has a typical temperature coefficient of ±200ppm/°C.

The internal oscillator frequency supply rejection is dependent on the operating frequency. For low frequencies (tens of Hz) in the linear regions of Figure 4 it is typically ±0.01%/%. For higher frequencies (hundreds of Hz) in the linear regions of Figure 4 it is typically +0.35%/%. Operation in the nonlinear regions for any frequency will degrade the frequency supply rejection.

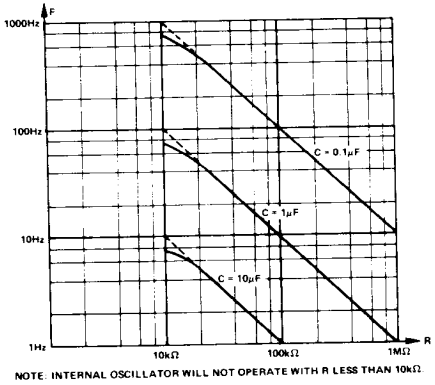


Figure 4. f_{CLK} versus R, C

8-BIT COMMUNICATIONS MODE (10/$\overline{8}$ LOW)

Data Write (8-Bit Bus Mode)

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations depending on control inputs LJ/$\overline{RJ}$ and LS/$\overline{MS}$. For left justified data LJ/$\overline{RJ}$ is held HIGH. For right justified data LJ/$\overline{RJ}$ is held LOW. The data protocol is determined by LS/$\overline{MS}$. A logic HIGH on LS/$\overline{MS}$ signals the least significant byte is to be loaded; a logic LOW signals the most significant byte is to be loaded. The data possibilities are shown in Figure 5.

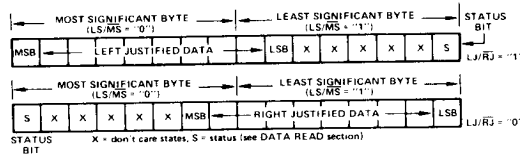


Figure 5. Formatting a 10-Bit Data Word

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the second write cycle. Figure 6 shows the timing diagram for this mode. A third write cycle is required for the strobed transfer mode. This allows the AD7527 DAC updating to be synchronized with a master strobe signal in systems where update timing is important. Figure 7 illustrates the timing of this mode.

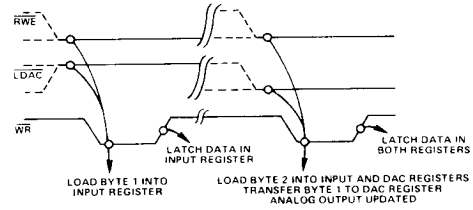


Figure 6. 8-Bit Loading, Automatic Transfer Mode

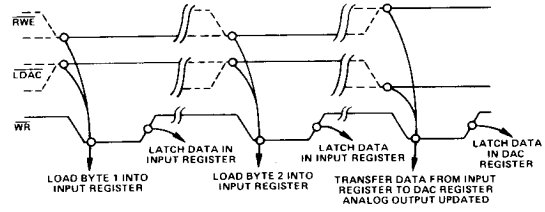


Figure 7. 8-Bit Loading, Strobed Transfer Mode

Data Read (8-Bit Bus Mode)
Two read cycles are required to place the contents of the 10-bit DAC register onto the external data bus. Since the data in the DAC register is already either left or right justified the data format control input LJ/$\overline{RJ}$ must reflect this formatting to avoid data misinterpretation. The LS/$\overline{MS}$ control input determines which byte is placed on the bus. The three-state drivers are enabled when $\overline{RD}$ goes low.

The status flag which indicates whether the AD7527 is in the *load* or *count* mode is only available when control input 10/$\overline{8}$ is low. The status flag can only be read. From Figure 5 the status bit is the most right-hand bit in a 16-bit left justified word and the most left-hand bit in a 16-bit right justified word. The status bit can be shifted into a microprocessor's accumulator carry position for testing. Note that the "don't care" states of Figure 5 are driven by the AD7527 three-state drivers during a data read operation. The status flag is high when the AD7527 is in the *load* mode and low when in the *count* mode.

10-BIT COMMUNICATIONS MODE (10/$\overline{8}$ HIGH)
Data Write (10-Bit Bus Mode)
If the available data bus is at least 10 bits wide (e.g., when using 16-bit μPs) then full 10-bit parallel loading is possible. This is the simplest method of AD7527 data loading. A right justified or left justified data format is selected by bus wiring. Like the 8-bit communications mode, two operating modes are possible for controlling the transfer of data from the input register to the DAC register. The simplest is the automatic transfer mode which causes both the input and DAC registers to be loaded simultaneously with a single write cycle (see Figure 8). A second write cycle is required for the strobed transfer mode to allow DAC updating to be synchronized with a master strobe. Figure 9 illustrates this mode timing.

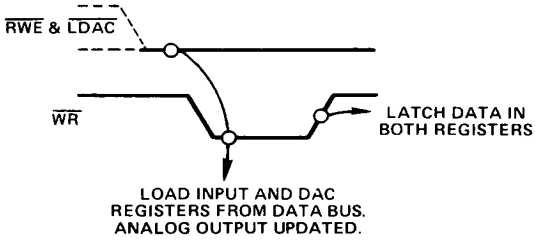


Figure 8. 10-Bit Loading, Automatic Transfer Mode

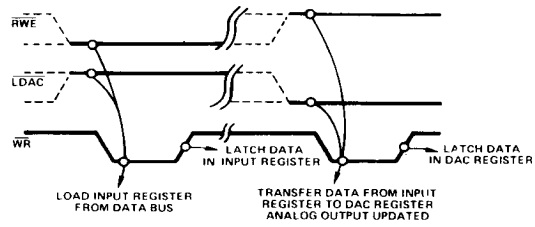


Figure 9. 10-Bit Loading, Strobed Transfer Mode

Data Read (10-Bit Bus Mode)
One read cycle is required to place the contents of the DAC register onto the external data bus. The three-state drivers are enabled when $\overline{RD}$ goes low.

The status flag is not directly available in the 10-bit communications mode but it can be obtained by using software control to switch the AD7527 to the 8-bit bus mode (see Figure 10). The two pull-up resistors on DB0 and DB1 automatically select, when 10/$\overline{8}$ goes low, the left justified data format, least significant byte. The processor can now read the status bit on DB2. When it has done so, it switches the AD7527 back to the 10-bit communications mode.

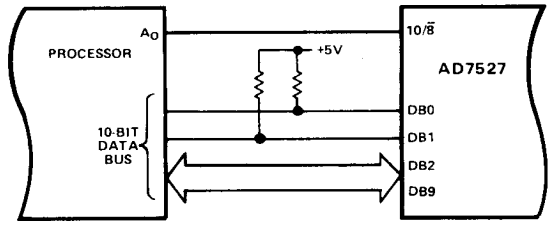


Figure 10. Reading Status Flag in 10-Bit Communications Mode

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 11 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity and the AD7527 offset input, R_{OFF} (pin 28), is tied to AGND. With a dc reference voltage or current (positive or negative polarity) applied at pin 27, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 2. When an offset voltage V_{OFF} is applied to pin 28, an extra term $-V_{OFF}$ is added to the analog output, V_{OUT}, of Table 2. To keep feedthrough to a minimum it is recommended that pin 28 be returned to a low impedance point, either AGND or an op-amp output.

For full scale trimming the DAC input is forced to 1111111111 either by using the data override function or by loading the DAC register with 1111111111. R1 is then adjusted for $V_{OUT} = -V_{REF}$ (1023/1024). Alternatively, full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Phase compensation capacitor C1 (10 to 25pF) may be required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1.

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of an LSB. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 12kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS} and low I_B.

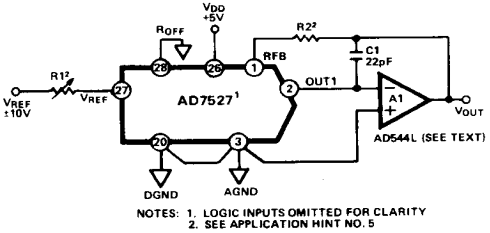


Figure 11. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$ = Full Scale
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -1/2\ V_{REF}$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	0V = Zero Scale

Table 2. Unipolar Binary Code Table for Circuit of Figure 11

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 12 and Table 3 illustrate the circuitry and code relationship for bipolar operation with offset binary coding. For half scale trimming (V_{OUT} = 0V) the DAC input is forced to 1000000000 either by using the data override function or by loading the DAC register with 1000000000. The ratio of R3 to R4 is then adjusted for V_{OUT} = 0V. Full scale trimming is similarly accomplished by forcing the DAC input to 1111111111 and adjusting R1 for $V_{OUT} = -V_{REF}/2$ (511/512). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage input.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. In fixed reference applications A2 can be a slow amplifier to minimize cost e.g., AD542L. However, A2 should still exhibit good offset and bias characteristics. For multiplying DAC applications A2 requires a bandwidth consistent with the V_{REF} bandwidth. R3 and R4 should be selected for matching and tracking over the temperature range of interest. Any mismatch will cause both offset and full scale errors. Phase compensation capacitor C1 (10pF to 25pF) may be required for stability.

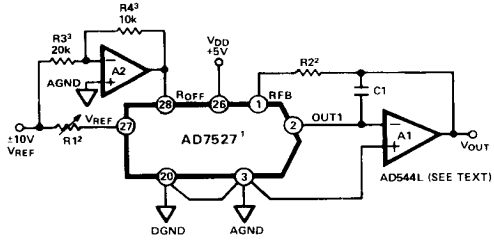


Figure 12. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$-\frac{V_{REF}}{2}\left(\frac{511}{512}\right)$
1000000001	$-\frac{V_{REF}}{2}\left(\frac{1}{512}\right)$
1000000000	0V
0111111111	$+\frac{V_{REF}}{2}\left(\frac{1}{512}\right)$
0000000000	$+\frac{V_{REF}}{2}\left(\frac{512}{512}\right)$

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 12

If the required analog output in bipolar operation is V_{OUT} = $\pm V_{REF}$ (as opposed to $\pm V_{REF}/2$ with Figure 12) then the AD7527 should be connected as shown in Figure 13. Table 4 illustrates the code relationship for this case.

For half scale trimming (V_{OUT} = 0V) the DAC input is forced to 1000000000 either by using the data override function or by loading the DAC register with 1000000000. R1 is then adjusted for V_{OUT} = 0V. Alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V. Full scale trimming is similarly accomplished by forcing the DAC input to 1111111111 and adjusting R5 for V_{OUT} = $+V_{REF}$ (511/512) or by varying the amplitude of V_{REF}.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking over the temperature range of interest. Mismatch of 2R3 to R4 causes both offset and full scale error. Mismatch of R5 and R4 and 2R3 causes full scale error. Phase compensation capacitor C1 (10pF to 25pF) may be required for stability.

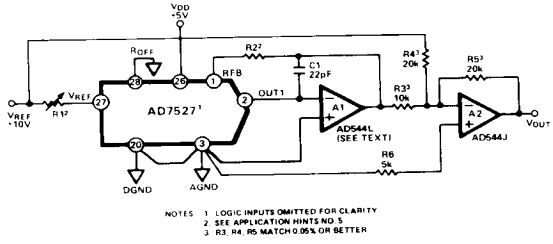


Figure 13. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$+V_{REF}\left(\frac{511}{512}\right)$
1000000001	$+V_{REF}\left(\frac{1}{512}\right)$
1000000000	0V
0111111111	$-V_{REF}\left(\frac{1}{512}\right)$
0000000000	$-V_{REF}\left(\frac{512}{512}\right)$

Table 4. Bipolar Code Table for Offset Binary Circuit of Figure 13

Figure 14 illustrates an arrangement to generate with two SPDT switches, one with center off, mode control signals for the AD7527. The truth table for CONT1 and CONT2 signals is shown under the pin function description of pin 8.

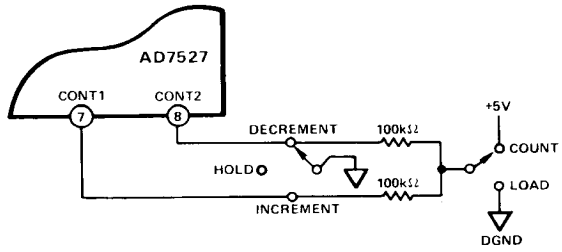


Figure 14. Typical Front Panel Mode Control Circuitry

4–20mA LOOP CIRCUITS

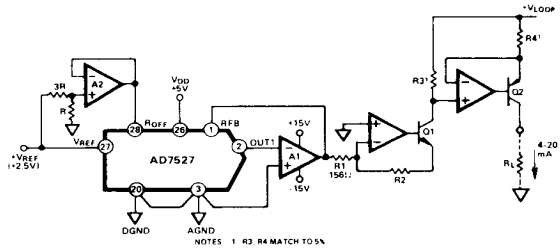


Figure 15. R_L Referenced to AGND

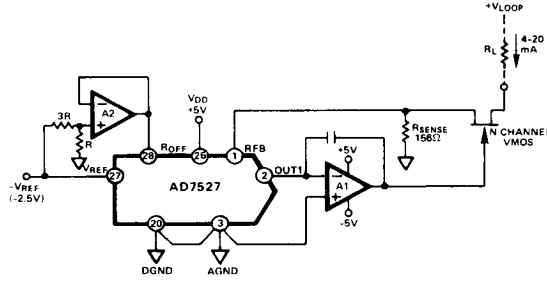


Figure 16. R_L Referenced to Positive Loop Supply

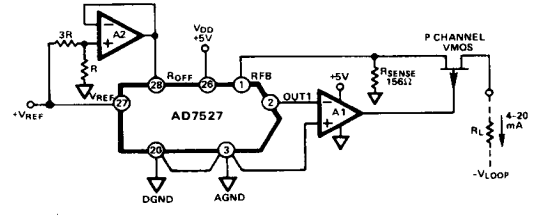


Figure 17. R_L Referenced to Negative Loop Supply (Note Single Supply Operation)

APPLICATION HINTS

To ensure system performance consistent with AD7527 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7527 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7527. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7527 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output of maximum magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7527 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. FEEDTHROUGH: The dynamic performance of the AD7527 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 11 is shown below which minimizes feedthrough from V_{REF} to the output in multiplying applications.

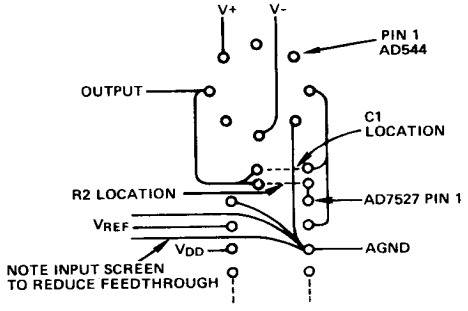


Figure 18. Suggested Layout Shows Copper Side (i.e. Bottom View)

5. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7527 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 0.51LSBs and 0.2LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full scale range as shown in Figures 11, 12 and 13, the temperature coefficients of the trim resistors should also be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:

$$\text{Temperature Coefficient Contribution Due to R1} = -\frac{R1}{R_{IN}} \quad (\gamma 1 + 300)$$

$$\text{Temperature Coefficient Contribution Due to R2} = +\frac{R2}{R_{IN}} \quad (\gamma 2 + 300)$$

Where $\gamma 1$ and $\gamma 2$ are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 27). For high quality wire-wound resistors γ = +50ppm/°C and for trimming potentiometers γ = ±50ppm/°C.

It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will be small. For the standard AD7527TD gain error specification of ±10LSBs it is recommended that R1 = 200Ω and R2 = 100Ω.

However if the AD7527GUD is used which has a specified gain error of ±1LSB it is recommended that R1 = 10Ω and R2 = 5Ω. With these values the maximum gain temperature coefficient is increased by only 0.34ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

6. For additional information on multiplying DACs refer to "Applications Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.