INTERSIL

2114
4096 Bit (1024x4) NMOS Static RAM

FEATURES

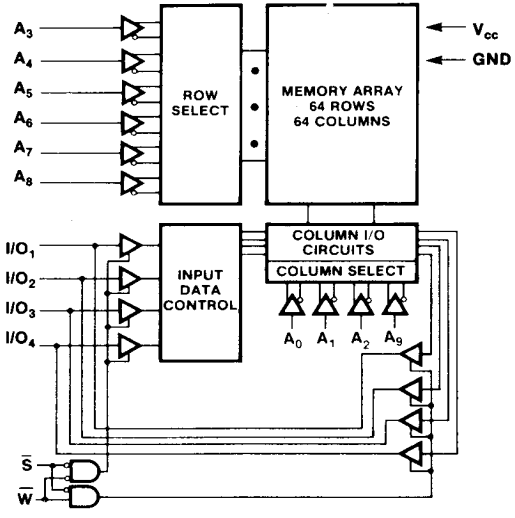
- **Cycle Time Equal to Access Time**
- **Completely Static - No Clock Required**
- **Common Data Input and Output**
- **TTL Compatible Inputs and Outputs**
- **883A Class B Processing Available**
- **Single +5 Volt Power Supply**
- **Pin Compatible with industry standard 2114**
- **Maximum Access Time:**
  - **-200 ns (-2)**
  - **-300 ns (-3)**
- **Maximum Power Dissipation:**
  - **-370 mW (2114L)**
  - **-525 mW (2114)**

DESCRIPTION

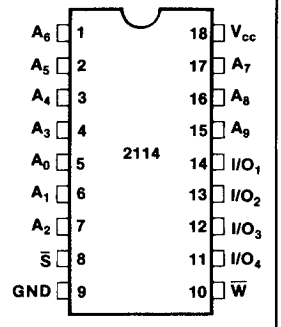
The 2114 is a 4096-bit static Random Access Memory organized 1024 words x 4 bits. The storage cells and decode and control circuitry are completely static, therefore no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 2114 is pin and performance compatible with the industry standard 2114 series, and the device is assembled in a standard 18-pin DIP for maximum system packing density.

BLOCK DIAGRAM

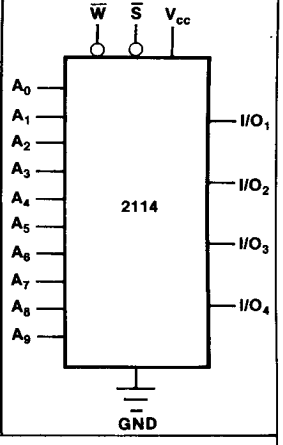


PIN CONFIGURATION



(outline dwgs JN,PN)

LOGIC SYMBOL



PIN NAMES

A_0-A_9	ADDRESS INPUTS
I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

POWER	ACCESS TIME 200ns	300ns	450ns	PACKAGE
370mW	D2114L2	D2114L3	D2114L	CERDIP
	P2114L2	P2114L3	P2114L	PLASTIC
525mW	D2114-2	D2114-3	D2114	CERDIP
	P2114-2	P2114-3	P2114	PLASTIC

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

PARAMETER	SYMBOL	TEST CONDITIONS	2114L		2114		UNITS
			MIN	MAX	MIN	MAX	
Input Load Current	I_{INLD}	V_{IN} = 0V to 5.25V		10		10	μA
Output Leakage Current	I_{OLK}	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10		10	μA
Power Supply Current	I_{CC2}	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = +25°C		65		90	mA
Power Supply Current	I_{CC1}	V_{IN} = +5.25V, $I_{I/O}$ = 0mA, T_A = 0°C		70		100	mA
Input Low Voltage	V_{IL}		−0.5	0.8	−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	2.0	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	2.4	V_{CC}	2.4	V_{CC}	V

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF

NOTE: These parameters are periodically sampled, not 100% tested.

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DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjunction with the other, can prevent the extraneous writing due to signal transitions.

A read occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high.

Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must to properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and Output Timing Reference Level = 1.5V

READ CYCLE

PARAMETER	SYMBOL	2114-2 2114L2		2114-3 2114L3		2114 2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	20		20		20		
Output Three-State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	50		50		50		

WRITE CYCLE

PARAMETER	SYMBOL	2114-2 2114L2		2114-3 2114L3		2114 2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output Three-State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	0		0		0		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

TIMING DIAGRAMS

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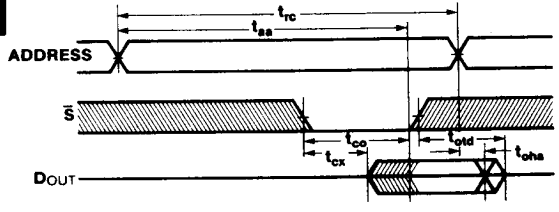
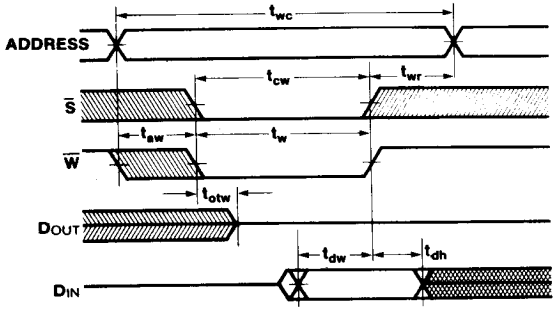
READ CYCLE

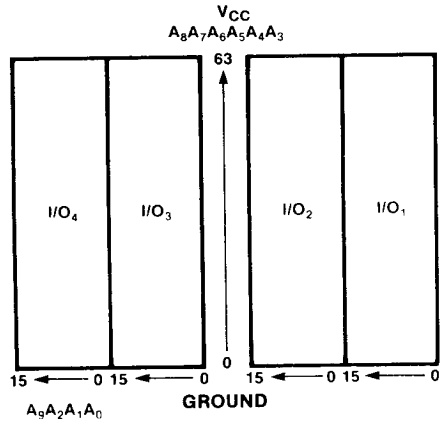


WRITE CYCLE



Note: $\overline{W}$ is high for a READ cycle.

2114 BIT MAP DIAGRAM



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