élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1881C
Sync Separator, Low Power

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Fixed 70 mV slicing of video input levels from 0.5 V_{P-P} to 2 V_{P-P}
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1881CN	−40°C to +85°C	8-pin DIP	MDP0031
EL1881CS	−40°C to +85°C	8-lead SO	MDP0027

Demo Board

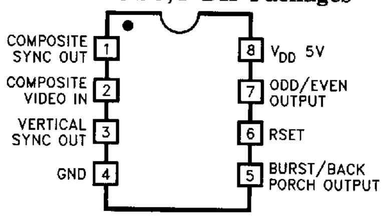
A dedicated demo board is not available. However, this device can be placed on the EL4584/5 demo board.

General Description

The EL1881C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing and odd/even field detection. Fixed 70 mV sync tip slicing provides sync edge detection when the video input level is between 0.5 Vp-p and 2 Vp-p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The **composite sync** output follows **video in** sync pulses, and a **vertical sync** pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The **odd/even** output indicates field polarity detected during the vertical blanking interval. The EL1881C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with lower required supply current.

Connection Diagram

EL1881C SO, P-DIP Packages



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Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Ambient Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C	Operating Junction Temperature	125°C
Lead Temperature (5 sec)	260°C	Power Dissipation	400 mW
Pin Voltages	−0.5V to V_{CC} + 0.5V		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise stated, V_{DD} = 5V, T_A = 25°C, R_{SET} = 681 kΩ

Parameter	Description	Min	Typ	Max	Test Level	Units
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3.0	I	mA
Clamp Voltage	Pin 2, Unloaded	1.35	1.5	1.65	I	V
Clamp Discharge Current	Pin 2 = 2V	3.2	12	16	I	µA
Clamp Charge Current	Pin 2 = 1V	−2.0	−1.5	−0.8	I	mA
R_{SET} Pin Reference Voltage	Pin 6	1.20	1.31	1.44	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA		0.4	0.8	I	V
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	4 2.4	4.8 3.5		IV I	V

Dynamic Characteristics

Parameter	Description	Min	Typ	Max	Test Level	Units
Comp Sync Prop Delay, t_{CS}	See Figure 2	20	45	90	I	ns
Vertical Sync Width, t_{VS}	Normal or Default trigger, 50%–50%	190	270	350	I	µs
Vertical Sync Default Delay, t_{VSD}	See Figure 3	35	65	85	I	µs
Burst/Back Porch Delay, t_{BD}	See Figure 2	250	450	650	I	ns
Burst/Back Porch Width, t_B	See Figure 2	2.5	3.6	4.5	I	µs
Input Dynamic Range	Video input amplitude to maintain 50% slice spec	0.5		2	I	V_{P-P}
Slice Level	V_{SLICE}/V_{CLAMP}	55	70	85	I	mV

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Pin Descriptions

Pin No.	Pin Name	Function
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video In	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	Gnd	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. A 681k 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. High during odd fields, low during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD} 5V	Positive supply. (5V)

Note: R_{SET} must be a 1% resistor.

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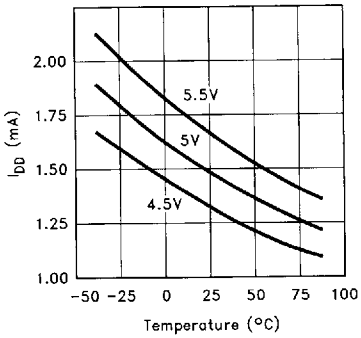
Typical Performance Curves

Supply Current, Quiescent
R_{SET} = 681k



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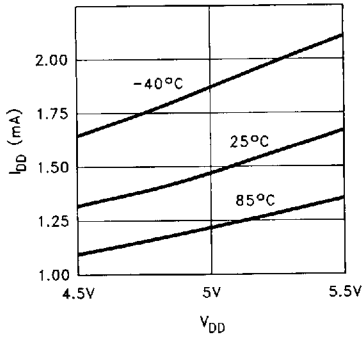
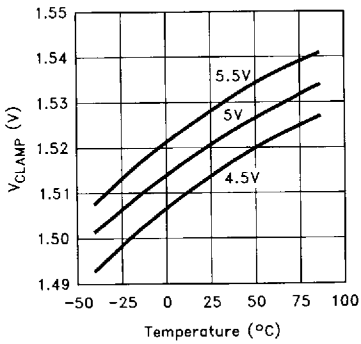
I_{DD} vs V_{DD}
R_{SET} = 681k



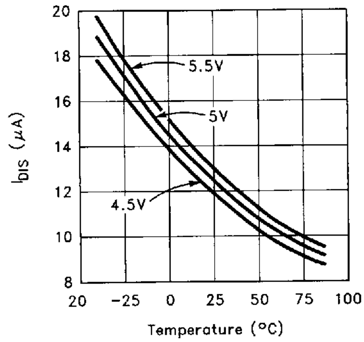
1881-3

V_{CLAMP} Voltage
R_{SET} = 681k



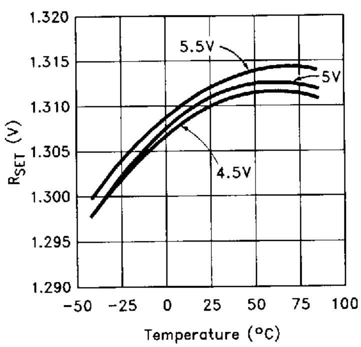
1881-4

Clamp Discharge Current
R_{SET} = 681k



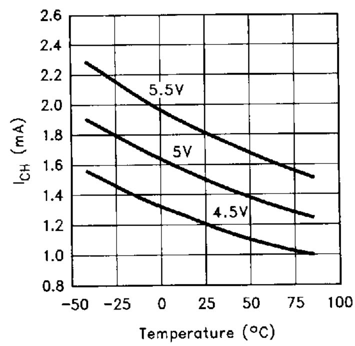
1881-5

V_{RSET}
R_{SET} = 681k



1881-6

Clamp Charge Current
R_{SET} = 681k



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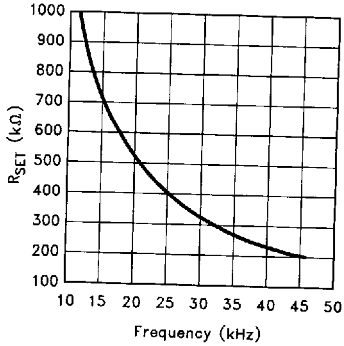
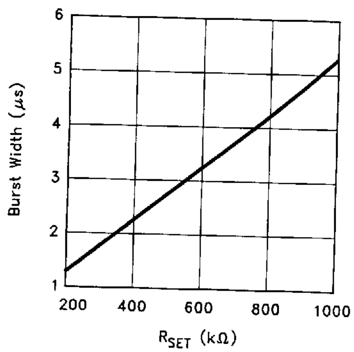
Typical Performance Curves — Contd.

R_{SET} vs Horizontal Frequency



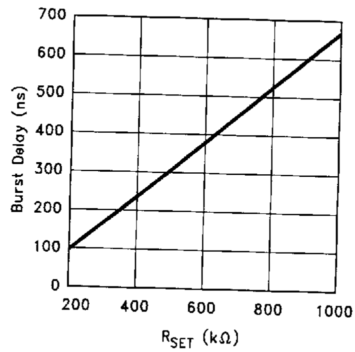
1881-8

Burst/Back Porch Width vs R_{SET}
V_{DD} = 5V, T = 25°C



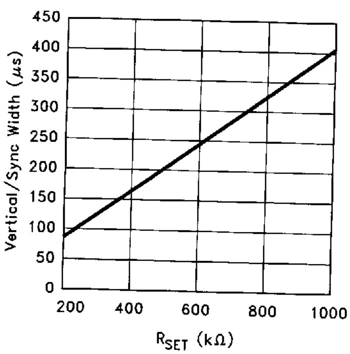
1881-9

Burst/Back Porch Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



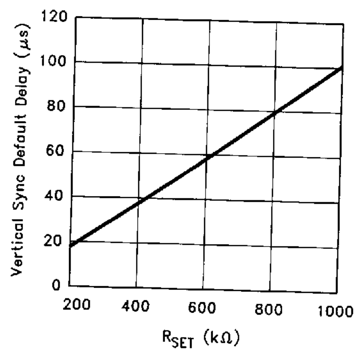
1881-10

Vertical Sync Width vs R_{SET}
V_{DD} = 5V, T = 25°C



1881-11

Vertical Default Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



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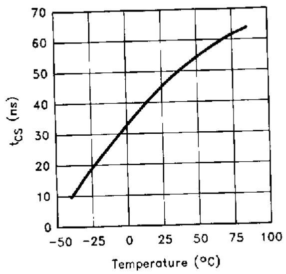
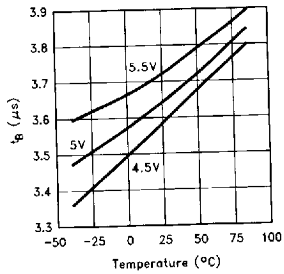
Typical Performance Curves — Contd.

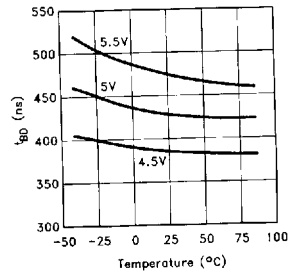
Composite Sync Prop Delay
R_{SET} = 681k, V_{DD} = 5V



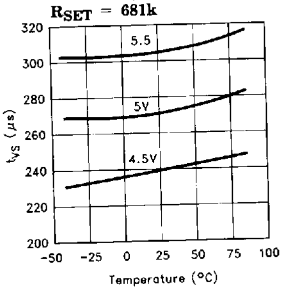
Burst/Back Porch Width,
R_{SET} = 681k



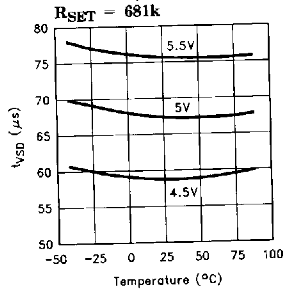
Burst/Back Porch Delay Time,
R_{SET} = 681k



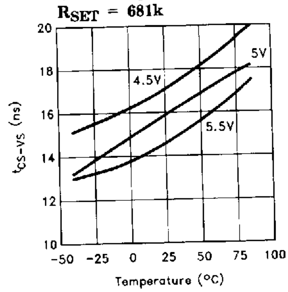
Vertical Sync Pulse Width
R_{SET} = 681k



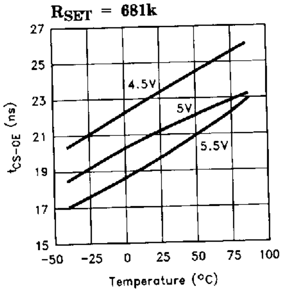
Vertical Sync Default Delay Time,
R_{SET} = 681k



Composite Sync to
Vertical Sync Delay Time
R_{SET} = 681k



Composite Sync to
Odd/Even Delay Time
R_{SET} = 681k



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Timing Diagrams

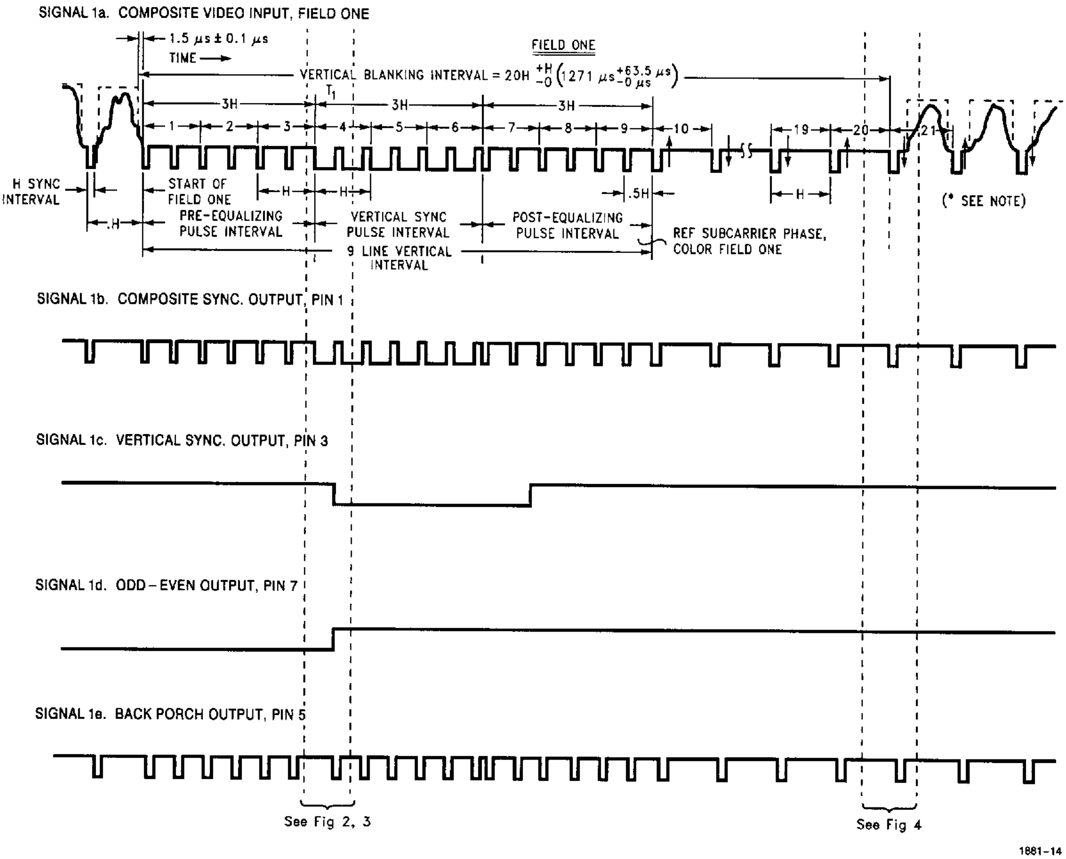

Figure 1. Standard (NTSC Input) Timing

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

Expanded Timing Diagrams

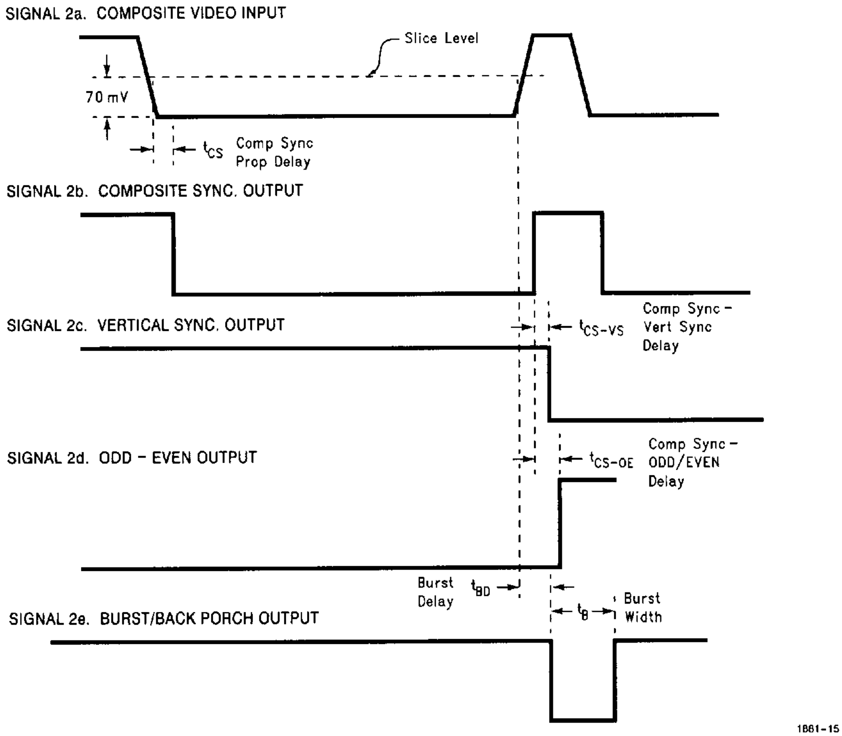

Figure 2. Standard Vertical Timing

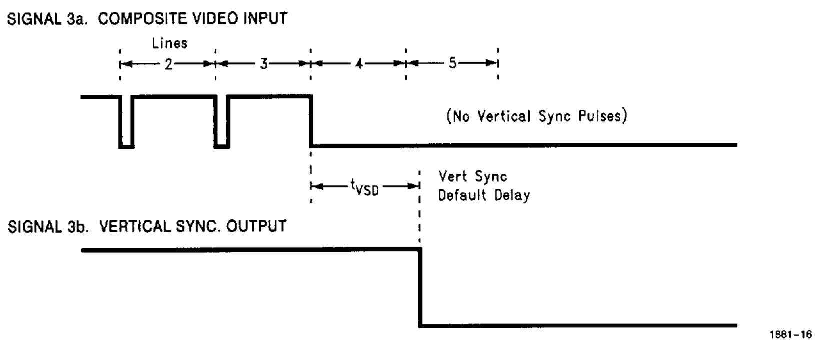

Figure 3. Non-Standard Vertical Timing

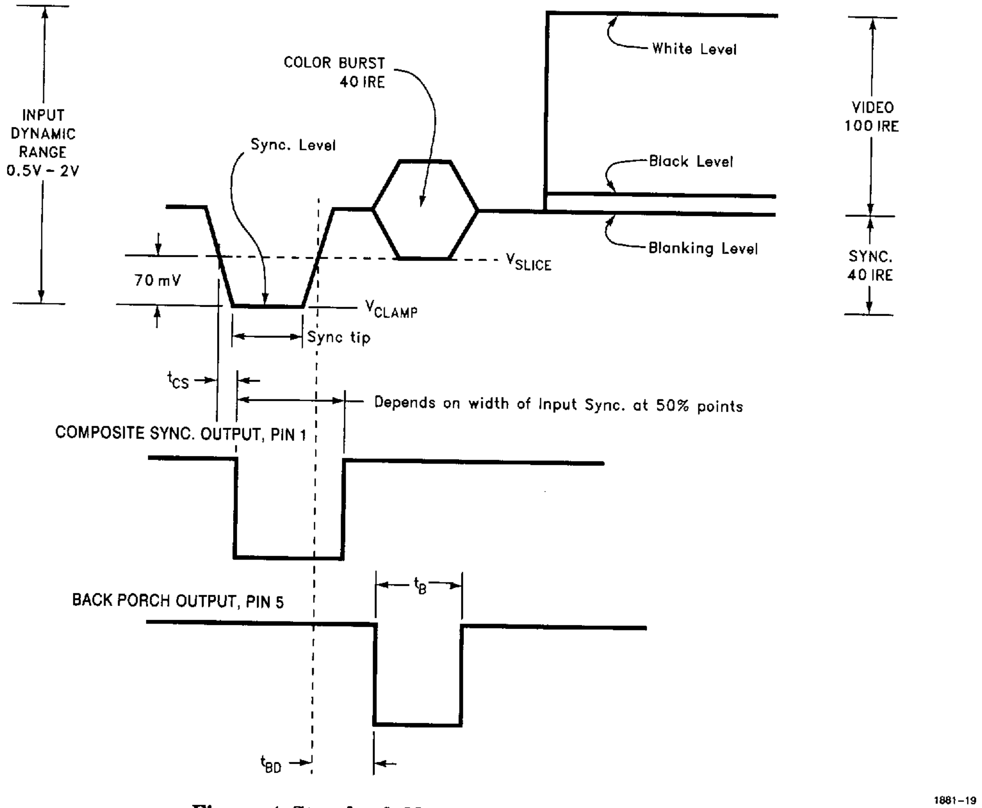

Figure 4. Standard (NTSC Input) H. Sync Detail

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to **Video In** pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1 mA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period − sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time T = 58.9 μs. The droop voltage will then be V = 5.9 mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by T = CV/I, where I = clamp charge current = 1 mA. Here T = 590 ns, about 12% of the sync pulse width of 4.7 μs. It is important to choose C1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Fixed Gain Buffer

The clamped video signal then passes to the fixed gain buffer which places the sync slice level at the equivalent level of 70 mV above sync tip. The output of this buffer is presented to the comparator, along with the slice reference. The comparator output is level shifted and buffered to TTL levels, and sent out as **Composite Sync** to pin 1.

Burst

A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an R_{SET} of 681 kΩ.

Vertical Sync

A low-going **Vertical Sync** pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1881C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for R_{SET} = 681 kΩ.

Odd/Even

Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1881C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

R_{SET}

An external R_{SET} resistor, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

Applications Information — Contd.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500 pF, which gives a single pole roll-off frequency of about 500 kHz. This sufficiently attenuates the 3.58 MHz (NTSC) or 4.43 MHz (PAL) color burst signal, yet passes the approximately 15 kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from the composite input to the outputs.

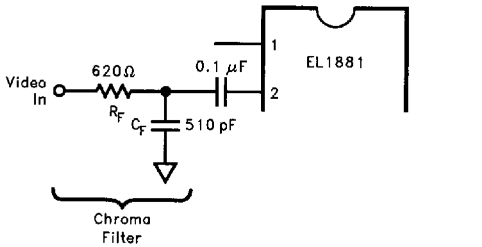

Figure 5

Simplified Block Diagram

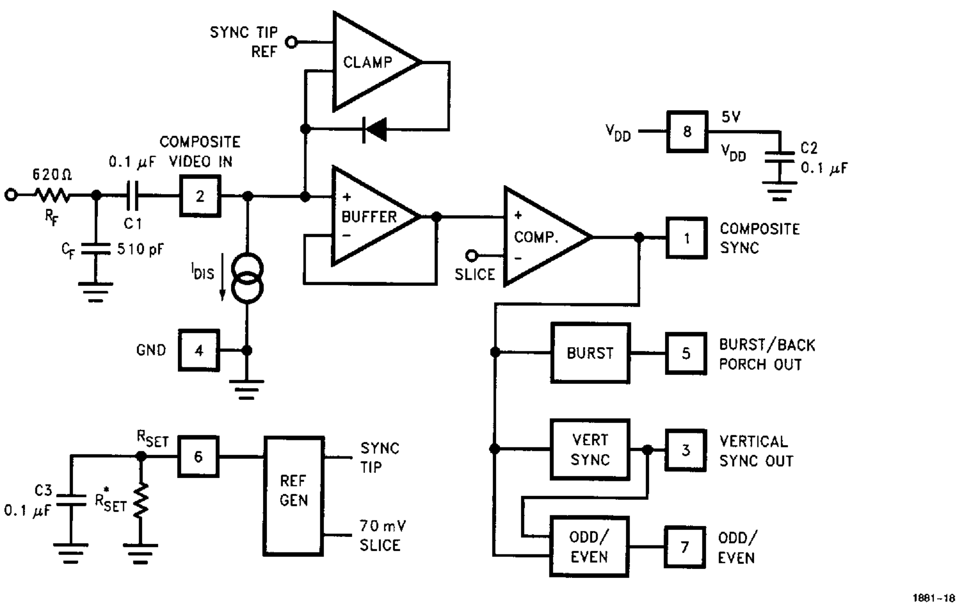

Figure 6

* Note: R_{SET} must be a 1% resistor.