élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4581C
Sync Separator, 50% Slice, S-H, Filter

Features

- NTSC, PAL and SECAM sync separation
- Single supply, + 5V
- Precision 50% slicing, internal caps
- Built-in color burst filter
- Decodes non-standard verticals
- Pin compatible with LM1881
- Low power
- Typically 1.5 mA supply current
- Resistor programmable scan rate
- Few external components
- Available in 8-pin DIP and SO-8 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4581CN	−40°C to +85°C	8-Pin DIP	MDP0031
EL4581CS	−40°C to +85°C	8-Lead SO	MDP0027

Demo Board

A dedicated demo board is not available. However, this device can be placed on the EL4584/5 Demo Board.

General Description

The EL4581C extracts timing information from standard negative going video sync found in NTSC, PAL, and SECAM broadcast systems. It can also be used in non standard formats and with computer graphics systems at higher scan rates, by adjusting a single external resistor. When the input does not have correct serration pulses in the vertical interval, a default vertical output is produced.

Outputs are composite sync, vertical sync, burst/back porch output, and odd/even output. The later operates only in interlaced scan formats.

The EL4581C provides a reliable method of determining correct sync slide level by setting it to the mid-point between sync tip and blanking level at the back porch. This 50% level is determined by two internal self timing sample and hold circuits that track sync tip and back porch levels. This also provides a degree of hum and noise rejection to the input signal, and compensates for varying input levels of 0.5 p-p to 2.0 Vp-p.

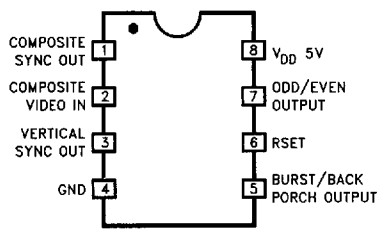
A built in linear phase, third order, low pass filter attenuates the chroma signal in color systems to prevent incorrectly set color burst from disturbing the 50% sync slide.

This device may be used to replace the industry standard LM1881, offering improved performance and reduced power consumption.

The EL4581C video sync separator is manufactured using Elantec's high performance analog CMOS process.

Connection Diagram

EL4581C SO, P-DIP Packages



Top View

Manufactured under U.S. Patent No. 5,528,303

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Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} + 0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	−40°C to +85°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise state V_{DD} = 5V, T_A = 25°C, R_{set} = 680 kΩ.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C	0.75	1.7	3	I	mA
Clamp Voltage	Pin 2, Unloaded	25°C	1.3	1.5	1.9	I	V
Discharge Current	Pin 2 = 2V	25°C	6	10	20	I	µA
Clamp Charge Current	Pin 2, V_{IN} = 1V	25°C	2	3		I	mA
Ref Voltage	Pin 6, V_{DD} = 5V (Note 2)	25°C	1.5	1.8	2.1	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C			800	I	mV
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	25°C	4 2.4			IV I	V

Note 1: No video signal, outputs unloaded.
Note 2: Tested for V_{DD} 5V ±5% which guarantees timing of output pulses over this range.

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Dynamic Characteristics

V_{DD} = 5V, I_V pk-pk video, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA. Signal voltages are peak to peak.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Vertical Sync Width, t_{VS}	(Note 3)	25°C	190	230	300	I	µs
Burst/Back Porch Width, t_B	(Note 3)	25°C	2.5	3.5	4.5	I	µs
Vertical Sync Default Delay t_{VSD}		25°C	40	55	70	I	µs
Filter Attenuation	F_{IN} = 3.4 MHz (Note 4)	25°C		24		V	dB
Composite Sync Prop Delay	V_{IN} − Composite Sync (Note 3)	25°C		260	400	I	ns
Input Dynamic Range	p-p NTSC Signal (Note 5)	25°C	0.5		2	I	V
Slice Level	Input Voltage = $1V_{P-P}$ (Note 6)	25°C Full	40% 40%	50% 50%	60% 60%	I IV	

Note 3: C/S, Vertical and Burst outputs are all active low − V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 4: Attenuation is a function of Rset (PIN6).
Note 5: Typical min. is 0.3 V_{P-P}.
Note 6: Refers to threshold level of sync. tip to back porch amplitude.

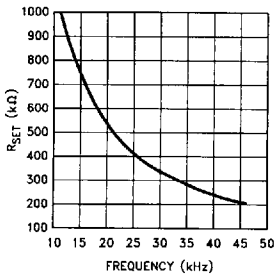
Pin Descriptions

Pin No.	Pin Name	Function
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video in	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	GND	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. 681k, 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. Low during odd fields, high during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD} 5V	Positive supply. (5V)

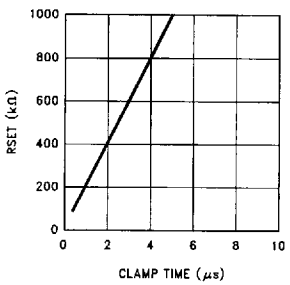
Note: R_{SET} must be a 1% resistor.

Typical Performance Characteristics

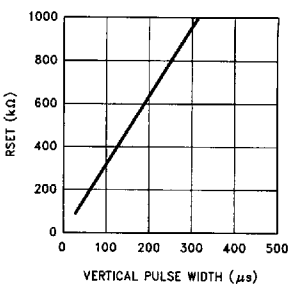
RSET vs Horizontal Frequency



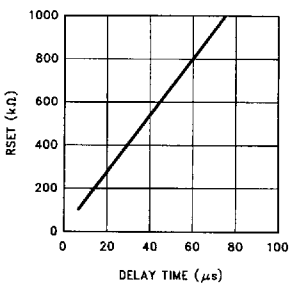
Back Porch Clamp On Time vs RSET



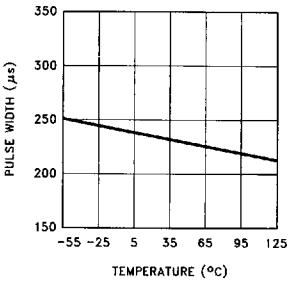
Vertical Pulse Width vs RSET



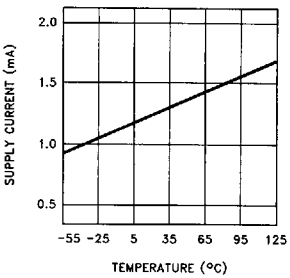
Vertical Default Delay Time vs RSET



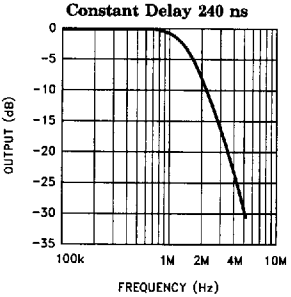
Vertical Pulse Width vs Temperature



Supply Current vs Temperature



Input Signal = 300 mV_{P-P} EL4581 Filter Characteristic Constant Delay 240 ns



4581-2

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Timing Diagrams

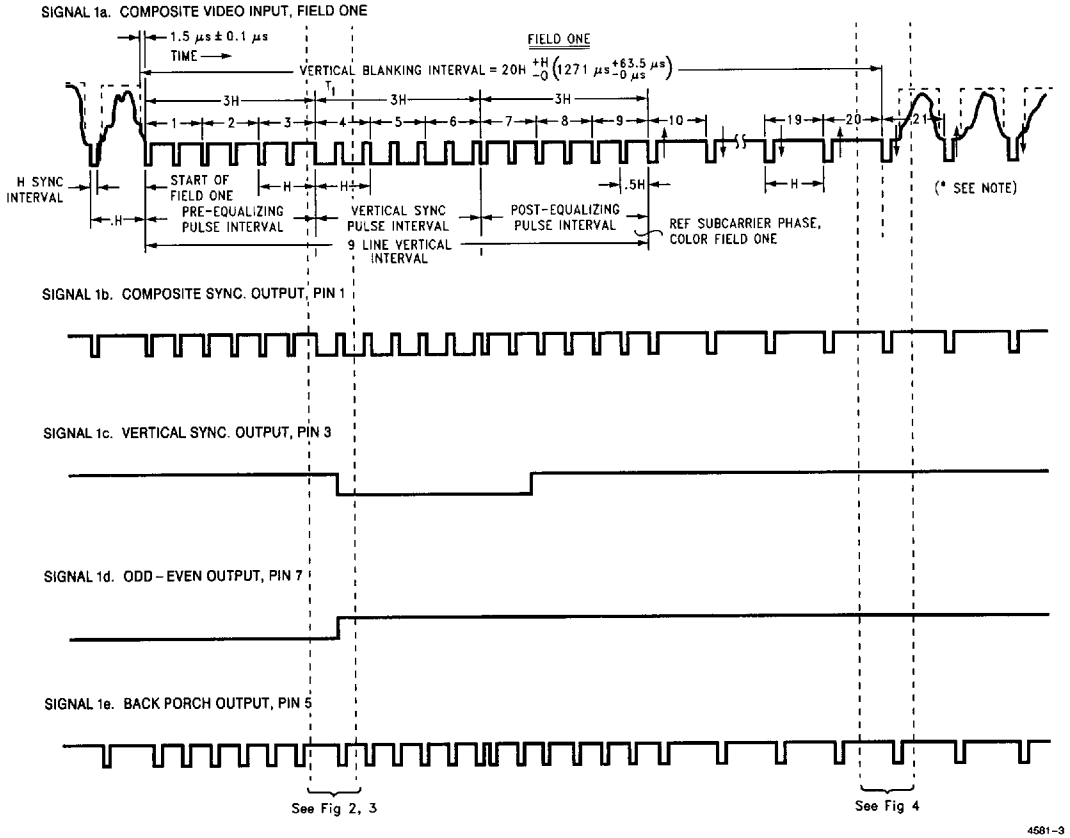

Figure 1

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

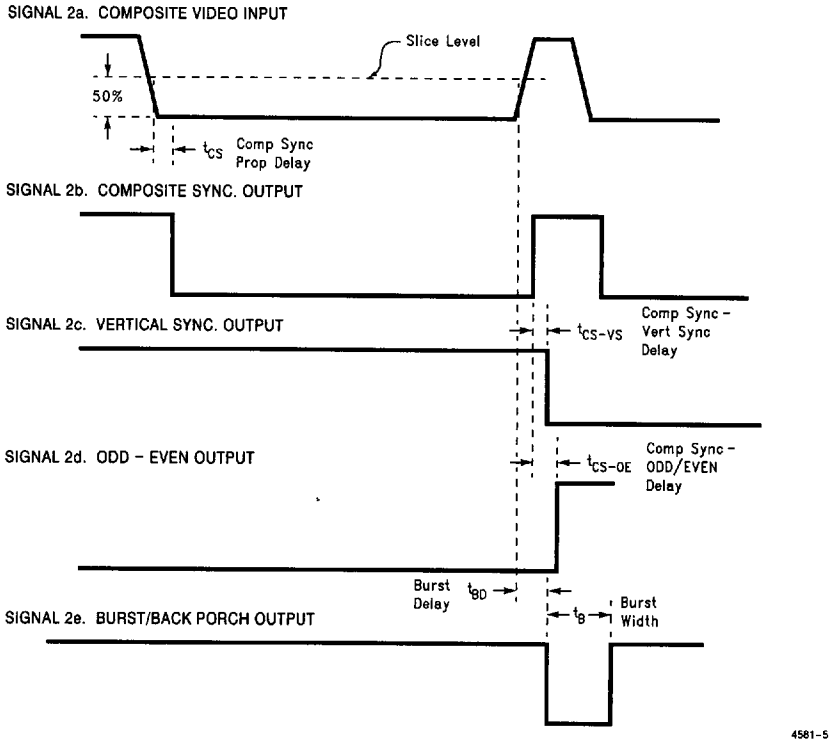

Figure 2

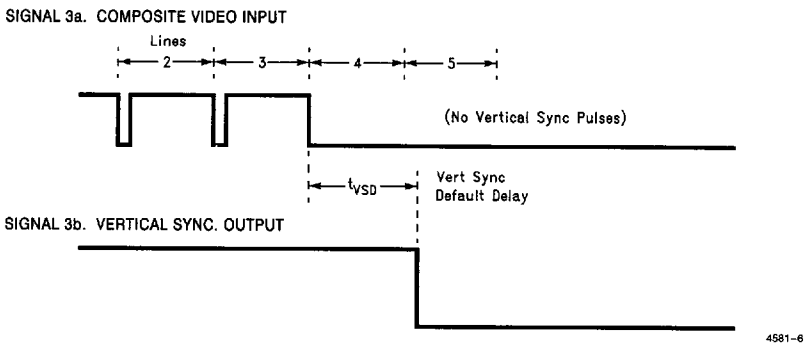

Figure 3

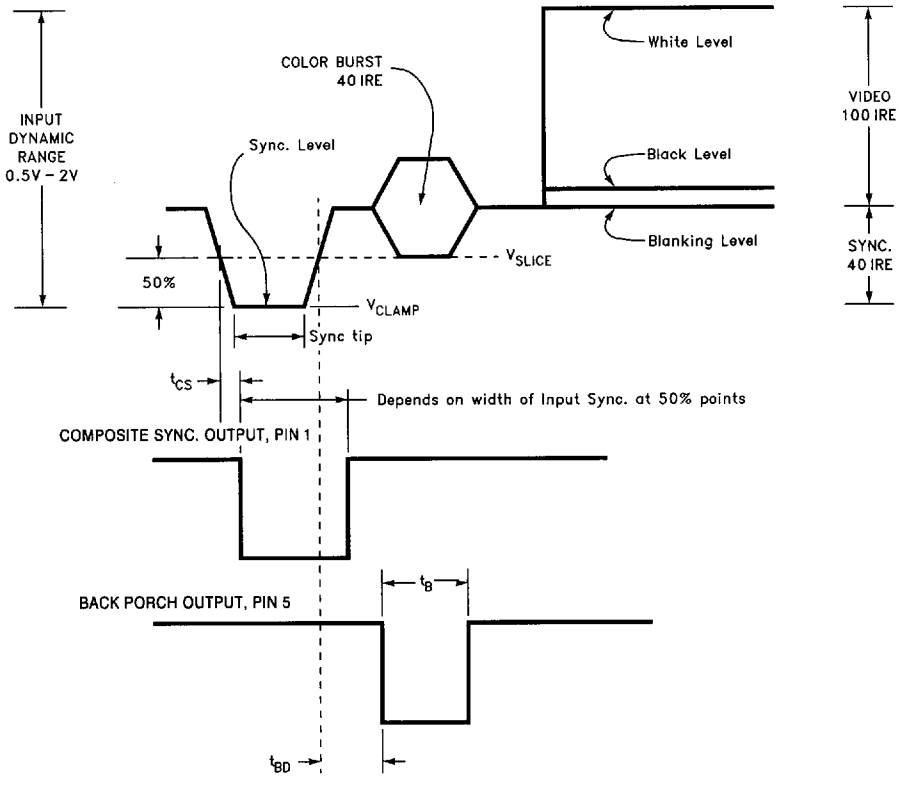

Figure 4. Standard (NTSC Input) H. Sync Detail

Description of Operation

A simplified block schematic is shown in Figure 2. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 2 via the capacitor C_1, nominally 0.1 μF. The clamp circuit A1 will prevent the input signal on pin 2 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From $I \bullet t = C \bullet V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. Note that the filter cut-off frequency is a function of RSET through I_{OT} and is proportional to I_{OT}.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 6 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divider R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S ouput buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer

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Description of Operation — Contd.

vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the time-out period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absense of a serration pulse, an internal timer will default the start of vertical.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RSET.

The odd/even circuit (O/E) comprises of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 7 is high during the odd field.

Loss of video signal can be detected by monitoring the C/S output. The 50% level of the previous video signal will remain held on the S/H capacitors after the input video signal has gone and the input on pin 2 has defaulted to the clamp voltage. Consequently the C/S output will remain low longer than the normal vertical pulse period. An external timing circuit could be used to detect this condition.

Block Diagram

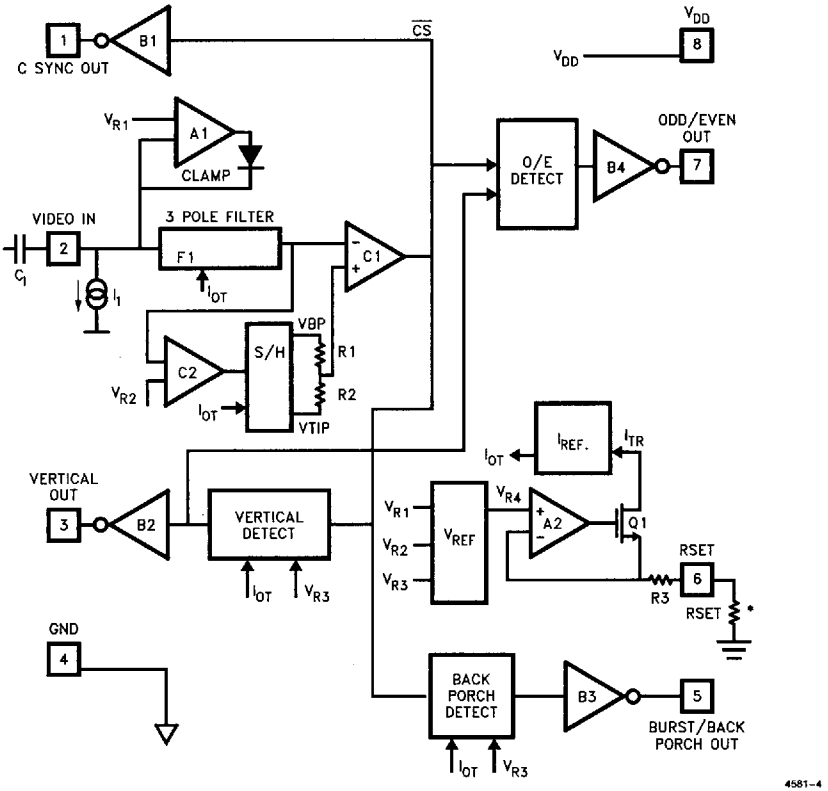


Figure 5

*Note: RSET must be a 1% resistor.

Soldering Packages to PC Boards

DIP Packages

Wave soldering is recommended for DIP packages. Solder plated boards are recommended. Rosin mildly activated (RMA) flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Hand soldering, Elantec's DIP packages will survive a peak temperature of 300°C (at leads) for a maximum period of 10 seconds.

Surface Mount Packages

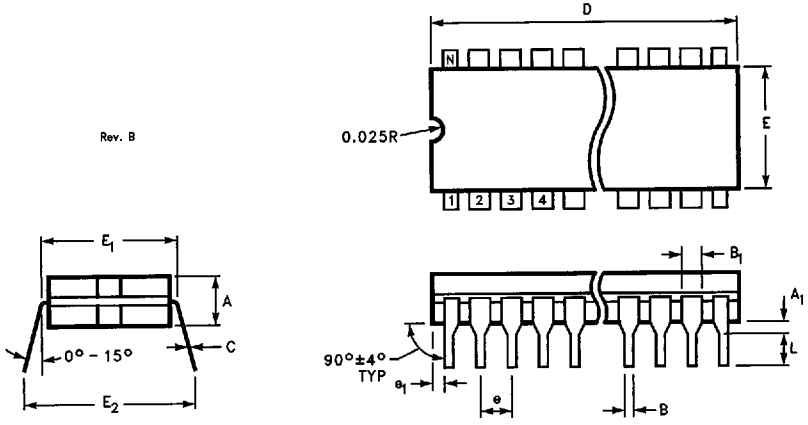
Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages to PC boards. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for a maximum of two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake boards at 65°C–90°C for 15 minutes. Preheat boards to within 60°C–70°C of the solder temperature. To reflow solder paste with vapor phase method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 215°C. For the IR reflow method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 220°C. The temperature/time ramp-up during vapor phase or IR reflow shall be no greater than 2°C/sec.

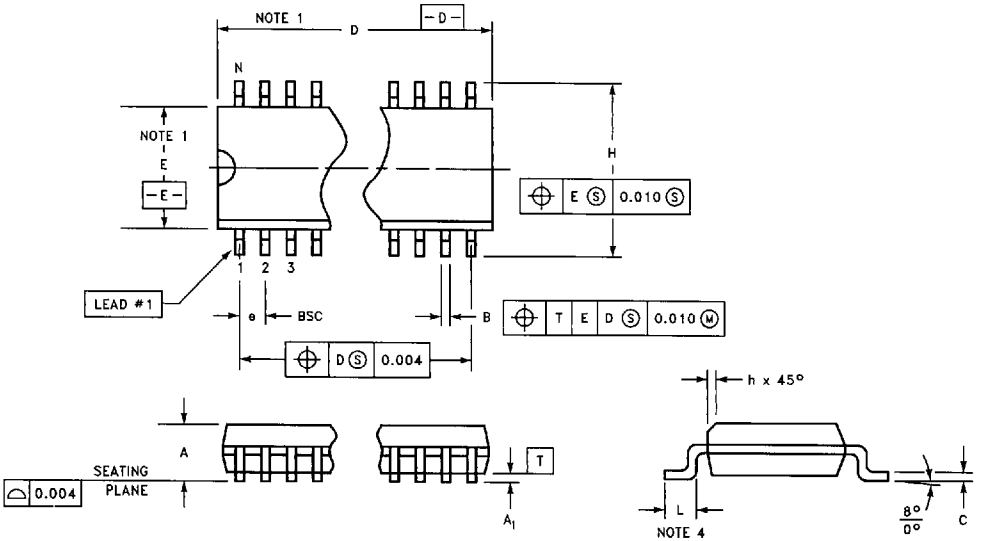
Hand soldering, Elantec's surface mount packages will survive a peak temperature of 260°C (at leads) for a maximum period of 10 seconds.

Package Outlines



MDP0016 Rev. B
CerDIP Package
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.160	0.140	0.160	0.140	0.160	0.140	0.160
A_1	0.115	0.055	0.020	0.050	0.015	0.060	0.020	0.050
B	0.016	0.023	0.016	0.021	0.014	0.026	0.016	0.021
B_1	0.050	0.065	0.050	0.060	0.038	0.068	0.050	0.060
C	0.008	0.012	0.008	0.012	0.008	0.018	0.008	0.012
D	0.375	0.395	0.760	0.785	0.940	0.960	1040.925	1.060
E	0.245	0.265	0.220	0.291	0.220	0.310	0.2780	0.298
E_1	0.300	0.320	0.300	0.320	0.290	0.320	0.300	0.320
E_2	0.340	0.390	0.340	0.390	0.360	0.410	0.340	0.390
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e_1	0.020	0.055	0.078	0.098	0.068	0.098	0.078	0.098
L	0.125	0.150	0.125	0.150	0.125	0.150	0.130	0.150
N	8-Lead		14-Lead		18-Lead		20-Lead	



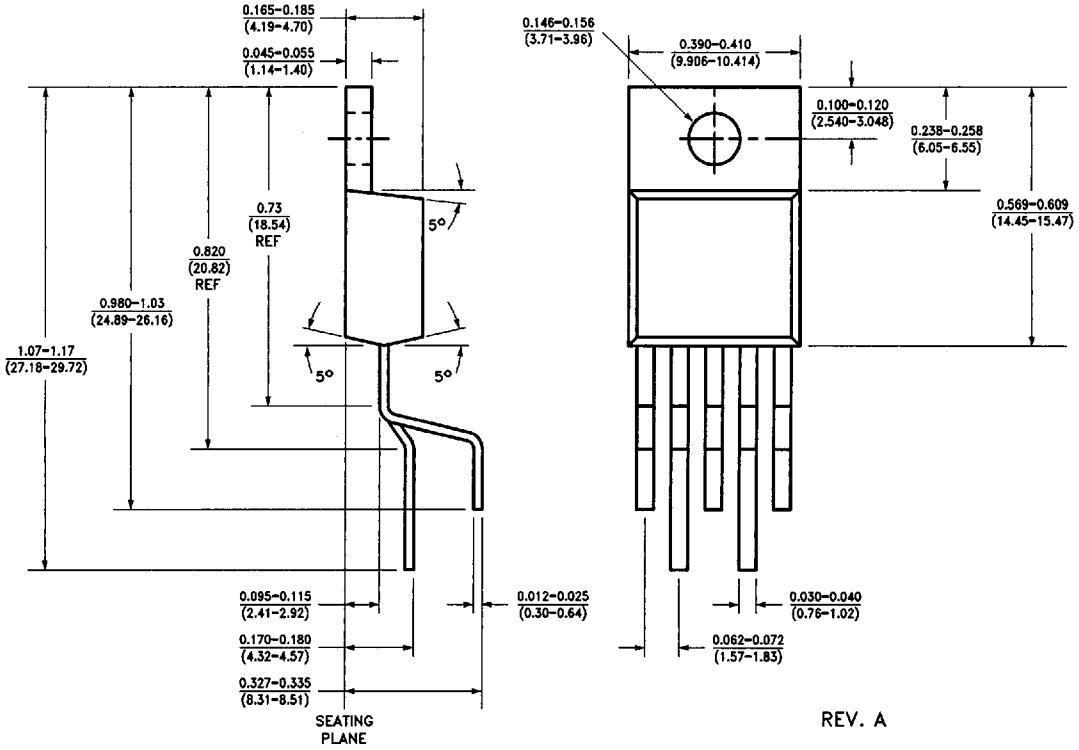
REV. C

Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: SO-8, SO-14, S0-16 packages are narrow body (0.150").
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.
Note 6: SOL-20T (thermal package) has 4 fused leads on each side of package.
Note 7: SOL-28T contains a thermal metal slug.

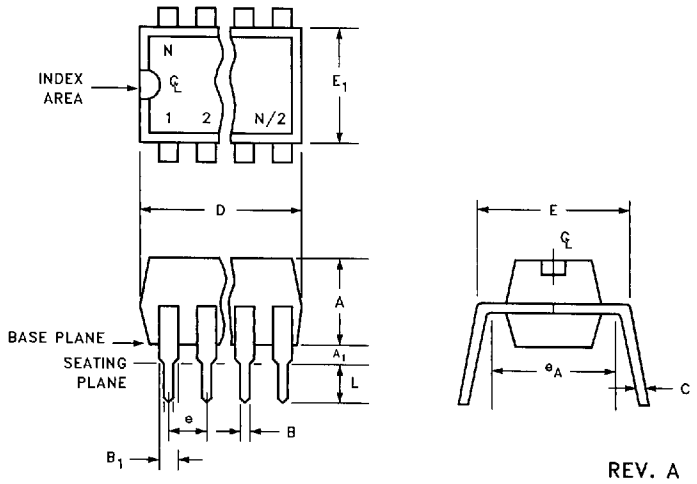
MDP0027 Rev. C
Package Outline—SOIC
Lead Finish—Solder Plate

Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010	0.008	0.010	0.009	0.012
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024

Package Outlines



MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate



MDP0031 Rev. A
Plastic Package
Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.745	0.755	0.745	0.755	0.875	0.905	0.925	1.045
E	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135
N	8		14		16		18		20	

Note: Package outline exclusive of any mold flashes. Mold flash protrusion shall not exceed 0.006" on any side.