March 1992
Edition 1.0A

FUJITSU

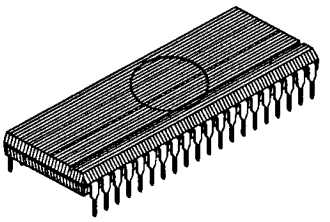
DATA SHEET

MB834200B
CMOS 4M-Bit Mask Read Only Memory

The Fujitsu MB834200B is a CMOS Si-gate mask-programmable static read only memory organized as 262,144 words by 16 bits or 524,288 words by 8 bits. It has TTL-compatible I/O 3-state output level with full-static operation (i.e., no clock signal needed) and a single +5 V power supply. The memory organization is user-configurable between 16 bits and 8 bits. This means that a system using an 8-bit and a 16-bit CPU can both use common data on the same chip

MB34200B is optimized to use in applications such as character generation and program storage, applications that require large memory capacity, high-speed, and minimal power.

- Organized: 524,288 words x 8 bits (512K x 8), or 262,144 words x 16 bits (256K x 16)
- Access time: 150 ns max.
- Completely static operation: No clocks required
- TTL compatible Input/Output
- Three-state output
- Single +5 V power supply
- Power dissipation: 275 mW max. (Active)
  5.5 MW max. (Standby, TTL input level)
  5.5 µW max. (Standby, CMOS input level)
- Package and ordering information:
  – 40-pin plastic DIP, order as MB834300BP
  – 44-pin plastic QFP, order as MB834300BPFQ
  – 48-pin plastic thin SOP (TSOP):
  Normal bend leads, order as MB834200BPFTN
  Reverse bend leads, order as MB834200BPFTR
  – 64-pin plastic QFP, order as MB834200BPFQ

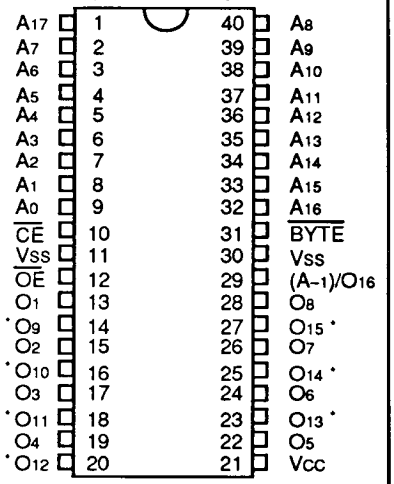


Plastic DIP Package
(DIP–40P–M01)

QFP (FPT-44P-M04) pages 6 and 7
TSOP (FPT-48P-M07) pages 8 and 9
TSOP (FPT-48P-M08) pages 10 and 11
QFP (FPT-64P-M01) pages 12 and 13

PIN ASSIGNMENT

(TOP VIEW)



*This pin is High-Z when the device is organized as 8-bits.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0[1]	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5[1]	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5[1]	V
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Eange	T_{STG}	–45 to +125	°C

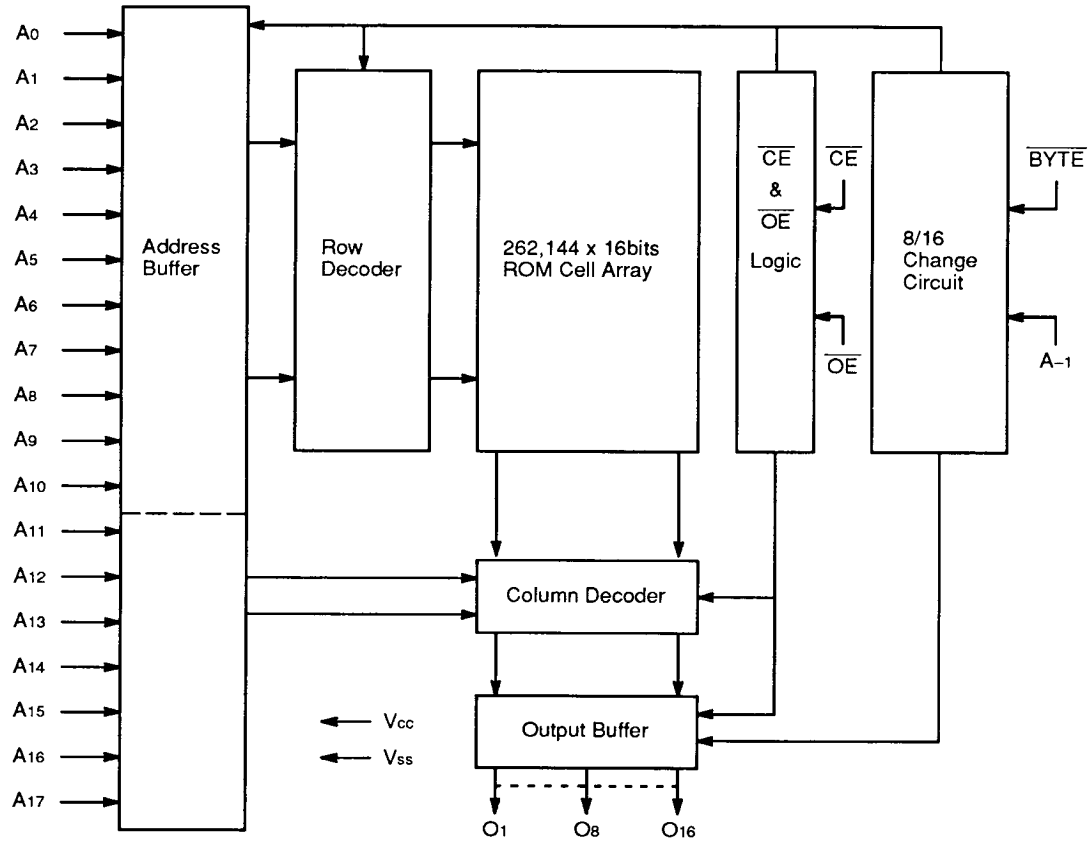
Note: [1]Referenced to GND

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB834200B BLOCK DIAGRAM



OUTPUT SELECTION MODE A-1 is LSB.

$\overline{BYTE}$	O1 to O8	O9 to O15	(A-1)/O16
H	O1 to O8	O9 to O15	O16
L	O1 to O8	High–Z	A–1 ("L" INPUT)
L	O9 to O16	High–Z	A–1 ("H" INPUT)

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Dissipation Mode
H	X	Not Selected	High–Z	Standby
L	H	Not Selected	High–Z	Active
L	L	Selected	DOUT	Active

CAPACITANCE (TA=25° C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	COUT			15	pF
Input Capacitance (VIN=0V)	CIN			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

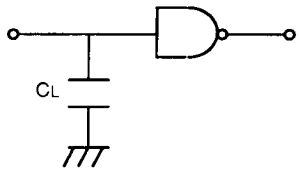
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=V_{IL}, Minimum Cycle	I_{CC}			50	mA
Standby Supply Current	$\overline{CE}$=V_{IH}	I_{SB1}			1	mA
	$\overline{CE}$=V_{CC}=V_{IH}, V_{IN}=GND or V_{CC}	I_{SB2}			10	µA
Input Leakage Current	V_{IN}=0 to V_{CC}	I_{LI}	–10		10	µA
Output Leakage Current	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}	$I_{LI/O}$	–10		10	µA
Input Low Voltage		V_{IL}	–0.3		0.8	V
Input High Voltage		V_{IH}	2.2		V_{CC}+0.3	V
Output High Voltage	I_{OH}=–400µA	V_{OH}	2.4			V
Output Low Voltage	I_{OL}=2.1mA	V_{OL}			0.4	V

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : t_T=5ns
- Timing Reference Levels : Input: . V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
- Output Load : 1 TTL Gate and 100pF



AC CHARACTERISTICS

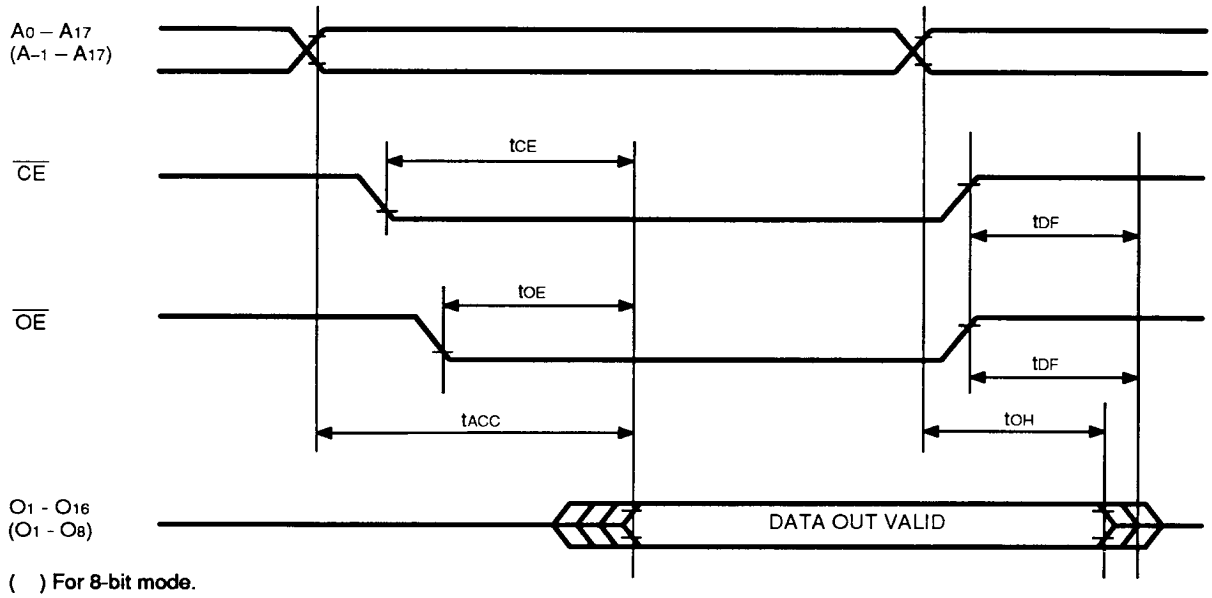
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{ACC}		150	ns
Chip Enable Access Time	$\overline{OE}$=V_{IL}	t_{CE}		150	ns
Output Enable Access Time	Note 1	t_{OE}		70	ns
Output Disable Time	Note 2	t_{DF}		60	ns
Output Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	t_{OH}	0		ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.

TIMING DIAGRAM



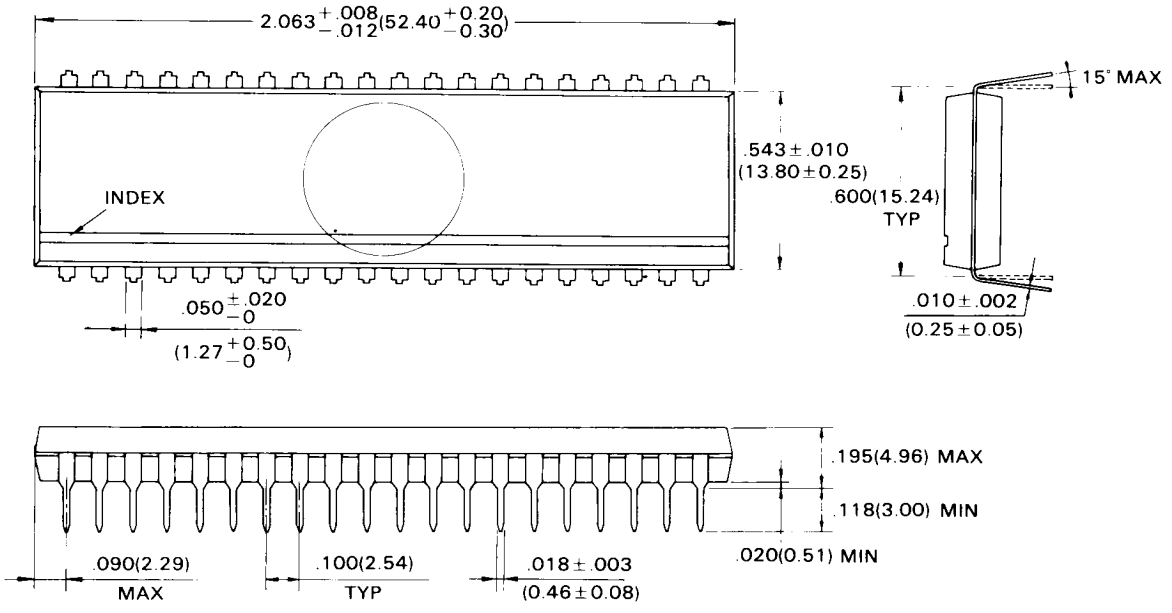
( ) For 8-bit mode.

PACKAGE DIMENSIONS

(Suffix: P)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE

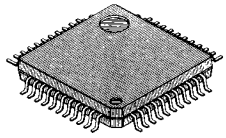
(Case No. : DIP-40P-M01)



Dimensions in
inches (millimeters)

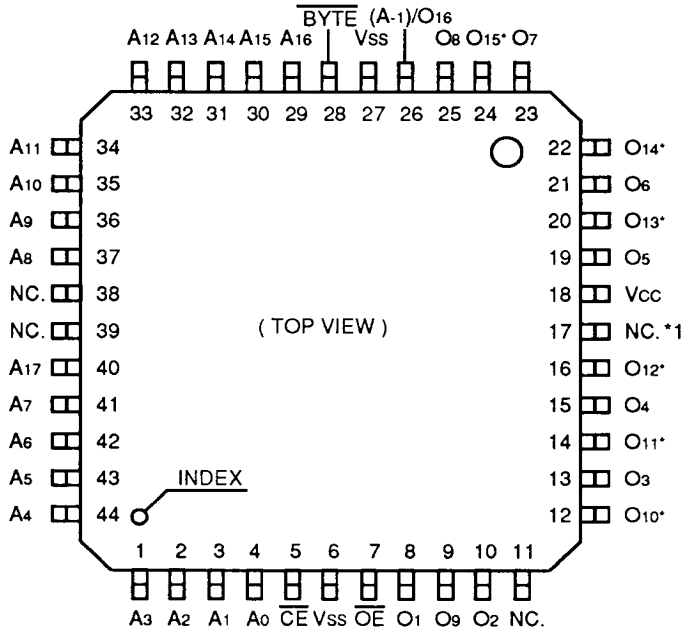
PACKAGE DIMENSIONS (Continued)

(Suffix: PFQ)



PLASTIC PACKAGE
FPT-44P-M04

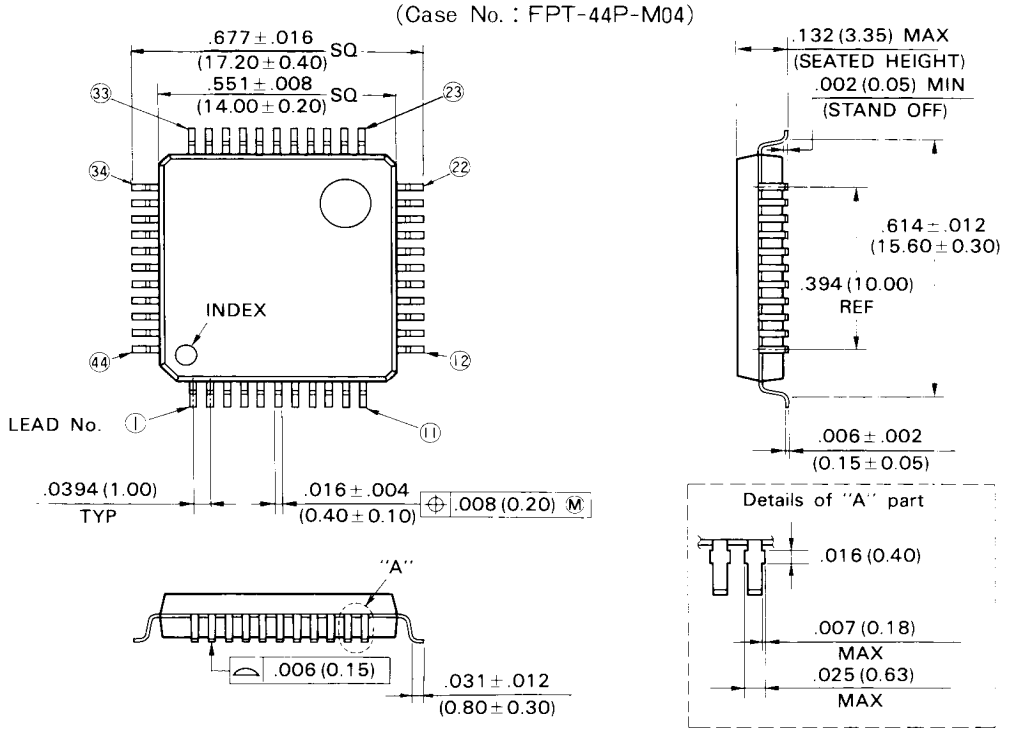
PIN ASSIGNMENT



This pin(*) is High–Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to Vss.

44-LEAD PLASTIC FLAT PACKAGE

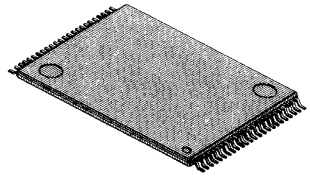
(Case No. : FPT-44P-M04)



Dimensions in
inches (millimeters)

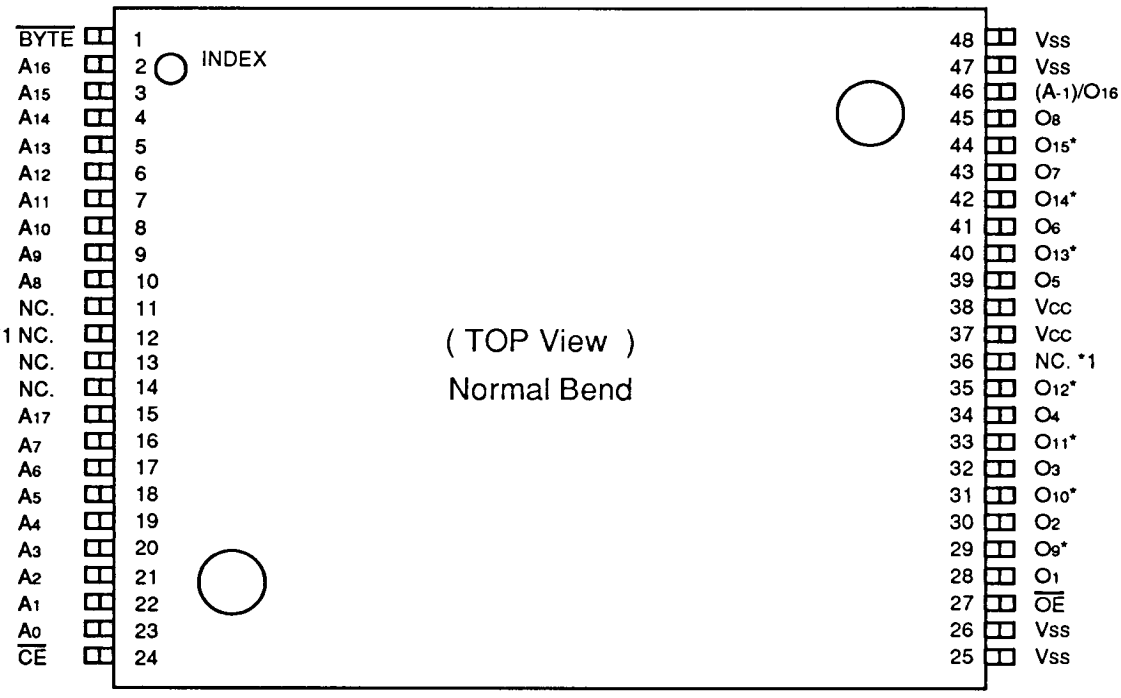
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



PLASTIC PACKAGE
FPT-48P-M07

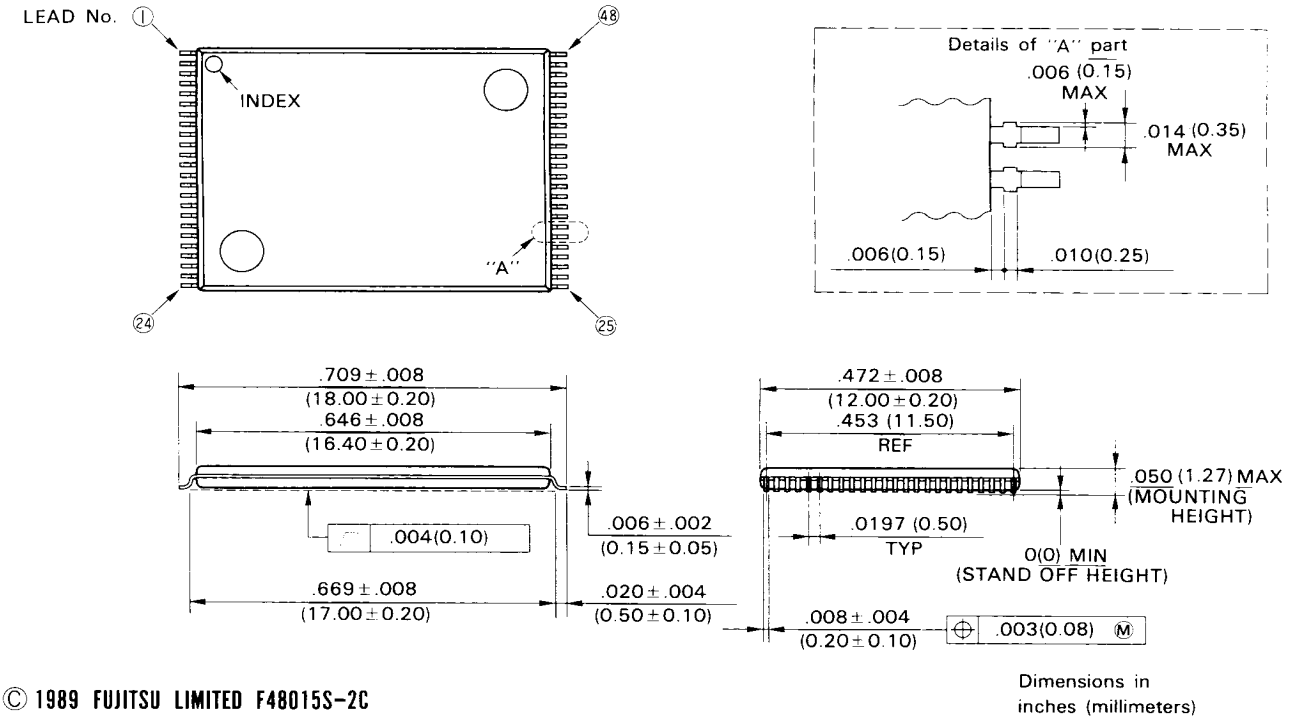
PIN ASSIGNMENT



This pin(*) is High–Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to Vss.

48-LEAD PLASTIC FLAT PACKAGE

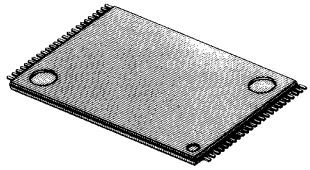
(Case No. : FPT-48P-M07)



Dimensions in inches (millimeters)

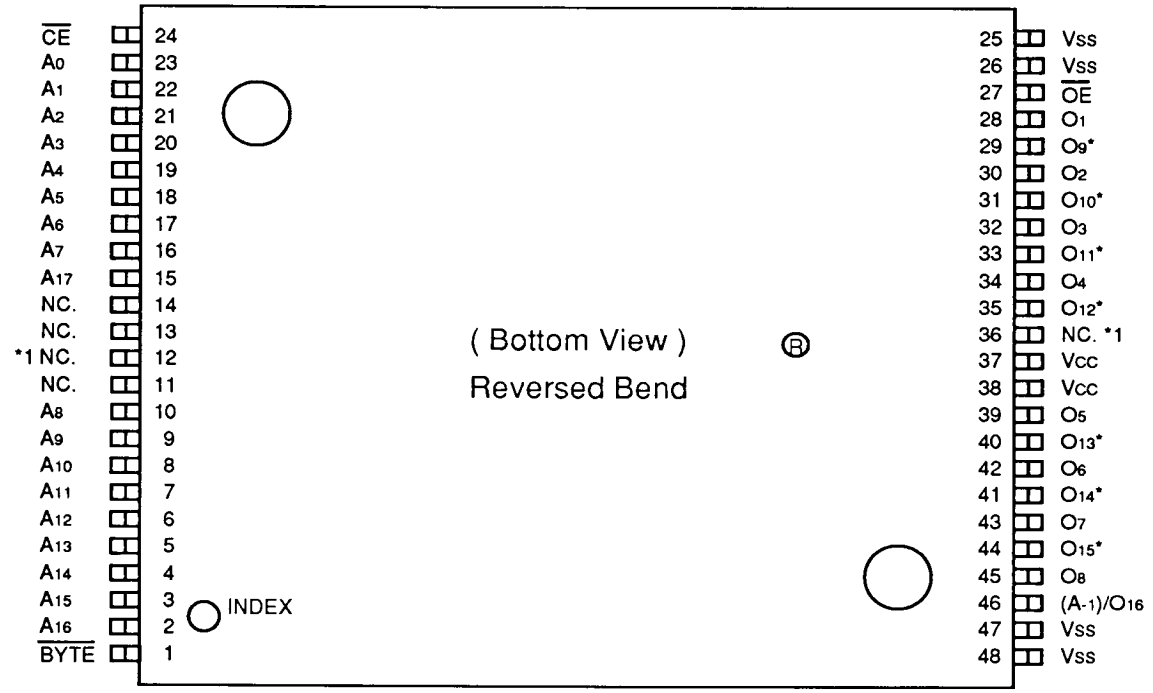
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



PLASTIC PACKAGE
FPT-48P-M08

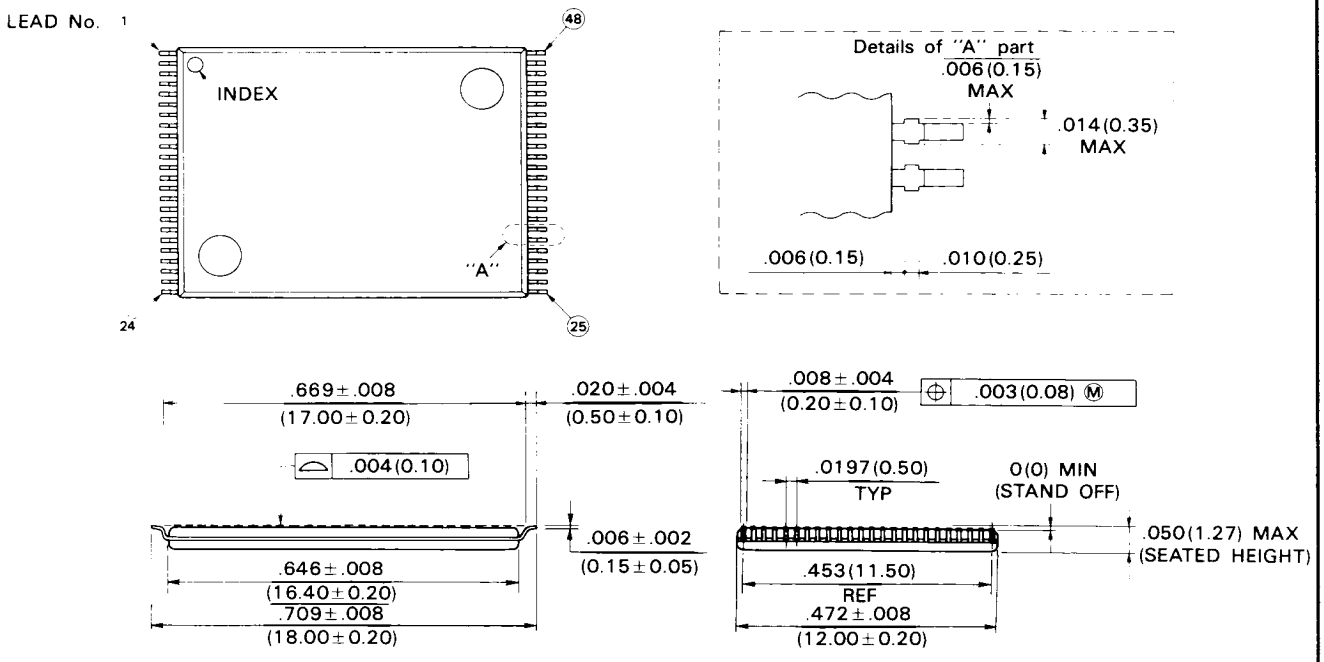
PIN ASSIGNMENT



This pin(*) is High–Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to Vss.

48-LEAD PLASTIC FLAT PACKAGE

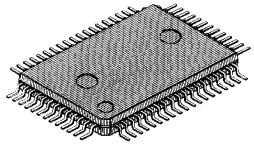
(Case No. : FPT-48P-M08)



Dimensions in inches (millimeters)

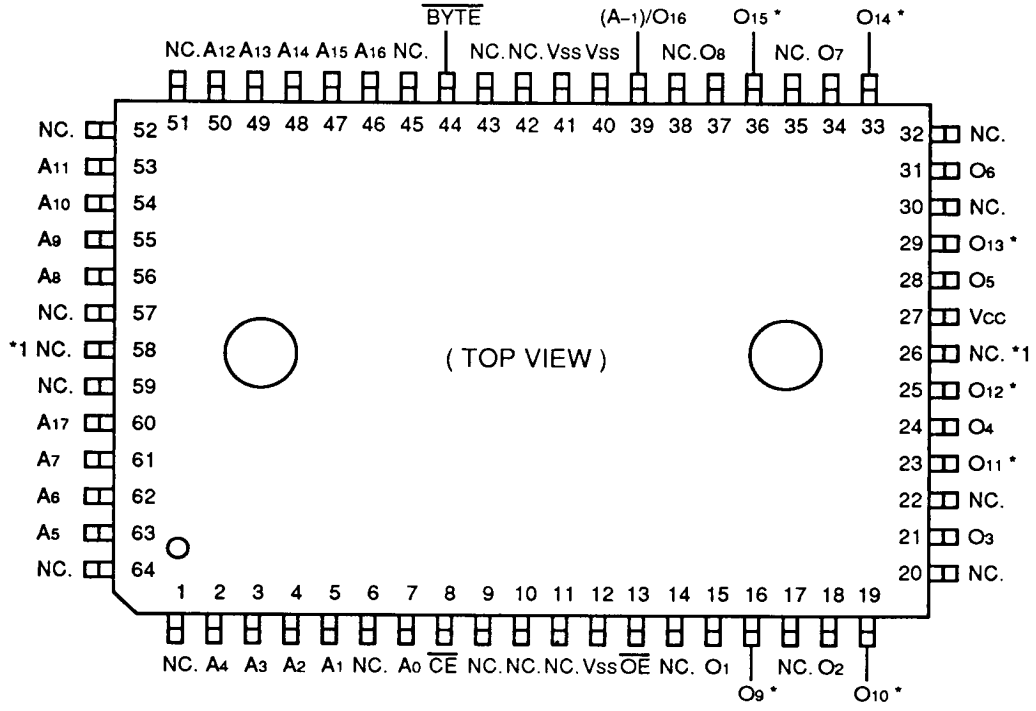
PACKAGE DIMENSIONS (Continued)

(Suffix: PFQ)



PLASTIC PACKAGE
FPT-64P-M01

PIN ASSIGNMENT



This pin(*) is High–Z, the device is used 8 bits.
*1: If the voltage is applied externally, it should be connected to Vss.

PACKAGE DIMENSIONS (Continued)