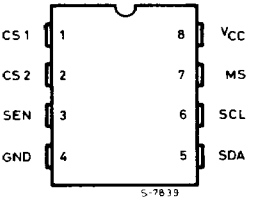
1024 BIT SERIAL S-BUS/I²C BUS NMOS EEPROM

- 10 YEAR DATA RETENTION
- SINGLE +5V POWER SUPPLY
- AUTOMATIC POWER DOWN
- INTERNAL HIGH VOLTAGE AND SHAPING GENERATOR
- SELF TIMED E/W OPERATION
- AUTOMATIC ERASE BEFORE WRITE
- 3-WIRES S-BUS (I²C BUS COMPATIBLE)
- 2 CHIP SELECT FOR SIMPLE MEMORY EXTENSION
- SELF INCREMENTING ADDRESS REGISTER
- MULTI-MODE ADDRESSING (WHEN MS = V_{IH} ALLOWING:
  - PARTITIONING OF THE 1024 BITS INTO:
    - 128 × 8bit
    - 64 × 16bit
    - 32 × 32bit
  - OPCODE-LIKE ADDRESSES FOR:
    - halting of a modify operation
    - reading of the device "busy" status
    - "block erase" operation
    - reloading of the address register with the pre-increment value

B
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

The M8571 is a 1024-bit Electrically Erasable Programmable Read Only Memory (EEPROM). It allows partitioning of the 1024-bit into: 128 × 8-bit (bytes); 64 × 16-bit (words); 32 × 32-bit (pages).
The M8571 is manufactured with SGS-THOMSON's reliable floating gate technology. Addresses and data are transferred serially via a three-line bidirectional bus (S-BUS). When the MS pin is at V_{IL} the device works like the PCD 8571 CMOS RAM. The built-in address register is incremented automatically after writing or reading of each address partition.
The M8571 is designed and tested for applications requiring up to 10.000 erase/write cycles and data retention in excess than 100 years.
The M8571 is available in 8-pin dual in-line plastic and ceramic packages.

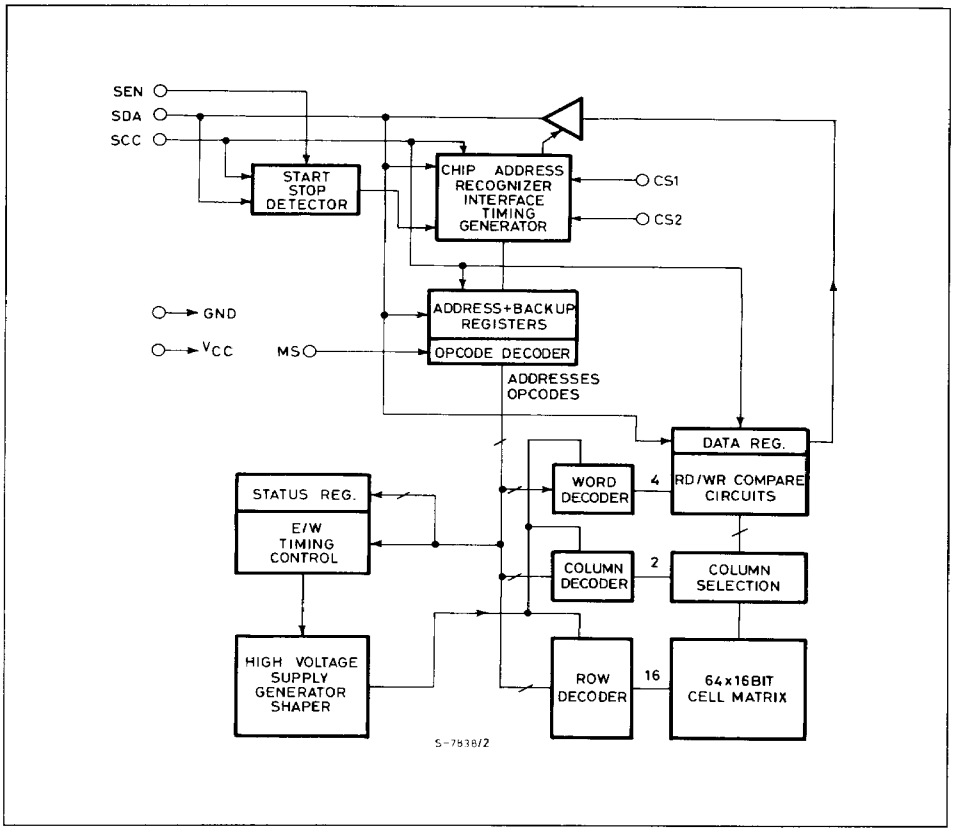
PIN NAMES

CS	CHIP SELECT INPUTS
SEN	START/STOP INPUT
SCL	CLOCK INPUT
SDA	DATA INPUT/OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
MS	MODE SELECT INPUT

PIN DESCRIPTION

- V_{CC}; GND: Power supplies.
- SCL: Clock line for the S-BUS system.
- SEN: Start/Stop line for the S-BUS system.
- SDA: Data line for the S-BUS system (open drain).
- CS1/CS2: Chip Select inputs. In order to select a device the 2 bits (7th and 6th) in the first byte of the interface protocol, must match the CS values.
- MS: Mode Select input to determine the operating mode of the M8571 (this pin can recognize a non standard level, $V_{IN} \geq$ 7.5V, to enable "Block Erase" operations).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
T_{amb}	Ambient temperature under bias /B1 /B6	−10 to + 80 −50 to + 95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (0° to +70°C, for standard Temperature/ −40° to +85°C for extended Temperature, V_{CC} = 5V ± 10% unless otherwise specified)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{CC2}	V_{CC} Current Active			10	20	mA
V_{IL}	Input Low Voltage		−0.1		1.5	V
V_{IH}	Input High Voltage		3.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

AC CHARACTERISTICS (refer to S-BUS Timing Diagram)

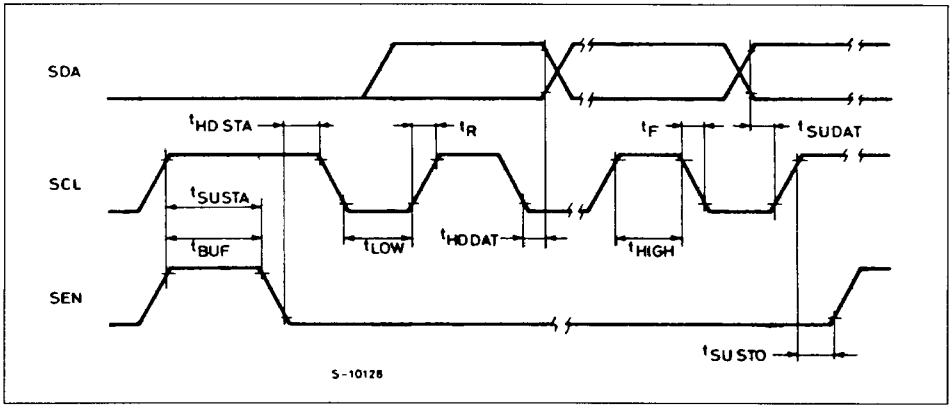
Symbol	Parameter	Test Conditions	Values		Unit
			Min.	Max.	
f_{SCL}	SCL clock frequency		0	125	KHz
T_I	Tolerable spike width on bus			100	ns
t_{AA}	SCL low to SDA data out valid			3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start		4		µs
t_{HDSTA}	Start condition hold time		4		µs
t_{LOW}	Clock low period		4		µs
t_{HIGH}	Clock high period		4		µs
$t_{SU\ STA}$	Start condition set-up time (for a repeated start condition)		4		µs
$t_{HD\ DAT}$	Data in hold time		0		µs
$t_{SU\ DAT}$	Data in set-up time		250		ns
t_R	SDA and SCL rise time			700	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU\ STO}$	Stop condition set-up time		4		µs

ERASE/WRITE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{EW}	Erase/Write cycle time	Note 1		6	10	ms
t_{BE}	Block erase time		5		10	ms

Note 1: The t_{EW} is the same for byte, word, and page configuration

S-BUS TIMING DIAGRAM



S-BUS DESCRIPTION

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²C bus. In fact the S-BUS includes decoding of START/STOP conditions and the arbitration procedure in case of multimaster system configuration. Both different transmission modes are shown in figures 2a and 2b. As it can be seen, the SDA line, in the I²C bus, represents the AND combination of SDA and SEN lines in the S-BUS.
If the SDA and the SEN lines of the S-BUS are short-circuit connected, they appear as the SDA line of I²C bus.
The START/STOP conditions (respectively points 1 and 6) are detected (by the peripherals designed to work with S-BUS) by a transition of the SEN line (1 - - >0/0 - - >1) while the SCL line is at the high level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the START information (point 1) the SEN line returns to the high level and remains unchanged for all the time the transmission is performed.
When the transmission is completed (point 5) the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the STOP information with a low to high transition; while the SCL line is at high level.
On the S-BUS, as on the I²C bus, each byte of eight bits is followed by one acknowledge bit which is a high level put on the SDA line by transmitter.
A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse as shown in Figure 3.

FIG. 1 - S-BUS CONFIGURATION

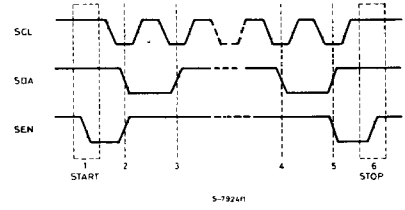


FIG. 2 - I²C BUS CONFIGURATION

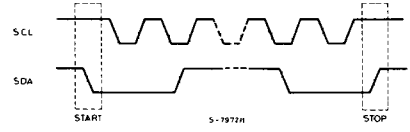
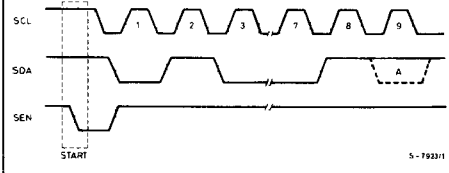


FIG. 3 - ACKNOWLEDGE



S-BUS DESCRIPTION (Continued)

An addressed receiver has to generate an aknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time.
In this case the master transmitter can generate the STOP information, via the SEN line, in order to abort the transfer.

COMPATIBILITY S-BUS/I²C BUS.

Using the S-BUS protocol it's possible to implement "mixed" system including S-BUS/I²C bus peripherals.
In order to have the compability with the I²C bus peripherals, the devices including the S-BUS interface must have their SDA and SEN pins connected together as shown in figures 5a and 5b.
It is also possible to use mixed S-BUS/I²C bus protocols as showed in figure 5c. S-BUS peripherals will only react to S-BUS protocol signals, while I²C bus peripheral will only react to I²C bus signals.

FIG. 4 - SYSTEM WITH S-BUS PERIPHERALS

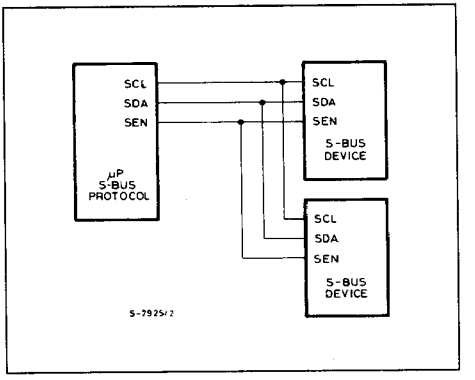
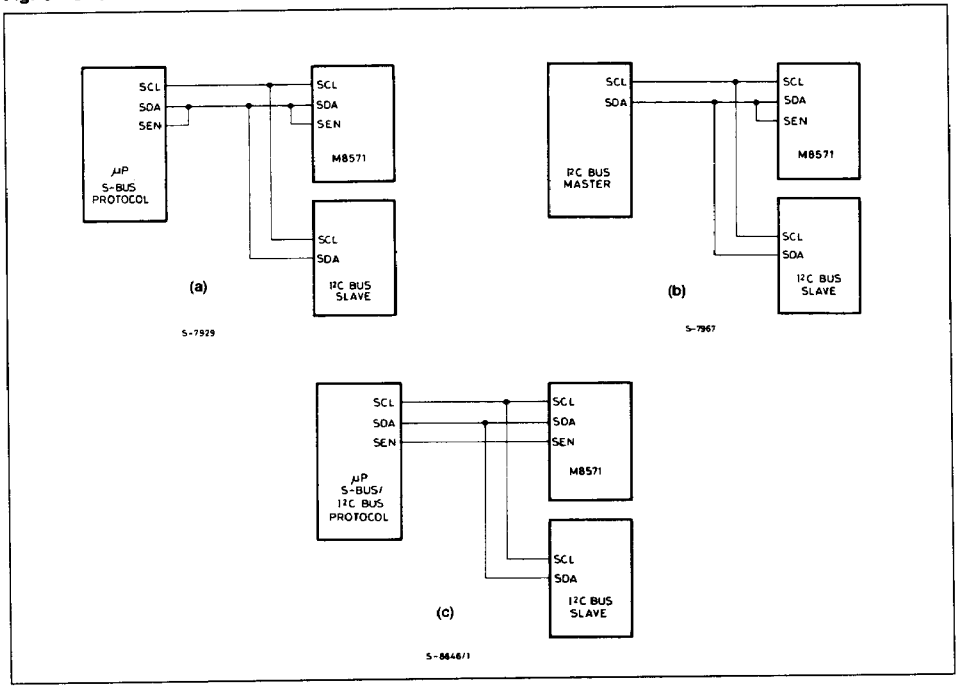


Fig. 5 - SYSTEM WITH "MIXED" S-BUS/I²C BUS PERIPHERAL

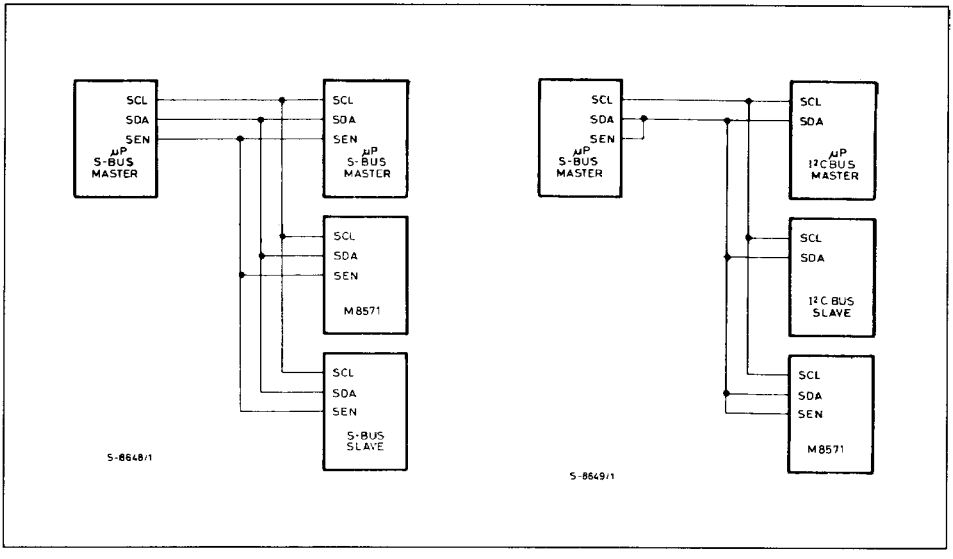


S-BUS DESCRIPTION (Continued)

MULTIMASTER SYSTEM.

The S-BUS allows the implementation of the multimaster configuration (two or more master stations and slave peripherals). In such a system if two or more transmitter, through the SEN line (SEN 1→0 while SCL = 1), require the bus at the same time, the arbitration procedure is performed as in the I²C bus.

FIG. 6 - MULTIMASTER SYSTEM



S-BUS INTERFACE

The serial, 3-wire, interface (SDA, SCL and SEN wires are open drain to allow "wired-and" operation) connects several devices which can be divided into "masters" and "slaves". A master is a device that can manage a data transfer; as such, it drives the Start and Stop (SEN), the clock (SCL) and the data (SDA) lines. The bus is "multimaster" in that more master devices can access it; arbitration procedures are provided in the bus management. Obviously, at least one master must be present on the bus. The M8571 is a hardware slave device. It can only answer the requests of the masters on the bus; therefore SDA is an I/O, while SCL and SEN are inputs. The S-BUS allows two operating speed: high (125KHz) and low (2KHz). The M8571 can work at both high and low speed.

START/STOP ACKNOWLEDGE

The timing specs of the S-BUS protocol require that data on the SDA and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of a data transfer.
A "high to low" transition on the SEN line, with SCL "high", is a start (STA).
A "low to high" transition on the SEN line, with SCL "high", is a stop.
Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmitter device place a "1" on the bus, the acknowledging receiver a "0").

INTERFACE PROTOCOL

The following description deals with 8-bits data transfers, so that it fully fits when the memory is "seen" as 128 x 8 array. Although the basic structure of the protocol remains the same the behaviour of the M8571 in 16 or 32 bit data transfers is somewhat different. The differencies are descibed later on.

The interface protocol comprises:
- A start condition (STA)
- A "chip address" byte, trasmitted by the master, containing two different informations.

  a) the code identifying the device the master wants to address (this information is present in the first seven bits); 4bits indicates the type of the device (i.e. memory, tuning, A/D, etc.; the code for memories is 1010); then there is a bit at low level and 2bits that are the Chip Select configuration that must match the hardware present on the 2 CS pins (this is the case of a device with 2 Chip Select like the M8571, for M8571 CS1 and CS2 must match respectively the 7th and the 6th bit of the byte).
  b) the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence, from now on, is different according to the value of the R/W bit.

1) R/$\overline{W}$ = "0" (WRITE)

   In all the following bytes the master acts as transmitter; the sequence follows with:
   a) a "word address" byte containing the address of the selected memory word and/or opcode (see word address/opcode section).
   b) a "data" byte which will be written at the address given in the previous byte.
   c) further data bytes which, due to the self incrementing address register, will be written in the "next" memory locations. At the end of each byte the M8571 acknowledges.
   d) a stop condition (STO)

After receiving and acknowledging a data byte or a set of data bytes to be written, the M8571 automatically erases the addressed memory locations and rewrites them with the received data. Since the E/W time for an EEPROM is in the order of 10 ms, the next operation can take place only after $t_{E/W}$ (what the master can and must do is described in the E/W TIME SPECS section).
An example of a write sequence is given below:

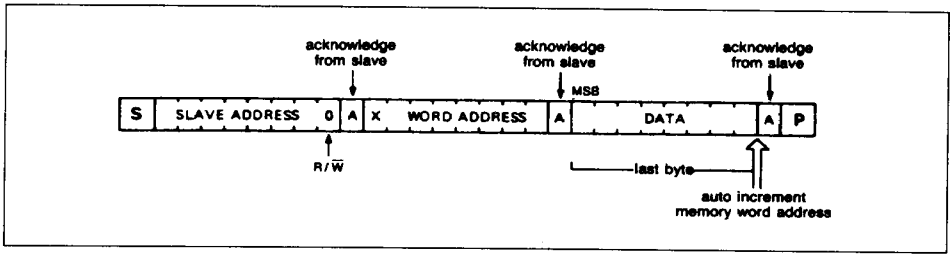
0. STA
1. 10100ss0 A (M8571 acknowledges only if "ss" matches its CS code)
2. xyyyyyyy A
3. zzzzzzzz A (at this moment the M8571 starts writing zzzzzzzz at the address yyyyyyy)

4a. tttttttt H (the new data is not acknowledged while the M8571 is busy)

4b. tttttttt A (now the M8571 writes data tttttttt at address yyyyyyy + 1)

The write sequence can be composed by an unlimited number of data bytes.

MASTER TRANSMITS TO SLAVE RECEIVER (WRITE MODE)



2) R/$\overline{W}$ = "1" (READ)

In this case the slave acts as transmitter and, therefore, the transmission changes direction. The second byte of the sequence will be sent by the M8571 and it will contain the data present in the memory present at the address pointed by the "current" value of the address register. Following bytes will be the data present at the "next" addresses. At the end of each byte, the M8571 places a "1" on the bus during acknowledge time and waits for the master to send a "0" (meaning "acknowledge"). When the master want to stop the transfer, it gives a "1" (not "acknowledged"): as a consequence, the M8571 leaves the bus high so that the master can give the stop condition. An example is given below:

0. STA
1. 10100ss1 A
2. xxxxxxxx H (xxxxxxxx is the data present in the currently addressed memory location; H is the high level placed on the bus by M8571)

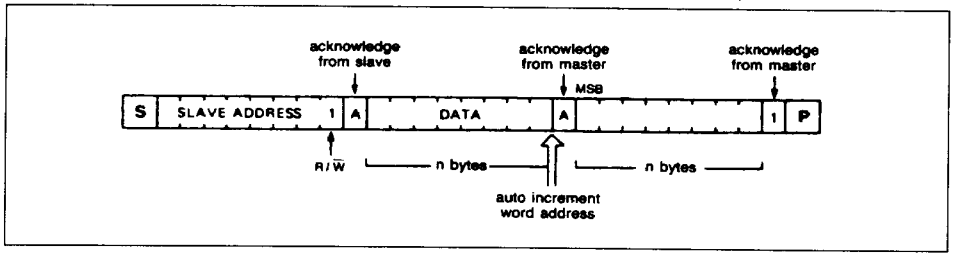
3) MIXED SEQUENCE

When the master wants to read a memory location different from the one currently addressed, a longer sequence is needed, which includes the writing of the address register. The sequence is as follows:

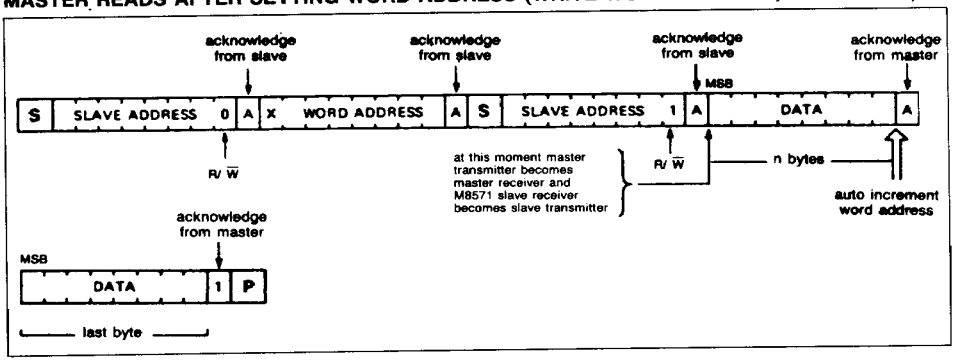
0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. STA
4. 10100ss1 A
5. xxxxxxxx H

Where xxxxxxxx is the data present in the yyyyyy memory location
As appears from the example, a start condition can be given without a previous stop condition.

MASTER READS SLAVE IMMEDIATELY AFTER FIRST BYTE (READ MODE)



MASTER READS AFTER SETTING WORD ADDRESS (WRITE WORD ADDRESS; READ DATA)



4) E/W TIME SPECS

After the beginning of an E/W operation at a certain location the M8571 is "busy" until the operation is finished. To show this busy state, the M8571 refuses acknowledge of the next data bytes to remove the M8571 from the "busy" state a data byte must be sent after the t_{EW} is over. This "dummy" byte will not be acknowledged and written. The data to be written in the next address must be sent again and will be acknowledged and written by the M8571.
The master device that wants to use the self increment feature must therefore keep sending the next data byte and monitoring the acknowledge bit until it becomes active.
The communication sequence on the bus becomes, therefore.

0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. zzzzzzzz A
4a. tttttttt H (not acknowledged when $t < t_{E/W}$)

after t_{EW}:

4b. tttttttt H (not acknowledged, the M8571 is removed from the "busy" state)
4c. tttttttt A (acknowledged, the M8571 starts writing data tttttttt at address yyyyyyyy + 1)

Now the M8571 will write data tttttttt at address yyyyyyy + 1

This usage mode keeps the bus unavailable for other tasks during the $t_{E/W}$ time. It is possible to free the bus by giving a stop condition (this condition stops only the bus sequence, not the E/W operation). After a stop condition the access sequence must be started again from the beginning (start).
The E/W circuitry in the M8571 performs automatically the "Erase before Write" sequence required by the technology. Furthermore, both erase and write last all (and only) the time needed for the required modification to happen (this is accomplished by an intelligent "compare and retry" circuitry). This optimizes E/W time but may have the drawback of "locking" the circuitry in case a memory location "breaks down" and can not be modified (in which case $t_{E/W}$ becomes infinite).
To overcome this drawback, it has been made possible to force the circuit out of the E/W status, that is to halt a modify operation. Two different modes are provided, depending on the value of the MS control pin:

$$MS \leqslant V_{IL}$$

The E/W operation is unconditionally stopped by a following valid chip address byte.

$$MS \geqslant V_{IH}$$

An opcode is provided to halt the operation (see "EEPROM mode" section).

5) WORD ADDRESS/OPCODE

The second byte transmitted in a write sequence can assume several meaning according to the value of the MS pin. In any case, it carries all the informations the M8571 needs to perform the desired operation.
MS can assume three different values:

- V_{IL} ($V_{IN} \leq 1.5V$)
- V_{IH} ($3.0V \leq V_{IN} < V_{CC}+1$)
- V_H ($9.0V \leq V_{IN} \leq 12V$)

With regards to the value of MS, the possible behaviours are:

a) MS = V_{IL} ("RAM mode")
In this mode the M8571 is compatible with the PCD 8571 RAM (128 x 8bit). The second byte of the sequence gives the address of the word to be selected, both for write and for read:
1. xyyyyyyy A
yyyyyyy is the word address; the first bit is "don't care; the main feature of this mode are the following:
. the memory appears as an 128 x 8 array
. only "byte operations are allowed;
. E/W operations are stopped by the following accesses.

b) MS = V_{IH} (EEPROM mode)

The word address-byte now must be regarded as mixed address-opcode byte; more precisely, the first three bits indicate the meaning to be attributed to the remainder of the byte. The possible combinations are:

0yyyyyyy	byte-mode (8 bits) RD or E/W at address yyyyyyy
10yyyyyy	word-mode (16 bits) RD or E/W at address yyyyyy
110yyyyy	page-mode (32 bits) RD or E/W at address yyyyy
11111111	E/W cycle stop
11100000	Read busy bit
11100100	Block Erase (needs V_H on MS pin, see also BLOCK mode)
11110001	Reload Address Register with pre-increment data

In this mode, as well as in RAM mode, the "busy" information is transmitted from the M8571 to the master using the "no acknowledge" format. Furthermore, "Read busy bit" instruction, which is always answered by the M8571 no matter what it is doing, allows the master to know wheter the "no acknowledge" condition comes from a "busy" status or from a malfunction; the "busy" status is signalled by the byte 11100101; the "no busy" by 00011010.
Also in this mode the self-incrementing address register is available, both for read and for write, for each word length.
The M8571 is provided with a double register for storing the address that is sent during the second byte of a write sequence.
When the self-incrementing is used, this address becomes the "starting address" of the modified string of bytes. The "reload" instruction allows the master to recover this address if it wants to read the modified string from the beginning, without the need for external storage of the "starting address".

c) MS = V_H (BLOCK mode)

The only instruction that can be executed in this mode is "Block Erase", which is useful to erase the whole array in a single shot. This can occur either during testing or at the set-up of a new system, when the whole memory must be written. When this instruction is given, the self-timing circuitry is disabled, so that the operation must be stopped (after t_{BE}) by the master executing a START on the bus. The "enable" feature obtained with the non standard level on MS was added to avoid unintentional clearing of the whole memory, whenever the "Block Erase" code was erroneously sent.

6) 16-bit or 32-bit OPERATIONS

The obvious advantage of an operation on 16 bits (a word) or on 32 bits (a page) is that the E/W time is 10ms for the whole word or page. When a word or page mode operation is required, the device behaviour undergoes some slight modifications:

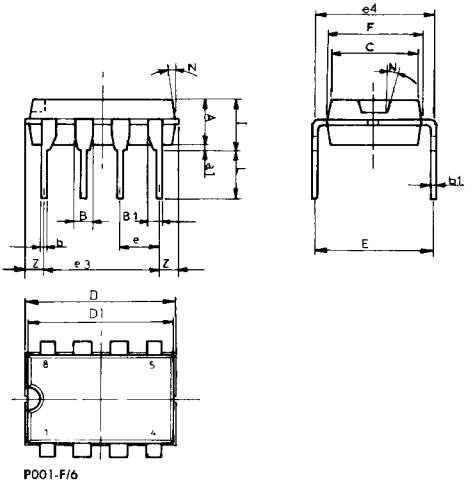
- The M8571 waits for receiving all the bytes that compose the word or the page before starting an E/W operation;
- The self-incrementing address register keeps into account the word or page lenght so that, at the end of a word or page mode operation, it points to the next word or page.

ORDERING INFORMATION

Port Number	Max Frequency	Supply Voltage	Temp. Range	Package
M8571B1	125 KHz	5V ± 10%	0° to +70°C	DIP-8
M8571B6	125 KHz	5V ± 10%	−40° to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063