Programmable Delay Lines

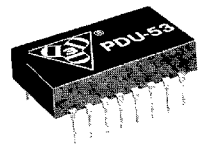
SERIES: PDU-53

100K ECL Interfaced
(3 BIT) 16 Pins DIP

data delay devices, inc.

Features:

- **3-BIT Programmable**
- **Accurate Timing**
- **Completely 100K ECL Interfaced**

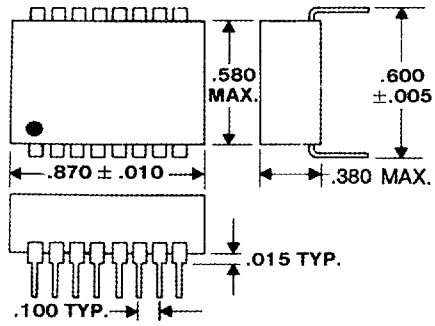


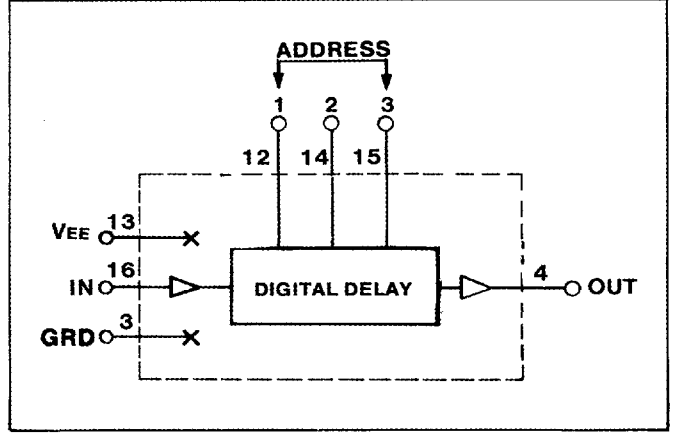
Specifications:

- **Min. input pulse width:** 3 ns or 15% of total delay whichever is greater.
- **Min. PRR:** 8 ns or 2 × pulse width whichever is greater.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** 5% or 40 ps whichever is greater.
- **Inherent delay (T_{DO}):** 2.2 ns.
- **Address to output prop. delay (T_{SUA}):** 2.9 ns max.
- **Power supply voltage:** −5V ± .7V.
- **Power supply current:** −150 ma.
- **Temperature coefficient:** 100 PPM/°C.
- **Operating temp. range:** 0°C to +85°C.
- **Storage temp. range:** −65°C to +150°C.
- **DC parameters:** See ECL-100K Logic Table on Page 6.

Test Conditions:

- **Input pulse width:** 10 ns
- **Input PRR:** 100 ns
- **Input pulse rise-time:** 1 ns
- **Input pulse voltage:** .8V p-p
- **Supply voltage (V_{EE}):** −4.5V
- **Ambient temperature(T_a):** +25°C





No pull-up resistors used internally on input & output.

Part No.	Delay Increment (ps)	Total Programmed Delay (ps)
PDU-53-100	100 ± 50	700
PDU-53-200	200 ± 60	1,400
PDU-53-250	250 ± 60	1,750
PDU-53-400	400 ± 80	2,800
PDU-53-500	500 ± 100	3,500
PDU-53-750	750 ± 100	5,250
PDU-53-1000	1,000 ± 200	7,000
PDU-53-1200	1,200 ± 200	8,400
PDU-53-1500	1,500 ± 200	10,500
PDU-53-2000	2,000 ± 400	14,000
PDU-53-2500	2,500 ± 400	17,500
PDU-53-3000	3,000 ± 500	21,000

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