Programmable Delay Lines

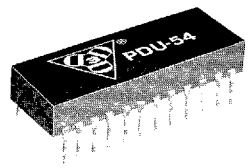
SERIES: PDU-54

100K ECL Interfaced
(4 BIT) 24 Pins DIP

data delay devices, inc.

Features:

- **4-BIT Programmable**
- **Accurate Timing**
- **Completely 100K ECL Interfaced**

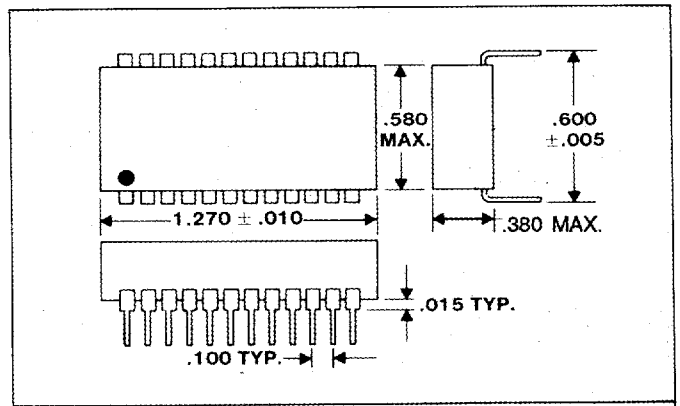


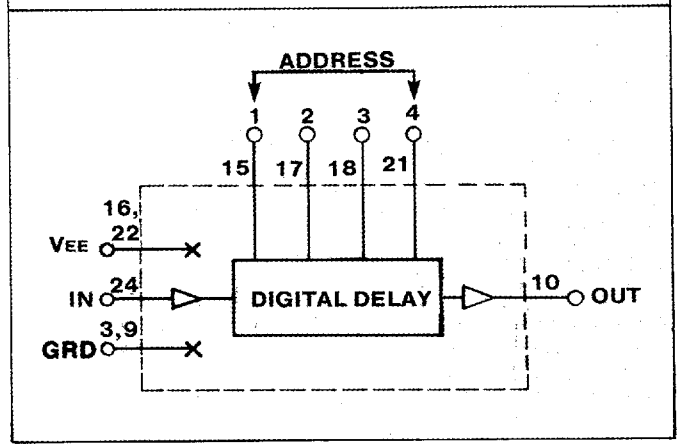
Specifications:

- **Min. input pulse width:** 3 ns or 10% of total delay whichever is greater.
- **Min. PRR:** 8 ns or 2 × pulse width whichever is greater.
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** 5% or 40 ps whichever is greater.
- **Inherent delay (T_{DO}):** 3.3 ns.
- **Address to output prop. delay (T_{SUA}):** 2.9 ns max.
- **Power supply voltage:** −5V ± .7V.
- **Power supply current:** −300 ma.
- **Temperature coefficient:** 100 PPM/°C.
- **Operating temp. range:** 0°C to +85°C.
- **Storage temp. range:** −65°C to +150°C.
- **DC parameters:** See ECL-100K Logic Table on Page 6.

Test Conditions:

- **Input pulse width:** 10 ns
- **Input PRR:** 100 ns
- **Input pulse rise-time:** 1 ns
- **Input pulse voltage:** .8V p-p
- **Supply voltage (V_{EE}):** −4.5V
- **Ambient temperature (T_A):** +25°C





No pull-up resistors used internally on input & output.

Part No.	Delay Increment (ps)	Total Programmed Delay (ns)
PDU-54-100	100 ± 50	1.50
PDU-54-200	200 ± 60	3.00
PDU-54-250	250 ± 60	3.75
PDU-54-400	400 ± 80	6.00
PDU-54-500	500 ± 100	7.50
PDU-54-750	750 ± 100	11.25
PDU-54-1000	1,000 ± 200	15.00
PDU-54-1200	1,200 ± 200	18.00
PDU-54-1500	1,500 ± 200	22.50
PDU-54-2000	2,000 ± 400	30.00
PDU-54-2500	2,500 ± 400	37.50
PDU-54-3000	3,000 ± 500	45.00

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