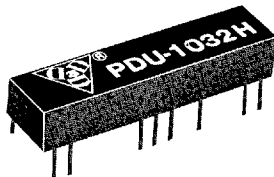


Digitally Programmable Delay Units

SERIES: PDU-1032H
(5-Bit) ECL Interfaced



Features:

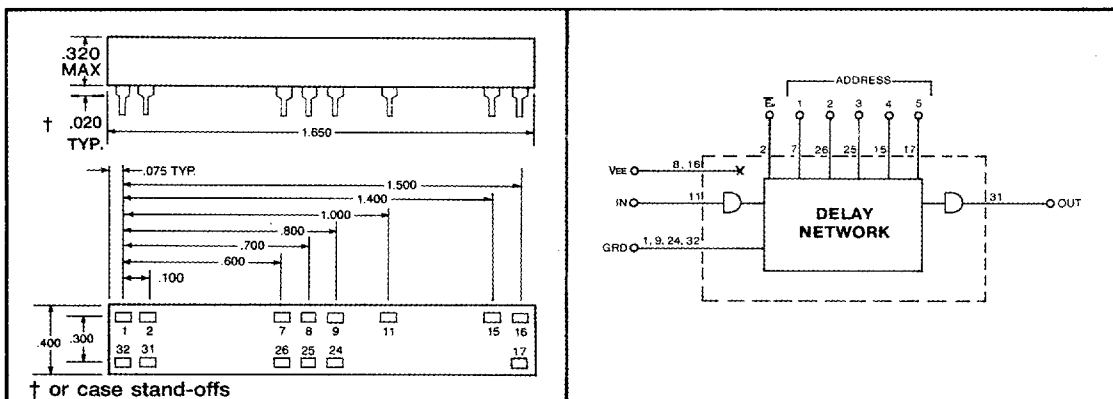
- Low propagation delay
- Input & output ECL buffered
- 5-BIT ECL programmable delay line
- Output same polarity of input
- Completely interfaced
- Compact & low profile

Specifications:

- **Delay variation:** Monotonic in one direction
- **Programmed delay tolerance:** $\pm 5\%$ or 2 ns whichever is greater.
- **Inherent delay (T_0):** 5.5 ns ± 1 ns for PDU-1032H-1 thru -5. Greater for rest of part numbers.
- **Propagation delay:**
Address to output (T_{SUA}) = 3.6 ns typ.
Enable to output (T_{SUE}) = 1.7 ns typ.
- **Power dissipation:** 615 mw typ.
- **Supply voltage:** -5 Vdc $\pm 5\%$.
- **Operating temperature:** 0-70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **DC parameters:** See ECL-10KH Logic Table on Page 6.

Test Conditions

- **Input pulse-width:** $\geq 150\%$ of Max. delay.
- **Input pulse spacing:** ≥ 3 times of Max. delay.
- **Input pulse voltage:** ECL logic.
- **Measurements taken @**
 $T_a = 25^\circ\text{C}$, $V_{EE} = -5\text{V}$.



TRUTH TABLE

Enable (\bar{E}_i)	Address					Delay Out
	5	4	3	2	1	
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{31}
1	ϕ	ϕ	ϕ	ϕ	ϕ	0

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
 T_0 = Reference or inherent delay of unit.
 $T_1 \rightarrow T_{31}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1032H-0.5	0.5 ± 0.3	15.5
PDU-1032H-1	1 ± 0.5	31
PDU-1032H-2	2 ± 0.5	62
PDU-1032H-3	3 ± 1.0	93
PDU-1032H-4	4 ± 1.0	124
PDU-1032H-5	5 ± 1.0	155
PDU-1032H-6	6 ± 1.0	186
PDU-1032H-8	8 ± 1.0	248
PDU-1032H-10	10 ± 1.5	310
PDU-1032H-12	12 ± 1.5	371
PDU-1032H-15	15 ± 1.5	465
PDU-1032H-20	20 ± 2.0	620

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