

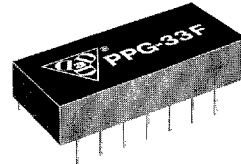
# Fast Logic Programmable Pulse Generator

SERIES: PPG-33F  
(3 Bit) TTL Interfaced



**Features:**

- Precise pulse widths
- 3-BIT address
- 1 ns to 50 ns incremental steps
- Trigger inherent delay  $T_{DO} = 3.5 \text{ ns} \pm 2 \text{ ns}$   
 $T_{DO} = 5.0 \text{ ns} \pm 2 \text{ ns}$
- Inherent pulse width  $PW_0 = 9 \text{ ns} \pm 2 \text{ ns}$   
 $PW_0 = 6 \text{ ns} \pm 2 \text{ ns}$
- Rising-edge triggered
- 14 pins DIP package
- Low profile



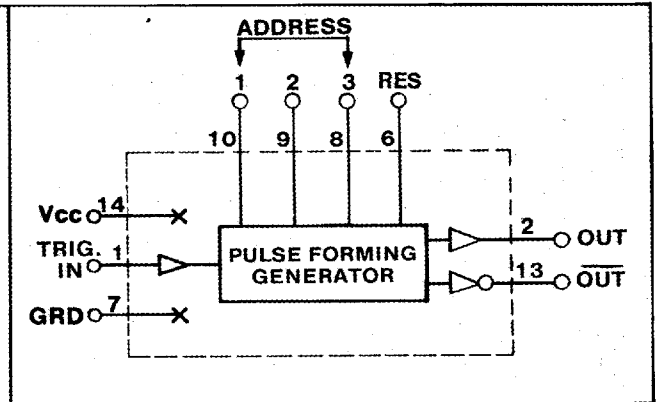
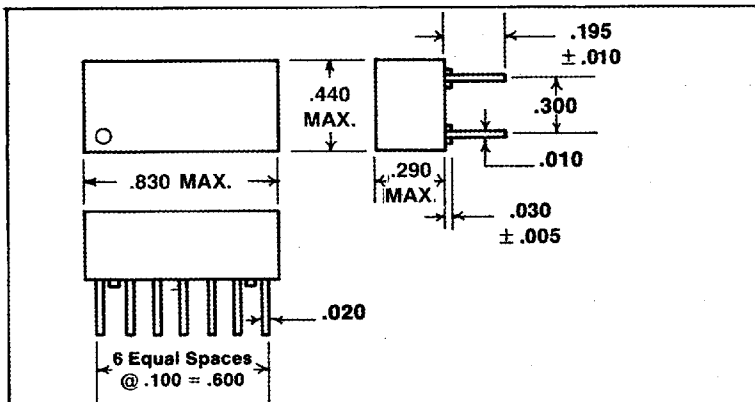
**Specifications:**

- Input pulse width: 6 ns min.
- Programmed pulse-width tolerance:  $\pm 5\%$  or 1 ns whichever is greater.
- Supply voltage (Vcc): 5 Vdc  $\pm 5\%$ .
- Operating temperature: 0° C to 70° C.
- Temperature coefficient: 100 PPM/° C.

■ Supply current:

- Iccl: 41 ma.
- Icch: 20 ma.

■ DC parameters: See TTL-Fast Schottky Logic Table on Page 6.



**TRUTH TABLE**

Enable RES	Address (Bit No.)			Pulse Width Out
	3	2	1	
0	0	0	0	$T_0$
0	0	0	1	$T_1$
0	0	1	0	$T_2$
0	0	1	1	$T_3$
0	1	0	0	$T_4$
0	1	0	1	$T_5$
0	1	1	0	$T_6$
0	1	1	1	$T_7$
1	0	0	0	0

1 = High  
 0 = Low  
 0 = Don't care  
 $T_0$  = Reference or inherent pulse width.  
 $T_1$  to  $T_7$  = Multiplier of pulse width.

Part Number	Incremental Pulse Width Per Step (ns)	Total Pulse Width Change (ns)
PPG-33F-5	.5 $\pm$ .3	3.5
PPG-33F-1	1 $\pm$ .4	7
PPG-33F-2	2 $\pm$ .4	14
PPG-33F-3	3 $\pm$ .5	21
PPG-33F-5	5 $\pm$ .6	35
PPG-33F-10	10 $\pm$ 1.0	70
PPG-33F-15	15 $\pm$ 1.3	105
PPG-33F-20	20 $\pm$ 1.5	140
PPG-33F-40	40 $\pm$ 2.0	280
PPG-33F-50	50 $\pm$ 2.5	350

Contact us for specific requirements. We customize.

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