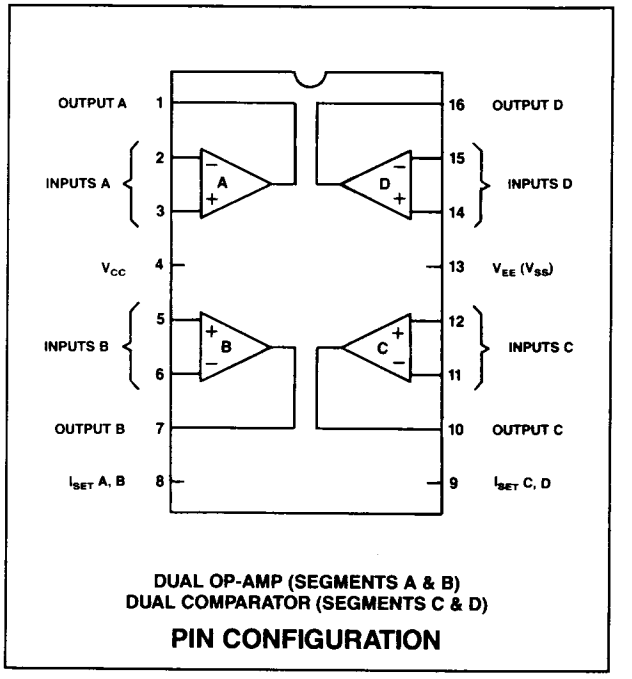
TL 14575
Dual OP AMP/Dual Comparator

GENERAL DESCRIPTION

The TL 14575 includes two internally compensated low power operational amplifiers plus two comparators in a single monolithic device.

Operating current may be programmed by choosing the value of an external resistor. This allows the TL 14575 to be used both in applications where high slew rates are demanded as well as in low power applications.

The TL 14575 is available in plastic and ceramic DIP, SOIC plastic package and in die form.



DUAL OP-AMP (SEGMENTS A & B)
DUAL COMPARATOR (SEGMENTS C & D)

PIN CONFIGURATION

FEATURES

- Replaces MC 14575
- Single 3V to 15V Power Supply OR Dual ±1.5V to ±7.5V Power Supplies
- Wide input voltage range
- Common mode range 0 to $V_{cc}-2$ Vdc (single supply)
- Typical offset <5mV (TL 14575-1)
- Resistor programmable current/slew rate
- Choice of 10mV or 50mV maximum offset
- Internally compensated op amps
- High input impedance
- MIL-STD-883 screening available
- CMOS and TTL compatible

TLSI, Inc. • 815 Broadhollow Road • Farmingdale, New York 11735 • Phone: (516) 755-7005 • Fax: (516) 755-7626

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{EE})

DC Supply Voltage, V_{CC} ..... −0.5 Vdc to +18 Vdc
Input Voltage, All Inputs, V_{in} ..... −0.5 Vdc to V_{CC} + 0.5 Vdc
DC Current Drain per Pin, I ..... 10 mAdc
Operating Temperature Range, T_A(military) ..... −55°C to +125°C
Operating Temperature Range, T_A (industrial) ..... −40°C to +85°C
Operating Temperature Range, T_A (commercial) ..... 0°C to +70°C
Storage Temperature Range, T_{stg} ..... −65°C to +150°C
Recommended Operating Supply Voltage Range, V_{CC} ..... +3.0 Vdc to +15 Vdc

General Note: Absolute maximum ratings are those limits which, if exceeded, may cause damage to the device. Proper operation is not implied at these limits.

ELECTRICAL CHARACTERISTICS

OPERATIONAL AMPLIFIER (V_{EE} = 0 V, T_A = 25°C)

PARAMETER	V_{CC} (Vdc)	MIN	TYP	MAX	UNITS	CONDITIONS
Input Common Mode Voltage Range, V_{ICR}	5.0 10 15	0 0 0		3.0 8.0 13	Vdc	I_{Set} = 200 µA
Output Voltage Range, V_{OR}	5.0 10 15	1.05 1.05 1.05		4.0 9.0 14	Vdc	I_{Set} = 50 µA R_L = 100 k
Input Offset Voltage, V_{IO} TL 14575 TL 14575-1	 10 10		 ±10 ±5.0	 ±50 ±10	mVdc	I_{Set} = 50 µA
Average Temperature Coefficient of Input Offset Voltage			20		µV/°C	
Input Bias Current, I_{IB}	10			1.0	nA	
Input Offset Current, I_{IO}	10			200	pA	
Open Loop Voltage Gain, A_{VOL}	10		90		dB	I_{Set} = 50 µA
Power Supply Rejection Ratio, PSRR	10		70		dB	
Common Mode Rejection Ratio, CMRR	10		80		dB	
Channel Separation	10		−100		dB	
Slew Rate, SR	10		2.5		V/µs	I_{Set} = 40 µA
Phase Margin, øm	10		45		Degrees	
Supply Current, Per pair, I_{CC}	5 10 15		50 100 150		µA	R_{Set} = 1 MΩ
Supply Current, Per pair, I_{CC}	5 10 15		0.5 1.2 1.8		mA	R_{Set} = 100 k

ELECTRICAL CHARACTERISTICS

COMPARATOR (V_{EE} = 0 Vdc, T_A = 25°C)

PARAMETER	V_{CC} (Vdc)	MIN	TYP	MAX	UNITS	CONDITIONS
Input Common Mode Voltage Range, V_{ICR}	5.0 10 15	0 0 0		3.0 8.0 13	Vdc	I_{Set} = 200 μA
Output Voltage — Low Level, V_{OL}	5.0 10 15		0 0 0	0.05 0.05 0.05	Vdc	I_{Set} = 50 μA
Output Voltage — High Level, V_{OH}	5.0 10 15	4.95 9.95 14.95	5.0 10 15		Vdc	I_{Set} = 50 μA
Output Drive Current (Military)					mAdc	I_{Set} = 50 μA
(V_{OH} = 2.5 Vdc) Source, I_{OH}	5.0	−2.4	−4.2			
(V_{OH} = 4.6 Vdc)	5.0	−0.51	−0.88			
(V_{OH} = 9.5 Vdc)	10	−1.3	−2.25			
(V_{OH} = 13.5 Vdc)	15	−3.4	−8.8			
(V_{OL} = 0.4 Vdc) Sink, I_{OL}	5.0	1.25	2.25		mAdc	I_{Set} = 50 μA
(V_{OL} = 0.5 Vdc)	10	3.25	5.6			
(V_{OL} = 1.5 Vdc)	15	8.5	20			
Output Drive Current (Commercial, Industrial)					mAdc	I_{Set} = 50 μA
(V_{OH} = 2.5 Vdc) Source, I_{OH}	5.0	−2.1	−4.2			
(V_{OH} = 4.6 Vdc)	5.0	−0.44	−0.88			
(V_{OH} = 9.5 Vdc)	10	−1.1	−2.25			
(V_{OH} = 13.5 Vdc)	15	−3.0	−8.8			
(V_{OL} = 0.4 Vdc) Sink, I_{OL}	5.0	1.2	2.25		mAdc	I_{Set} = 50 μA
(V_{OL} = 0.5 Vdc)	10	2.6	5.6			
(V_{OL} = 1.5 Vdc)	15	7.5	20			
Input Offset Voltage, V_{IO}					mVdc	I_{Set} = 50 μA
TL 14575	10			±50		
TL 14575-1	10			±10		
Average Temperature Coefficient of Input Offset Voltage			20		μV/°C	
Input Bias Current, I_{IB}	10			1.0	nA	
Input Offset Current, I_{IO}	10			200	pA	
Open Loop Voltage Gain, A_{VOL}	10		96		dB	I_{Set} = 50 μA
Power Supply Rejection Ratio, PSRR	10		70		dB	
Common Mode Rejection Ratio, CMRR	10		80		dB	
Channel Separation	10		−100		dB	
Output Rise Time, t_{TLH} and Fall Time, t_{THL}	10		100		ns	I_{Set} = 50 μA C_L = 50 pF
Propagation Delay Time, 5mV Overdrive, t_d	10		1000		ns	I_{Set} = 50 μA C_L = 50 pF
Supply Current—Per pair, I_{CC}	5 10 15		50 100 150		μA	R_{Set} = 1 MΩ
Supply Current—Per pair, I_{CC}	5 10 15		0.45 1.0 1.5		mA	R_{Set} = 100 k

TL 14575
Dual OP AMP/Dual Comparator

The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{EE} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

$$I_{Set}\,(\mu A) \approx \frac{V_{CC} - V_{EE} - 1}{R_{Set}\,(M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair are then given by:

$$I_{SetA,B} = I_{SetC,D}\,(\mu A) \approx \frac{V_{CC} - V_{EE} - 1}{2\,R_{Set}\,(M\Omega)}$$

If a pair of op amps or comparators are not used, the I_{Set} pin for that pair may be tied to V_{CC} for minimum power consumption.

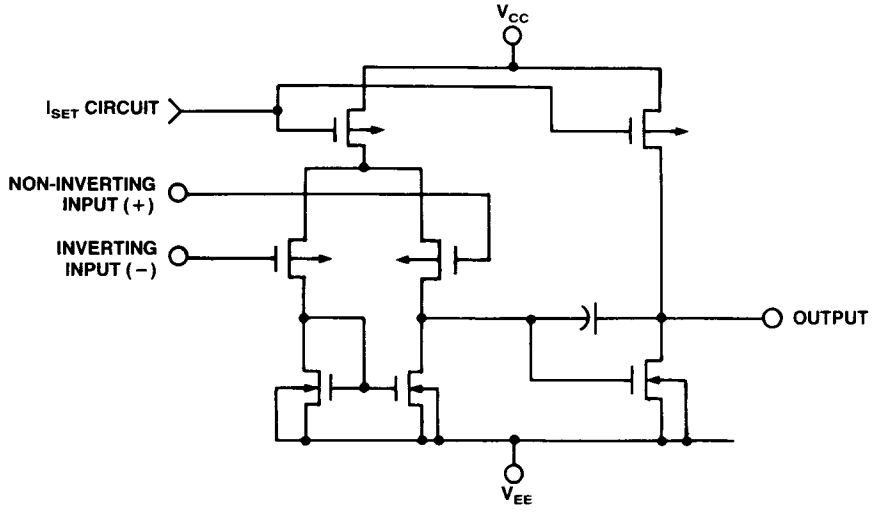
It should be noted that increasing I_{Set} for comparators will decrease propagation delay for that comparator.

For operational amplifiers, the maximum obtainable output voltage (V_{OH}) for a given load resistor connected to V_{EE} is given by:

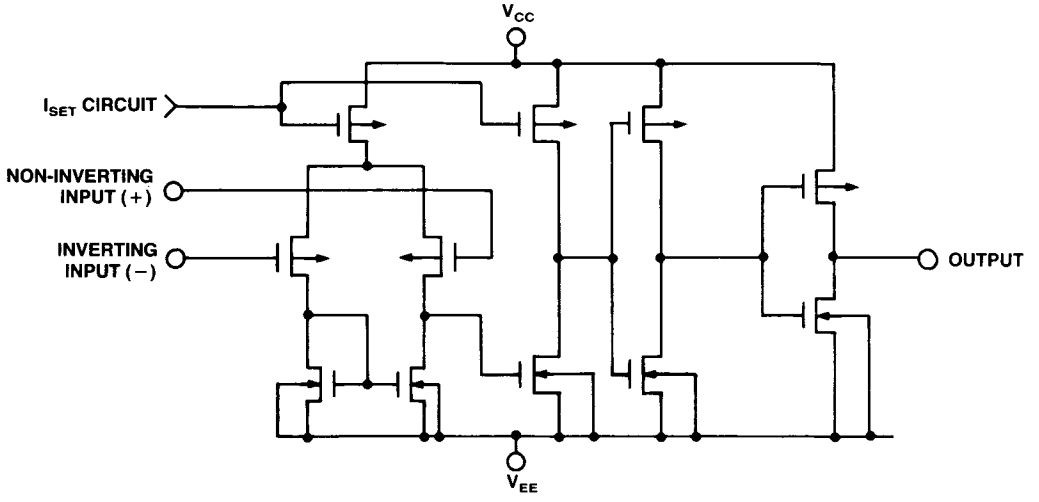
$$V_{OH} = (4 \times 10^{-3}\, I_{Set})R_L - 0.05 \text{ v}, \; R_L \text{ in } k\Omega$$
$$\text{if } (4 \times 10^{-3}\, I_{Set})R_L < V_{DD}, \; I_{Set} \text{ in } \mu A$$

Typical op amp slew rates are given by:

$$S_R \approx 0.05\, I_{Set}\,(V/\mu s), \; I_{Set} \text{ in } \mu A$$



SCHEMATIC DIAGRAM, OPERATIONAL AMPLIFIER



SCHEMATIC DIAGRAM, COMPARATOR

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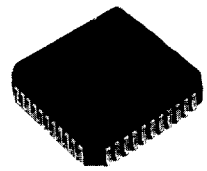
PACKAGES



DUAL IN-LINE PACKAGES (DIP)

PLASTIC DIP	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERAMIC DIP, SIDE BRAZED	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERDIP	8 through 24 (300 mil); 24 through 48 (600 mil)

SURFACE MOUNT PACKAGES

SOIC	8 through 16 (150 mil); 16 through 28 (300 mil)
PLCC	20 through 84
QUAD FLAT PACK	44 through 208
BUMPERED QFP	100 and up
CHIP CARRIER (LCC)	18 through 68
CERAMIC QFP	44 through 160 (EIJ); 132 through 164 (JEDEC)
CERFLAT	14 through 28
CERQUAD	20 through 68

PIN GRID ARRAYS

PLASTIC PGA	28 through 244
PGA	28 through 244

This is a partial list; consult factory for availability of other packages.
NOTE: Devices are available in anti-static tubes or trays, on tape & reel, or in die form.