BIMOS LATCH/DRIVERS

PRODUCT PREVIEW

The UCN4801A is a high-voltage, high-current latch/driver comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

The unit feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

- High-voltage, high-current outputs
- Output transient protection
- CMOS, PMOS, NMOS, TTL Compatible inputs
- Internal pull-down resistors
- Low-power CMOS latches

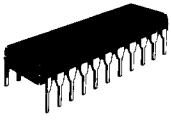
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
		DP
UCN 4801A	– 20°C to + 85°C	●

BIMOS

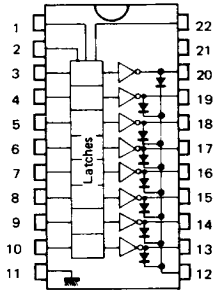
LATCH/DRIVERS

CASE CB-180



DP SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT
(Top view)



1 - Clear	22 - Output enable
2 - Strobe	21 - V_{CC}
3 - Input 1	20 - Output 1
4 - Input 2	19 - Output 2
5 - Input 3	18 - Output 3
6 - Input 4	17 - Output 4
7 - Input 5	16 - Output 5
8 - Input 6	15 - Output 6
9 - Input 7	14 - Output 7
10 - Input 8	13 - Output 8
11 - GND	12 - Common

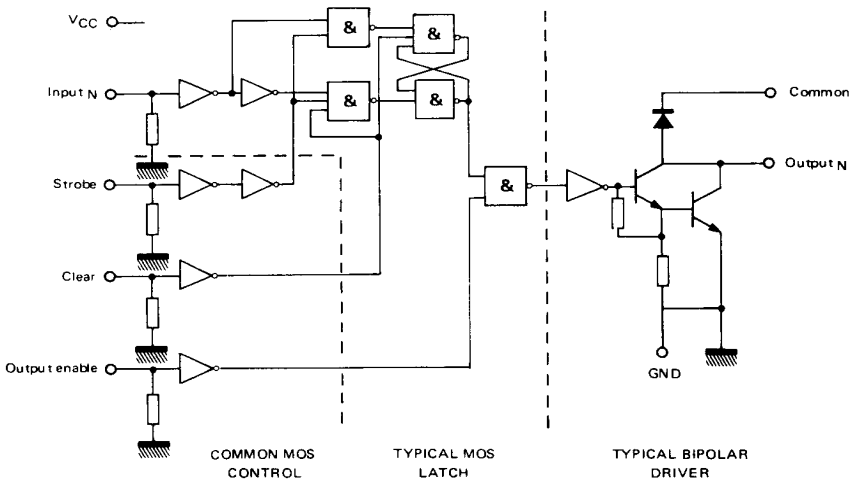
Ref. 04800

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Output voltage	V_O	50	V
Supply voltage	V_{CC}	18	V
Input voltage range	V_I	-0.3 to V_{CC}+0.3	V
Continous collector current	I_C	500	mA
Power dissipation*	P_{tot}	2.0	W
Operating ambient temperature range	T_{oper}	− 20 to+ 85	°C
Storage temperature	T_{stg}	− 55 to+ 125	°C

* Derate at the rate of 20mW/°C above Tamb = +25°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 5 V (Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Output leakage current (V_O = 50 V) T_{amb} = + 25°C T_{amb} = + 70°C	I_O	 – –	 – –	 50 100	μA
Collector-Emitter saturation voltage I_O = 100 mA I_O = 200 mA I_O = 350 mA, V_{CC} = 7V	$V_{O(Sat)}$	 – – –	 0.9 1.1 1.3	 1.1 1.3 1.6	V
Input voltage V_{CC} = 15 V V_{CC} = 10 V V_{CC} = 5 V - (Note 1)	$V_{I(O)}$ $V_{I(1)}$	– 13.5 8.5 3.5	– – – –	1 – – –	V
Input resistance V_{CC} = 15 V V_{CC} = 10 V V_{CC} = 5 V	R_{IN}	 50 50 50	 200 300 600	 – – –	KΩ
Supply current - Outputs open V_{CC} = 15 V V_{CC} = 10 V V_{CC} = 5 V All drivers off, all inputs = 0 V	$I_{CC(on)}$ (each stage) $I_{CC(off)}$	 – – – –	 1 0.9 0.7 50	 2 1.7 1 100	mA μA
Clamp diode leakage current (V_R = 50V) T_{amb} = + 25°C T_{amb} = + 70°C	I_R	 – –	 – –	 50 100	μA
Clamp diode forward voltage I_F = 350 mA	V_F	–	1.7	2	V

Note 1 : Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic «1».

TRUTH TABLE

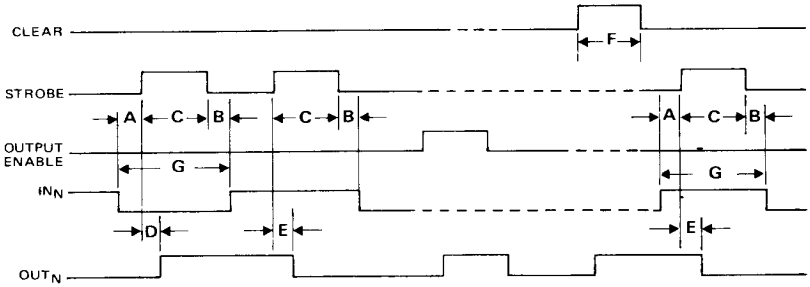
IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

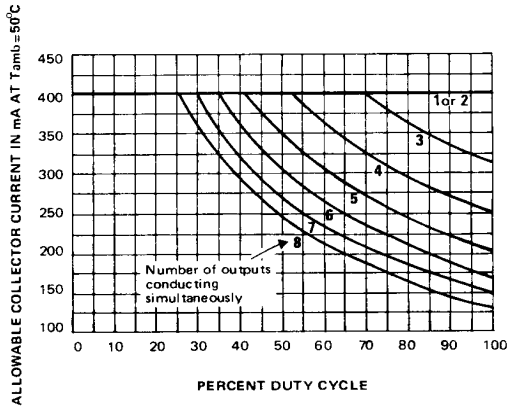
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

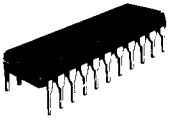
(Logic levels are V_{CC} and GND) V_{CC} = 5V, Tamb = 25°C



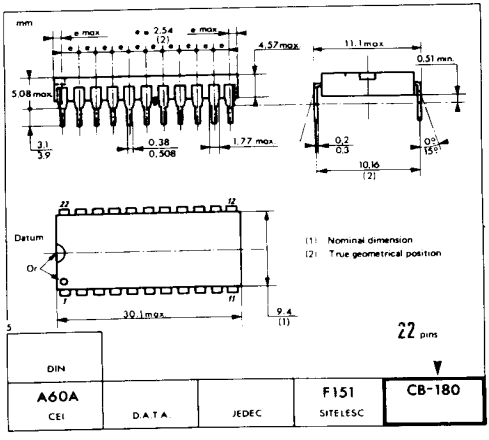
A.	Minimum data active time before strobe enabled (data set-up time)	100 ns
B.	Minimum data active time after strobe disabled (data hold time)	100 ns
C.	Minimum strobe pulse width	300 ns
D.	Typical time between strobe activation and output on to off transition	500 ns
E.	Typical time between strobe activation and output off to on transition	500 ns
F.	Minimum clear pulse width	300 ns
G.	Minimum data pulse width	500 ns



CB-180



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.