CMOS 4-BIT MICROCONTROLLER

TMP47C425AF

The 47C425A is the high speed and high performance 4-bit single chip microcomputer with LCD driver, based on the TLCS-47 CMOS series. The 47C425A has two oscillation circuits. It is possible to switch the operating mode ; high speed operation and low power consumption operation.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C425AF	4096 x 8-bit	256 x 4-bit	QFP67	TMP47C925AG

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time :
  1.9μs (at 4.2MHz), 244μs (at 32.8KHz)
- ◆89 basic instructions
- ◆Table look-up instrucitons
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (27 pins)
  - Input 1 port 4 pins
  - I/O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆LCD driver (automatic display)
  - LCD direct drive (Max. 12-digit display at 1/4 duty LCD)
  - 1/4, 1/3, 1/2 duty or static drive are programmably selectable.
- ◆Dual clock operation
  High-speed/low-power-consumption operating mode
- ◆Real Time Emulator : BM47212A

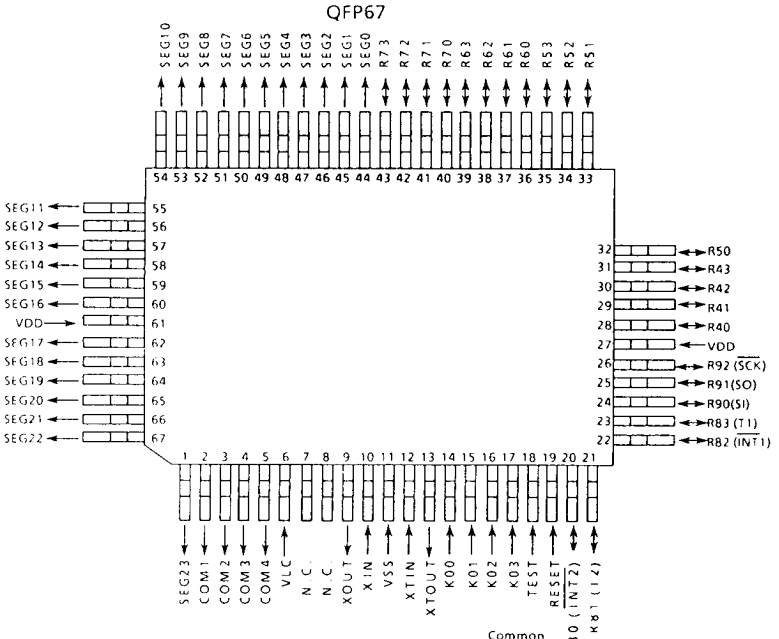
QFP67

TMP47C425AF

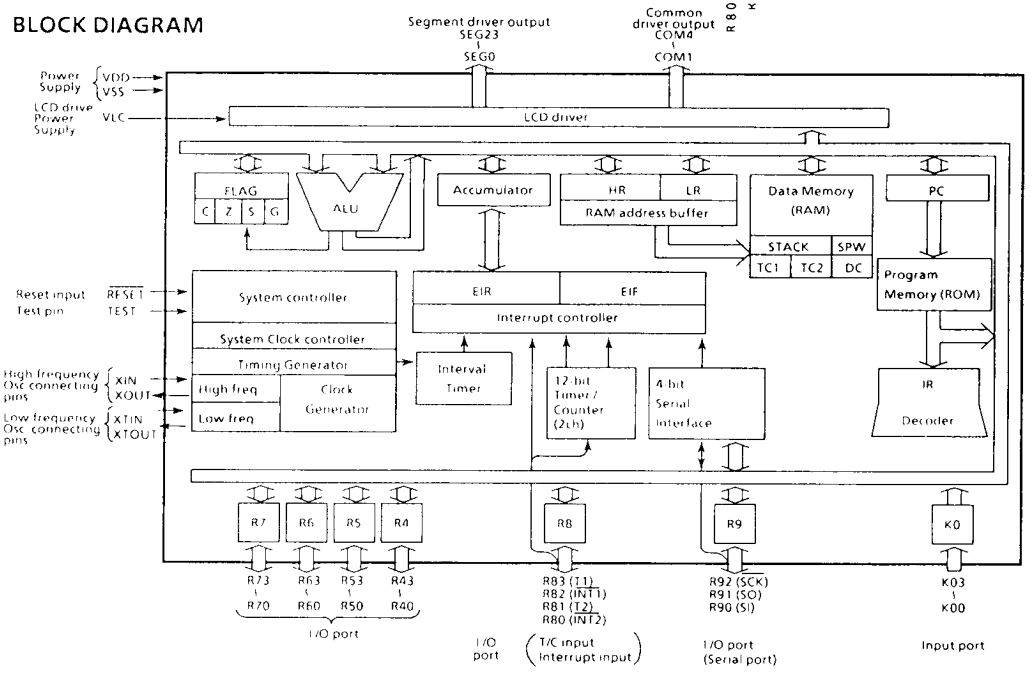
QFC67

TMP47C925AG

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
R43 - R40	I / O	4-bit I/O port with latch. When using as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and tested by the manipulation of the L-register indirect addressing.	
R53 - R50			
R63 - R60			
R73 - R70			
R83(T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82($\overline{INT1}$)			External interrupt 1 input
R81(T2)			Timer/Counter 2 external input
R80($\overline{INT2}$)			External interrupt 2 input
R92($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91(SO)	I / O (Output)		Serial data output
R90(SI)	I/O (Input)		Serial data input
SEG23 - SEG0	Output	LCD segment driver output	
COM4 - COM1		LCD common driver output	
XIN	Input	Resonator connecting pins (High-frequency). For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
XTIN	Input	Resonator connecting pins (Low-frequency). For inputting external clock, XTIN is used and XTOUT is opened.	
XTOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C425A, the configuration and functions of hardwares are described. As the description include mainly differences from the 47C400A, refer to the technical data sheets for the 47C400A.
The 47C425A doesn't have the hold function.

1. SYSTEM CONFIGURATION

(1) I/O Ports
(2) System Clock Controller
(3) Interval Timer
(4) Timer/Counter (TC1, TC2)
(5) Serial Interface
(6) LCD Driver

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O Ports

The 47C425A has 7 ports (27 pins) each as follows:

① K0 ; 4-bit input
② R4, R5, R6, R7 ; 4-bit input/output
③ R8 ; 4-bit input/output (Shared by external interrupt input and Timer/Counter input)
④ R9 ; 3-bit input/output (Shared by serial port)

P1, P2, and KE ports are eliminated from the 47C400A. Table 2-1 lists the port address assignments and I/O instructions that can access the ports. The 5-bit to 8-bit data conversion instruction [OUTB @HL] is invalid.

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	SIO status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	——	–	–	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	System Clock control	–	○	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	LCD driver control	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial Interface control	–	○	–	–	–	–	–

Note. "——" means the reserved state. Unavailable for the user programs.

Table 2-1. Port Address Assignments and Available I/O Instructions

2.2 System Clock Controller

The 47C425A has two oscillation circuits with a high-frequncy clock and a low-frequency clock. Power consumption can be decreased by switching to low-speed operation using the low-frequency clock when necessary (dual clock operation). The high-frequency clock can be obtained by connecting an oscillator to the XIN and XOUT pins; the low-frequency clock can be obtained by connecting the oscillator to the XTIN and XTOUT pins.

2.2.1 Ciucuit Configuration

Figure 2-1 shows the configuration of system clock controller.

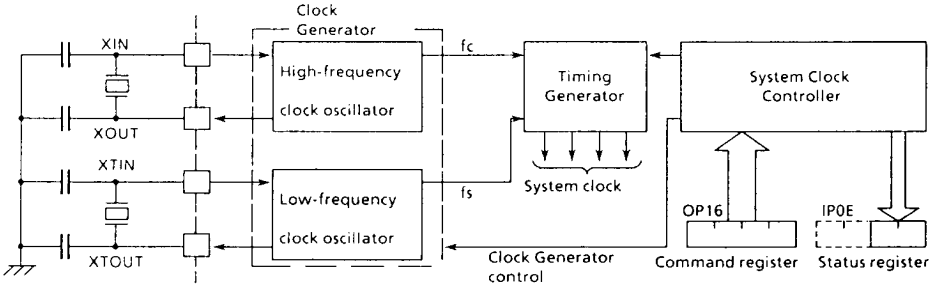


Figure 2-1. System Clock Controller

2.2.2 Dual Clock Operation and Control

Dual clock operation involves two modes: Normal operating mode using the high-frequency clock, and SLOW operating mode using the low-frequency clock. Both oscillators start operating when the power is turned on, after which the Normal operation is selected automatically. Operating mode switching is performed using the command register (OP16).

Bit 2 of OP16 is set to "1" to switch from Normal operation to SLOW operation. The high-frequency clock will stop oscillating at this time.

Returning from SLOW operation to Normal operation is performed by clearing bit 2 of OP16 to "0" and, at the same time, setting the warm up time in the lower 2 bits (DWUT). When the set warm up time has elapsed, the Normal operation is entered. During reset, the mode is Normal operation. Figure 2-2 shows operating mode transition. Figure 2-4 shows the command registers.

(1) Operating Mode Transition

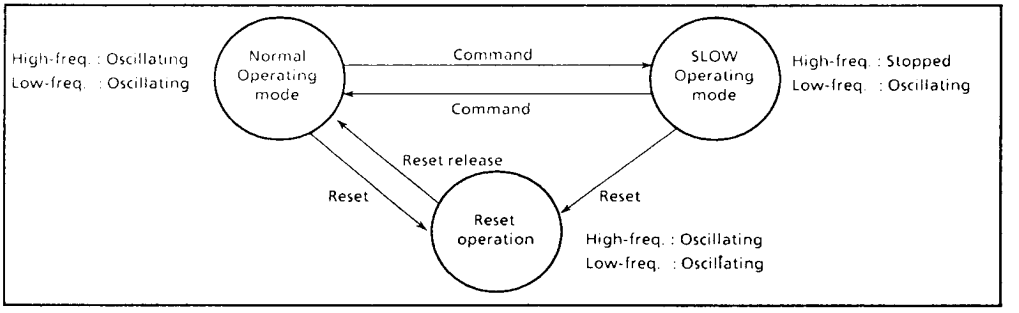


Figure 2-2. Operating Mode Transition Diagram

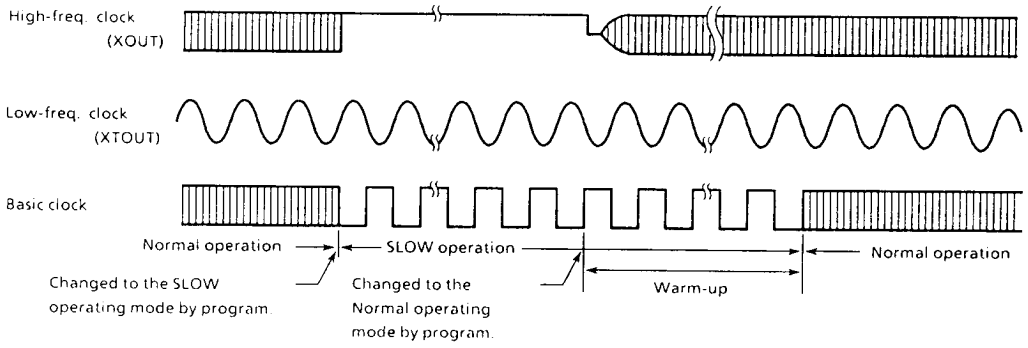


Figure 2-3. System Clock Switching Timing

(2) Operating Mode Control

System Clock control command register (Port address OP16)

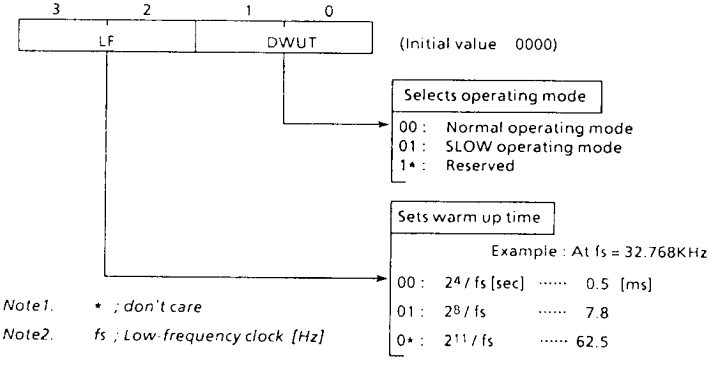


Figure 2-4. Command Register

Note 1. The following operations and functions connot be used in the SLOW operation ; therefore, this must be taken into consideration in programming.

(1) Timer/Counter 4096Hz (at fs = 32.8kHz) count operation (can be used with other count rates).

2 Interval timer interrupt 4096Hz (at fs = 32.8kHz) operation (can be used with other timer rates).

3 Serial Interface.

Note 2. The power consumption of the oscillator and internal hardware is decreased in the SLOW operation, but power consumption through pin interfaces (dependent on the external circuitry and program) may prevent overall low power consumption operation; therefore, caution is necessary during system design and interface circuit design.

2.3 Interval Timer

2.3.1 Configuration of Interval Timer

The interval timer is configured with a 15-stage binary counter and inputs the oscillation circuit output (fs) for the low-frequency clock; therefore, the final stage output is $fs/2^{15}$ [Hz]. This interval timer is cleared to "0" during reset.

Also, "fs" is input directly into the interval timer; therefore, the interval timer interrupts, timer/counter and LCD driver will not operate normally if the low-frequency oscillation is not stable.

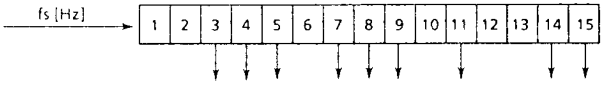


Figure 2-5. Interval Timer

2.3.2 Interval Timer Interrupt (ITMR)

Constant-frequency interrupts can be generated using the interval timer, Four different frequencies can be selected for interval timer interrupts using the command register (OP19). The command register is also initialized to "0" during reset.

An interval timer interrupt is generated at the first rising edge of the binary counters output after the command is set to the command register.

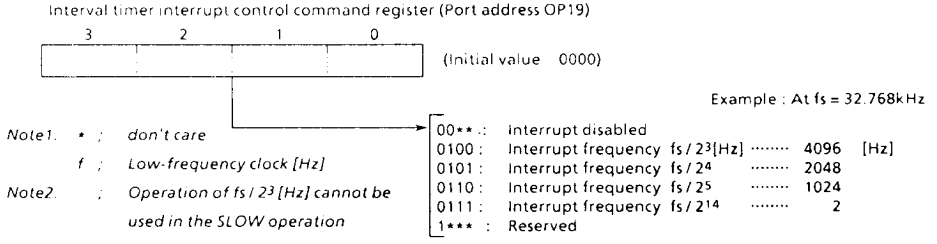


Figure 2-6. Command Register

2.4 Timer/Counter

The timer / counter of the 47C425A is operated by a low-frequency clock (fs); therefore, the following operating frequencies differ from those of the 47C400A.

① Internal pulse rate.
② Maximum frequency applied in the event counter mode.
③ Drop ratio of instruction execution time when the timer is used.

(1) Internal pulse rate

The intrnal pulse rates shown in Table 2-2 can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D).

The values of lower 2 bits (bit1, 0)	Internal pulse rate	Max. setting time	At fs = 32.768KHz	
			Internal pulse rate	Max. setting time
00	$fs / 2^3$ [Hz]	$2^{15} / fs$ [sec]	4096 [Hz]	1 [sec]
01	$fs / 2^7$	$2^{19} / fs$	265	16
10	$fs / 2^{11}$	$2^{23} / fs$	16	256
11	$fs / 2^{15}$	$2^{27} / fs$	1	4096

Table 2-2. Internal Pulse Rate

(2) Maximum frequency applied in the event counter mode.

		Normal operating mode	SLOW operating mode
a. In 1-channel operation		fc / 32 [Hz]	fs / 32 [Hz]
b. In 2-channel operation	TC1	fc / 32	fs / 32
	TC2	fc / 40	fs / 40

(3) Drap ratio of instruction execution time when the timer is used.
With the 47C425A, count operation is inserted in the ratio of once per [(basic clock frequency) /2^3] / (internal pulse rate) instruction cycle; therefore, execution speed drops as follows:

$$100 \div \left\{ \frac{(\text{basic clock frequency}) / 2^3}{(\text{internal pulse rate})} - 1 \right\} \%$$

Example 1: When fc = 4MHz and fs = 32.8kHz in the Normal operation and the internal pulse rate fs/2^3 is selected, count operation is inserted once per each cycle of 122 instructions; therefore, there is a drop of 100/121 = 0.83% for an instruction execution speed of 2μs.

Example 2: When fs = 32.8kHz in the SLOW operation, and the internal pulse rate fs/2^{11} is selected, count operation is inserted once per each cycle of 256 instructions; therefore, there is a drop of 0.39% for an instruction execution speed of 244μs. In addition, when the basic clock is obtained from "fs" (SLOW operation), count operation cannot be used with an internal pulse rate of fs/2^3.

2.5 Serial Interface

When operating using the internal clock, fs/2^2 [Hz] is used as the serial clock. Consequently, when operating at fs = 32.768kHz, the maximum transfer rate is 8192bps. When the reading and writing of serial data cannot follow this clock rate, the serial clock is automatically stopped and the next shift operation stands by untill the processing is completed.
External clock can be used in the same way as for the 47C400A. The serial interface cannot be used in the SLOW operating mode.

2.6 LCD Driver

The 47C425A has built-in circuit that directly drives the Liquid Crystal Display (LCD) and its control circuit.
The 47C425A has the following connecting pins with:

① Segment output pin 24 pins (SEG23 - SEG0)
② Common output pin 4pins (COM4 - COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD devices of following drive methods :

1. 1 / 4 duty (1 / 3 bias) LCD ..... Max.96 segments (8 segments × 12 digits)
2. 1 / 3 duty (1 / 3 bias) LCD ..... Max.72 segments (8 segments × 9 digits)
3. 1 / 2 duty (1 / 2 bias) LCD ..... Max.48 segments (8 segments × 6 digits)
4. Static LCD ..... Max.24 segments (8 segments × 3 digits)

2.6.1 Circuit Configuration

Figure 2-7 shows the configuration of the LCD driver.

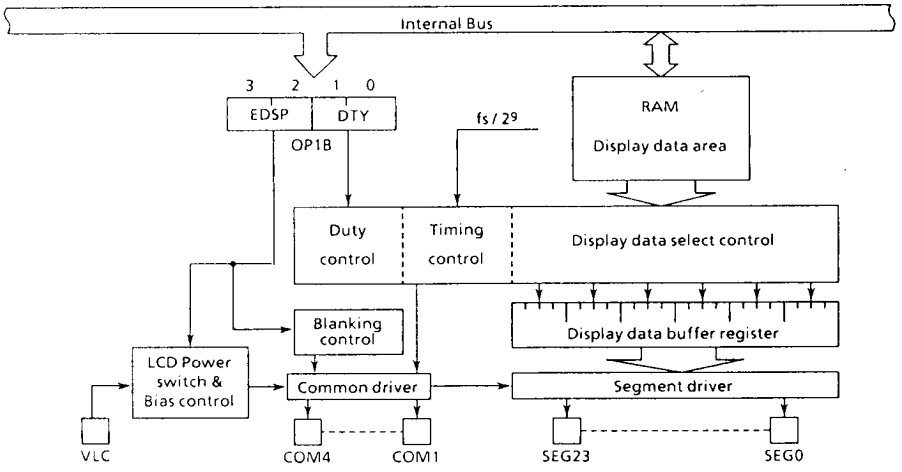


Figure 2-7. Configuration of LCD Driver

2.6.2 Control of LCD Driver

The LCD driver is controlled by the command register (OP1B).

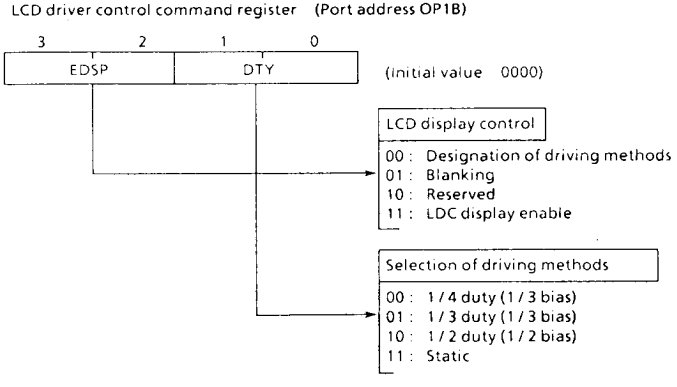
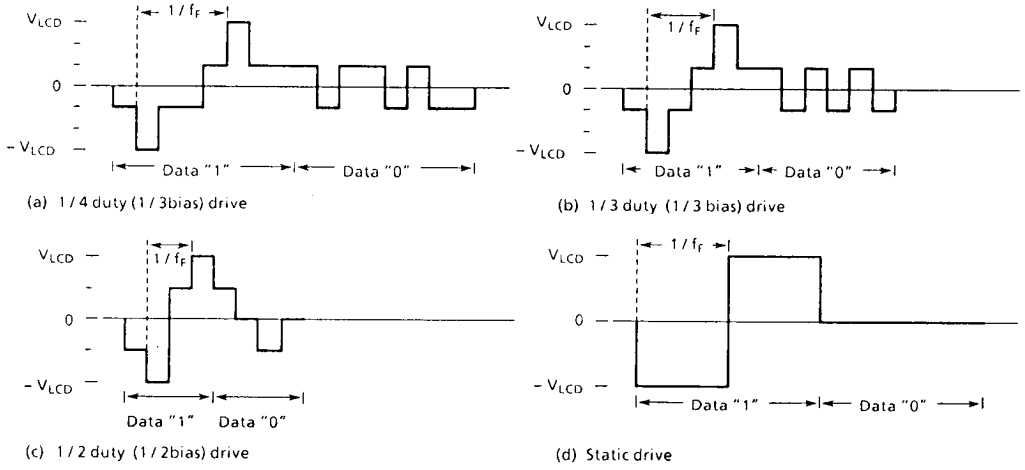


Figure 2-8. LCD Driver Control Command Register

(1) Driving methods of LCD

4 kinds of driving methods can be selected by DTY (bits 1 and 0 of command register).
Figure 2-9 shows driving waveforms for LCD.



Note. : f_F ; Frame frequency V_{LCD} ; LCD drive voltage (= V_{DD}-V_{LC})

Figure 2-3. Driving Waveform for LCD (Voltage between COM-SEG)

(2) Frame frequency

The frame frequency is set accoding to the driving method and base frequency as shown in Table 2-3.
The base frequency is given by the Interval Timer.

Base Frequency[Hz] \ Driving Method	Frame Frequency [Hz] 1/4duty	1/3duty	1/2duty	static
$\frac{fs}{2^9}$	$\frac{fs}{2^9}$	$\frac{4}{3} \cdot \frac{fs}{2^9}$	$\frac{4}{2} \cdot \frac{fs}{2^9}$	$\frac{fs}{2^9}$
At fs = 32.768KHz	64	85	128	64

fs ; Basic clock frequency [Hz]

Table 2-3. Frame Frequency Setting

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is obtained from the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.
The LCD light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.
During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage. Both the segment output and common output become V_{DD} level at this time and the LCD turn off.
The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bits 2 and 3 of the command register) to "11_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

2.6.3 LCD Display Operation

(1) Display data setting

Display data are stored to the display data area (Max. 24 words) in the data memory.

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.

Figure 2-10 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method; therefore, the number of display data area bits used to store the data also differs (Refer to Table 2-4). Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

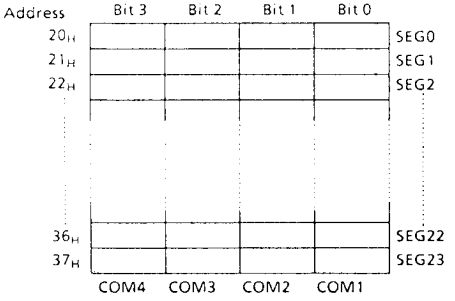


Figure 2-10. Display Data Area and SEG/COM

Driving Method	Bit 3	Bit 2	Bit 1	Bit 0
1 / 4 duty	COM4	COM3	COM2	COM1
1 / 3 duty	–	COM3	COM2	COM1
1 / 2 duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

Table 2-4. Driving Method and Bit for Display Data

(2) Blanking

Blanking is applied by setting EDSP to "01_B" and turns off the LCD by outputting the non light operation level to the COM pin. The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

2.6.4 Control Method of LCD Driver

(1) Initial Setting

Flow chart of initial setting is shown in Figure 2-11.

Example : Driving of 1 / 4duty LCD

```
LD      A, #0000B   ; Sets 1/4 duty drive
OUT     A, %OP1B
 :                  ; Initializes display data area
 :
LD      A, #1100B   ; Enable display (Relese of blanking)
OUT     A, %OP1B
 :
```

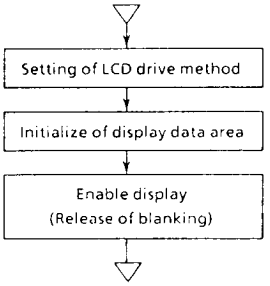


Figure 2-11. Initial Setting of LCD Driver

(2) Display Data

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction. This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 2-12 and the display data are as shown in Table 2-5.

Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20_H and 21_H.

```
        LD      HL, #0FCH           ; Sets the data counter
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16 ,@HL+
        ST      #DTBL/256,@HL+
        LD      HL,#20H             ; Stores display data
        LDL     A, @DC
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        :
DTBL : DATA     11011111B, 00000110B, 11100011B, 10100111B, 00110110B,
                10110101B, 11110101B, 00010111B, 11110111B, 10110111B
```

Numeral	Display	Display data		Numeral	Display	Display data	
		Upper	Lower			Upper	Lower
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 2-5. Example of Display Data (1/4 Duty)

Table 2-6 shows the same numerical display used in Table 2-5, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are the same as those shown in Figure 2-14.
Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20 through 23_H.

```
        LD      HL, 0FCH            ; Sets the data counter
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16,   @HL+
        ST      #DTBL/256,  @HL+
        LD      HL, #20H            ; Stores display data
        LDL     A, @DC
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
         :
DTBL : DATA     01110111B, 00100010B, 10010111B, 10100111B, 11100010B,
                11100101B, 11110101B, 01100011B, 11110111B, 11100111B
```

Numeral	Display data				Numeral	Display data			
	Upper			Lower		Upper			Lower
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**10	**01	**11	7	**01	**10	**00	**11
3	**10	**01	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

*Note. * ; don't care*

Table 2-6. Example of Display Data (1/2 Duty)

(3) Driving Example

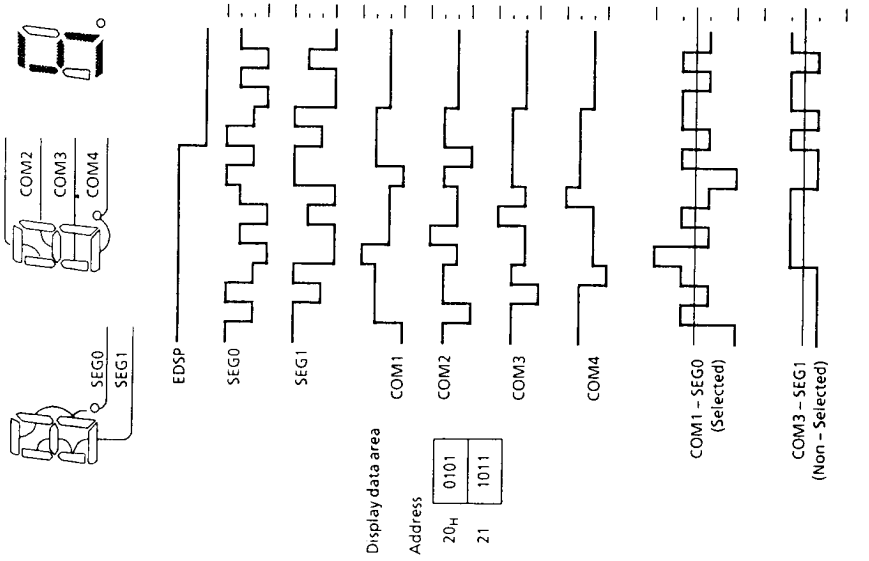


Figure 2-12. 1/4 Duty (1/3 Bias) Drive

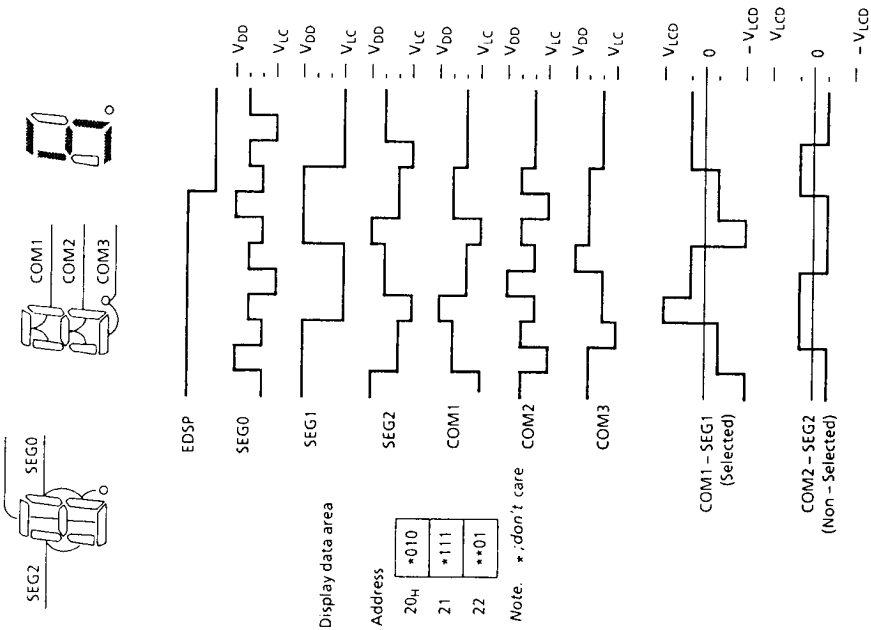


Figure 2-13. 1/3 Duty (1/3 Bias) Drive

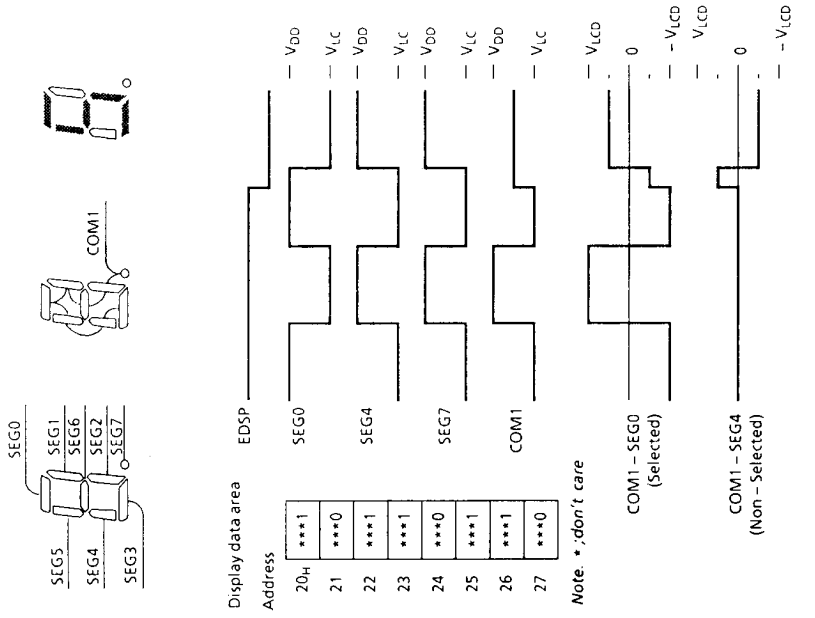


Figure 2-15. Static Drive

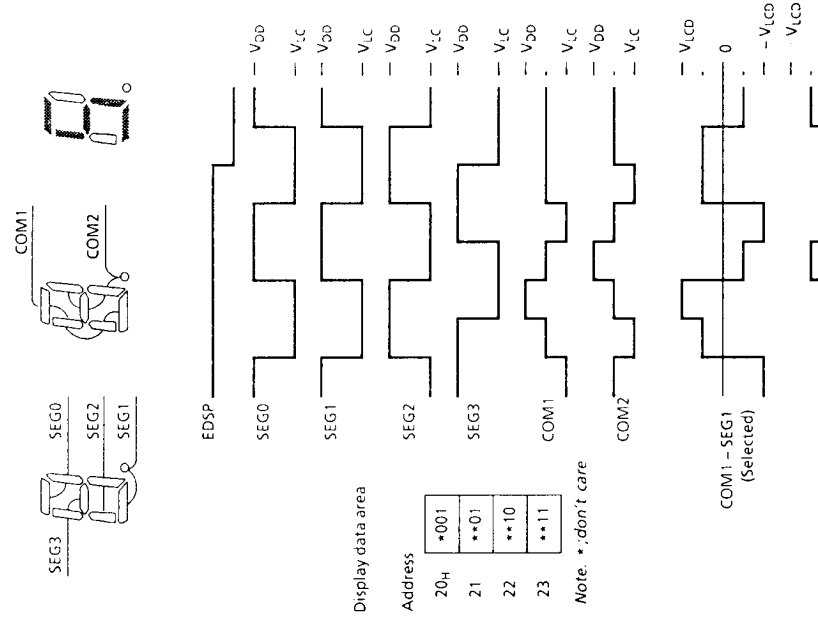


Figure 2-14. 1/2 Duty (1/2 Bias) Drive

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Supply Voltage (LCD drive)	V_{LC}		− 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	℃
Storage Temperature	T_{stg}		− 55 to 125	℃
Operating Temperature	T_{opr}		− 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency (High freq.)	fc	XIN, XOUT		0.4	4.2	MHz
Clock Frequency (Low freq.)	fs	XTIN, XTOUT		30.0	34.0	KHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW mode

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	− 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down resistor		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Segment Output Resistance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} − V_{LC} = 3V	—	20	—	KΩ
Common Output Resistance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS} fc = 4MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3V, V_{LC} = V_{SS} fs = 32.768KHz	—	15	30	μA

Note 1. Typ. values shows those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance R_{OS}, R_{OC} : Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$: Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
$V_{O1/2}$: Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$: Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. Supply Current I_{DD} : V_{IN} = 5.3V/0.2V
The Port K0 is open when the input resistor is contained.
The voltage applied to the Port R is within the valid range.

Note 6. Supply Current I_{DDS} : V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

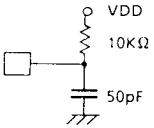
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = −30 to 70°C)

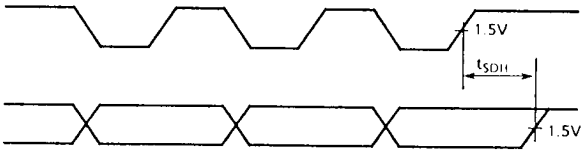
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	1.9	—	20	μs
		In the SLOW mode	235	—	267	μs
High level Clock pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy} - 300$	—	—	ns

Note. Shift Data Hold Time :

External Circuit for $\overline{SCK}$ pin and SO pin



Serial port (Completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = −30 to 70°C)

(1) 4MHz

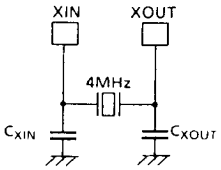
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT} = 30pF$

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30pF$

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT} = 20pF$

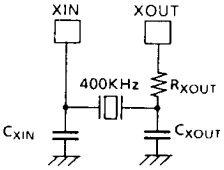


(2) 400KHz

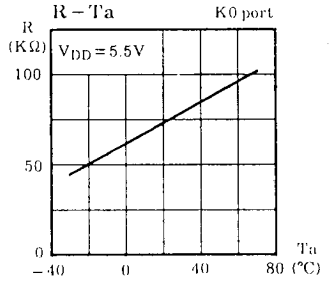
Ceramic Resonator

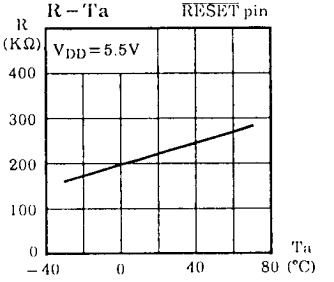
CSB400B (MURATA) $C_{XIN} = C_{XOUT} = 220pF$, $R_{XOUT} = 6.8K\Omega$

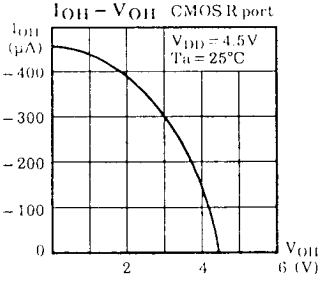
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT} = 100pF$, $R_{XOUT} = 10K\Omega$

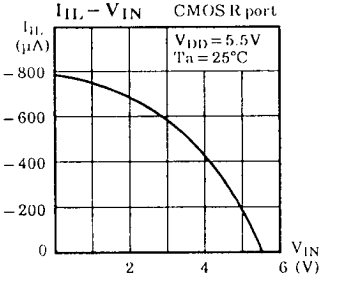


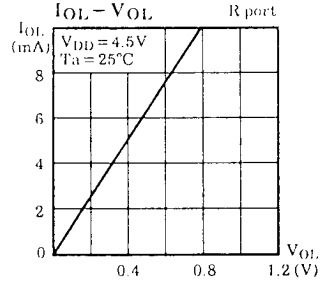
TYPICAL CHARACTERISTICS

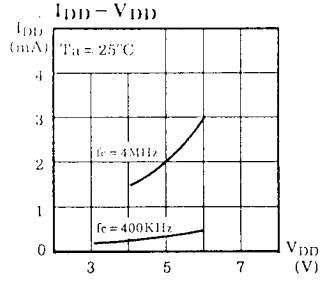


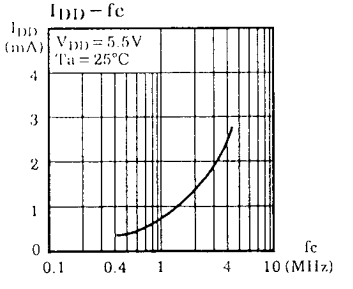








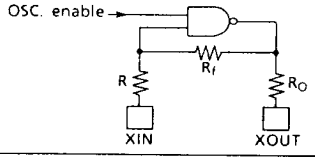
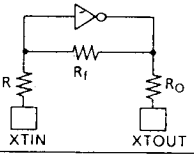
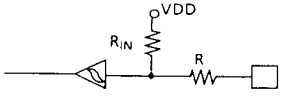
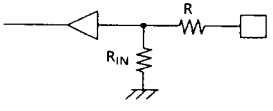




INPUT/OUTPUT CIRCUITRY

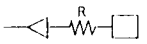
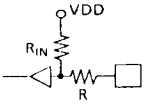
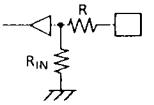
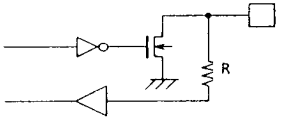
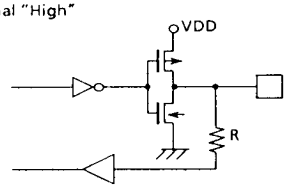
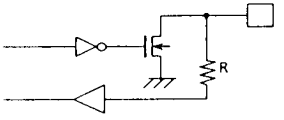
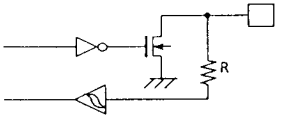
(1) Control pins

Input/Output circuitries of the 47C425A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins (High frequency) R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
XTIN XTOUT	INPUT OUTPUT		Resonator connecting pins (Low frequency) R = 1KΩ (typ.) Rf = 15MΩ (typ.) RO = 200KΩ (typ.)
$\overline{\text{RESET}}$	INPUT		Hysteresis input Pull-up resistor RIN = 220KΩ (typ.) R = 1KΩ (typ.)
TEST	INPUT		Contained pull-down resistor RIN = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O ports

The input/output circuitries of the 47C425A I/O ports shown below, any one of the circuitries can be chosen by a code (GA to GF) as a mask option.

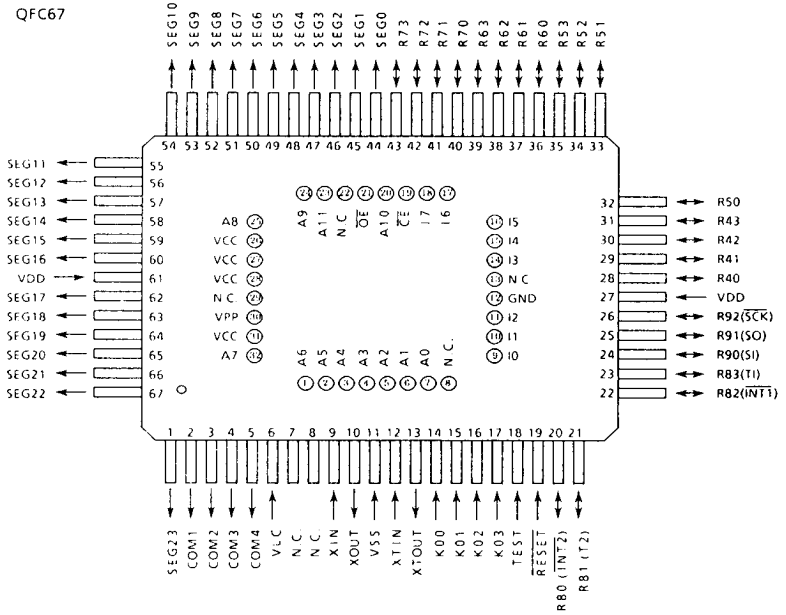
PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		GA, GD	GB, GE	GC, GF	
K0	Input				pull-up/pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
		GA, GB, GC	GD, GE, GF		
R4 R5 R6	I/O	Initial "Hi-Z" 	Initial "High" 		Sink open drain or push-pull output R = 1KΩ (typ.)
R7	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)

CMOS 4-BIT MICROCONTROLLER

TMP47C925AG

The 47C925A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C425A application systems (programs).
The 47C925A is pin compatible with the 47C425A which is mask-programmed ROM device.

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ	Max.	UNIT
Address Delay Time	t_{AD}	VSS = 0V, V_{DD} = 4.5 to 6.0V	—	—	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	—	—	ns
Data Hold Time	t_{IH}	T_{opr} = − 30 to 70°C	50	—	—	ns

NOTES FOR USE

(1) Program memory
The program area is shown in Figure 1.

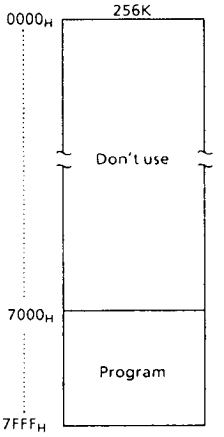


Figure 1. Program area

(2) Data memory
The 47C925A contains 256 × 4-bit data memory.

(3) I/O ports
Input/Output circuitries of the 47C925A I/O ports are similar to the code GA of the 47C425A.
When this chip is used as evaluator with other I/O code (GB-GF), it is necessary to provide the external resistors (Refer to Figure 2).

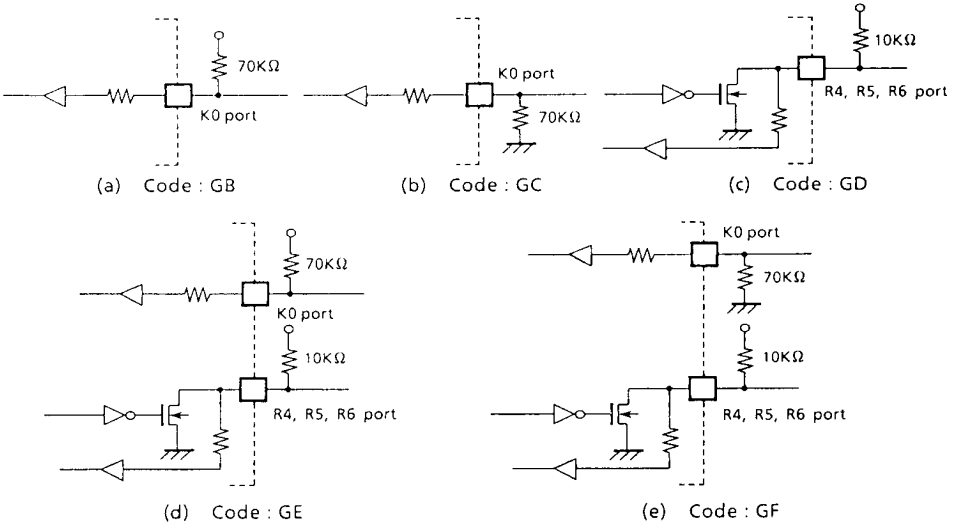


Figure 2. I/O code and external circuitry