

DRAM

4 MEG x 4 DRAM

FAST PAGE MODE: MT4C40004
STATIC COLUMN: MT4C40005

DRAM

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single power supply : +5V±10% or +3.3V±10%
- Low power, 5mW standby; 250mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Refresh modes: \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR), and HIDDEN
- 2048-cycle refresh distributed across 32ms or 4096-cycle refresh distributed across 64ms

OPTIONS

- Timing

50ns access	-5
60ns access	-6
70ns access	-7
80ns access	-8
- Packages

Plastic ZIP (475mil)	Z
Plastic SOJ (400mil)	DJ
Plastic TSOP (*)	TG
- Refresh Period

2048 cycles @ 32ms	R
4096 cycles @ 64ms	None
- Operating Temperature, TA

Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
- Power Supply

+5V±10%	None
+3.3V±10%	V

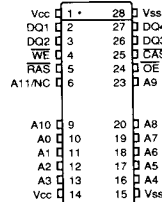
MARKING

GENERAL DESCRIPTION

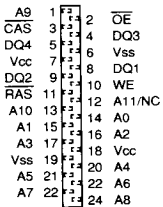
The MT4C40004/5 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 10-12 bits (A0-A11) at a time. \overline{RAS} is used to latch the first 11/12 bits and \overline{CAS} the latter 10/11 bits. A READ or WRITE cycle is selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-7)



24-Pin ZIP



*Consult factory on availability of TSOP packages

pins remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pins, data out (Q), is activated and retains the selected cell data as long as \overline{CAS} remains LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by \overline{WE} and \overline{OE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 -A10/11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR), or HIDDEN refresh) so that all 2048/4096 combinations of \overline{RAS} addresses (A0 -A10/ A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic \overline{RAS} addressing.

The MT4C40004/5 are available with either 2048 cycles or 4096 cycles of refreshing. If CBR refresh is used, the number of cycles is a "don't care."