

8.192 WORD X 8 BIT CMOS STATIC RAM

**DESCRIPTION**

The TC5563APL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE2 is a logical low or CE1 is a logical high, the device is placed in low power standby mode in which standby current is 0.6µA typically. The TC5563APL has three control inputs. Two chip enables (CE1, CE2) allow for device selection and data retention control, and an output enable input (OE) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC5563APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5563APL is offered in a dual-in-line 28 pin standard 300 mil plastic package.

**FEATURES**

- Low Power Dissipation  
27.5mW/MHz (Max.) Operating
- Standby Current: 1µA (Max.) Ta=25°C
- Access Time  
TC5563APL-10L: 100ns (Max.)  
TC5563APL-12L: 120ns (Max.)  
TC5563APL-15L: 150ns (Max.)
- 5V Single Power Supply
- Power Down Features: CE2, CE1
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

| Package Type               | Device Name |
|----------------------------|-------------|
| 600 mil DIP                | *TC5565APL  |
| 300 mil DIP (Slim Package) | TC5563APL   |
| Flat Package (SOP)         | *TC5565APL  |

\*: See TC5565APL/AFL Technical Data.

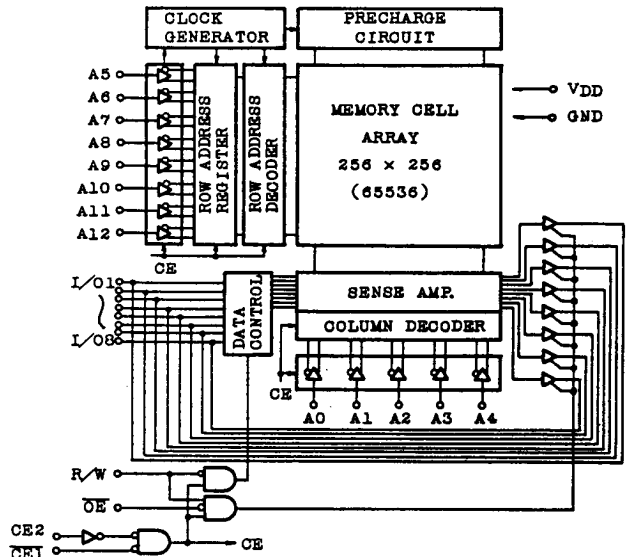
**PIN CONNECTION (TOP VIEW)**

| TC5563APL |    |    |      | 64k bit EPROM<br>TMM2764D |    |    |      |
|-----------|----|----|------|---------------------------|----|----|------|
| N.C.      | 1  | 28 | VDD  | Vpp                       | 1  | 28 | VCC  |
| A12       | 2  | 27 | R/W  | A12                       | 2  | 27 | FGM  |
| A7        | 3  | 26 | CE2  | A7                        | 3  | 26 | N.C. |
| A6        | 4  | 25 | A8   | A6                        | 4  | 25 | A8   |
| A5        | 5  | 24 | A9   | A5                        | 5  | 24 | A9   |
| A4        | 6  | 23 | A11  | A4                        | 6  | 23 | A11  |
| A3        | 7  | 22 | OE   | A3                        | 7  | 22 | OE   |
| A2        | 8  | 21 | A10  | A2                        | 8  | 21 | A10  |
| A1        | 9  | 20 | CE1  | A1                        | 9  | 20 | CE   |
| A0        | 10 | 19 | I/O8 | A0                        | 10 | 19 | 07   |
| I/O1      | 11 | 18 | I/O9 | 00                        | 11 | 18 | 06   |
| I/O2      | 12 | 17 | I/O6 | 01                        | 12 | 17 | 05   |
| I/O3      | 13 | 16 | I/O5 | 02                        | 13 | 16 | 04   |
| GND       | 14 | 15 | I/O4 | GND                       | 14 | 15 | 03   |

**PIN NAMES**

|             |                          |
|-------------|--------------------------|
| A0 ~ A12    | Address Inputs           |
| R/W         | Read/Write Control Input |
| OE          | Output Enable Input      |
| CE1, CE2    | Chip Enable Inputs       |
| I/O1 ~ I/O8 | Data Inputs/Outputs      |
| VDD         | Power (+5V)              |
| GND         | Ground                   |
| N.C.        | No Connection            |

**BLOCK DIAGRAM**



# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## OPERATION MODE

| OPERATION MODE  | $\overline{CE1}$ | CE2 | $\overline{OE}$ | R/W | I/O1 ~ I/O8 | POWER            |
|-----------------|------------------|-----|-----------------|-----|-------------|------------------|
| Read            | L                | H   | L               | H   | DOUT        | I <sub>DDO</sub> |
| Write           | L                | H   | *               | L   | DIN         | I <sub>DDO</sub> |
| Output Deselect | L                | H   | H               | H   | High-Z      | I <sub>DDO</sub> |
| Standby         | H                | *   | *               | *   | High-Z      | I <sub>DDS</sub> |
|                 | *                | L   | *               | *   | High-Z      |                  |

\*: H or L

## MAXIMUM RATINGS

| SYMBOL              | ITEM                     | RATING                      | UNIT     |
|---------------------|--------------------------|-----------------------------|----------|
| V <sub>DD</sub>     | Power Supply Voltage     | -0.3 ~ 7.0                  | V        |
| V <sub>IN</sub>     | Input Voltage            | -0.3* ~ 7.0                 | V        |
| V <sub>I/O</sub>    | Input and Output Voltage | -0.5 ~ V <sub>DD</sub> +0.5 | V        |
| P <sub>D</sub>      | Power Dissipation        | 0.8                         | W        |
| T <sub>solder</sub> | Soldering Temperature    | 260 ± 10                    | °C · sec |
| T <sub>stg</sub>    | Storage Temperature      | -55 ~ 150                   | °C       |
| T <sub>opr</sub>    | Operating Temperature    | 0 ~ 70                      | °C       |

\*: -3.0V at pulse width 50ns Max.

## D.C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL          | PARAMETER                     | MIN.  | TYP. | MAX.                 | UNIT |
|-----------------|-------------------------------|-------|------|----------------------|------|
| V <sub>DD</sub> | Power Supply Voltage          | 4.5   | 5.0  | 5.5                  | V    |
| V <sub>IH</sub> | Input High Voltage            | 2.2   | -    | V <sub>DD</sub> +0.3 |      |
| V <sub>IL</sub> | Input Low Voltage             | -0.3* | -    | 0.8                  |      |
| V <sub>DH</sub> | Data Retention Supply Voltage | 2.0   | -    | 5.5                  |      |

\*: -3.0V at pulse width 50ns Max.

# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

| SYMBOL                 | PARAMETER              | TEST CONDITION   | MIN.                                    | TYP.   | MAX.     | UNIT      |    |
|------------------------|------------------------|--|---|--------|----------|-----------|----|
| IIL                    | Input Leakage Current  | V <sub>IN</sub> =0~V <sub>DD</sub>   | -                                       | -      | ±1.0     | μA        |    |
| IOH                    | Output High Current    | VOH=2.4V   | -1.0                                    | -      | -        | mA        |    |
| IOL                    | Output Low Current     | VOL=0.4V   | 4.0                                     | -      | -        | mA        |    |
| ILO                    | Output Leakage Current | CE1=V <sub>IH</sub> or CE2=V <sub>IL</sub> or<br>R/W=V <sub>IL</sub> or OE=V <sub>IH</sub><br>V <sub>OUT</sub> =0~V <sub>DD</sub>                | -                                       | -      | ±1.0     | μA        |    |
| I <sub>DDO1</sub>      | Operating Current      | V <sub>DD</sub> =5.5V<br>CE1=V <sub>IL</sub><br>CE2=V <sub>IH</sub><br>Other input=<br>V <sub>IH</sub> /V <sub>IL</sub><br>I <sub>OUT</sub> =0mA | t <sub>cycle</sub> =1.0μs               | -      | -        | 10        | mA |
|                        |                        |  | TC5563APL-10L t <sub>cycle</sub> =100ns | -      | -        | 45        | mA |
|                        |                        |  | TC5563APL-12L t <sub>cycle</sub> =120ns | -      | -        | 40        | mA |
|                        |                        |  | TC5563APL-15L t <sub>cycle</sub> =150ns | -      | -        | 35        | mA |
| I <sub>DDO2</sub>      | Operating Current      | V <sub>DD</sub> =5.5V<br>CE1=0.2V<br>CE2=V <sub>DD</sub> -0.2V<br>Other input=<br>V <sub>DD</sub> -0.2V/0.2V<br>I <sub>OUT</sub> =0mA            | t <sub>cycle</sub> =1.0μs               | -      | -        | 5         | mA |
|                        |                        |  | TC5563APL-10L t <sub>cycle</sub> =100ns | -      | -        | 40        | mA |
|                        |                        |  | TC5563APL-12L t <sub>cycle</sub> =120ns | -      | -        | 35        | mA |
|                        |                        |  | TC5563APL-15L t <sub>cycle</sub> =150ns | -      | -        | 30        | mA |
| I <sub>DDO1</sub>      | Standby Current        | CE1=V <sub>IH</sub> or CE2=V <sub>IL</sub>   | -                                       | -      | 3        | mA        |    |
| *<br>I <sub>DDO2</sub> | Standby Current        | CE1=V <sub>DD</sub> -0.2V<br>or CE2=0.2V   | Ta=25°C<br>Ta=0~70°C                    | -<br>- | 0.6<br>- | 1.0<br>30 | μA |

\*: In standby mode with CE1 ≥ V<sub>DD</sub>-0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V<sub>DD</sub>-0.2V or CE2 ≤ 0.2V.

### CAPACITANCE (Ta=25°C)

| SYMBOL           | PARAMETER          | TEST CONDITION        | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> =GND  | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> =GND | 10   |      |

Note: This parameter is periodically sampled and is not 100% tested.

# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

A.C. CHARACTERISTICS ( $T_a=0\sim 70^\circ\text{C}$ ,  $V_{DD}=5V\pm 10\%$ )

## READ CYCLE

| SYMBOL    | PARAMETER                                  | TC5563APL-10L |      | TC5563APL-12L |      | TC5563APL-15L |      | UNIT |
|-----------|--|---------------|------|---------------|------|---------------|------|------|
|           |  | MIN.          | MAX. | MIN.          | MAX. | MIN.          | MAX. |      |
| $t_{RC}$  | Read Cycle Time                            | 100           | -    | 120           | -    | 150           | -    | ns   |
| $t_{ACC}$ | Address Access Time                        | -             | 100  | -             | 120  | -             | 150  |      |
| $t_{CO1}$ | CE1 Access Time                            | -             | 100  | -             | 120  | -             | 150  |      |
| $t_{CO2}$ | CE2 Access Time                            | -             | 100  | -             | 120  | -             | 150  |      |
| $t_{OE}$  | Output Enable to Output Valid              | -             | 50   | -             | 60   | -             | 70   |      |
| $t_{COE}$ | Chip Enable (CE1, CE2) to Output in Low-Z  | 10            | -    | 10            | -    | 15            | -    |      |
| $t_{OEE}$ | Output Enable to Output in Low-Z           | 5             | -    | 5             | -    | 5             | -    |      |
| $t_{OD}$  | Chip Enable (CE1, CE2) to Output in High-Z | -             | 35   | -             | 40   | -             | 50   |      |
| $t_{ODO}$ | Output Enable to Output in High-Z          | -             | 35   | -             | 40   | -             | 50   |      |
| $t_{OH}$  | Output Data Hold Time                      | 20            | -    | 20            | -    | 20            | -    |      |

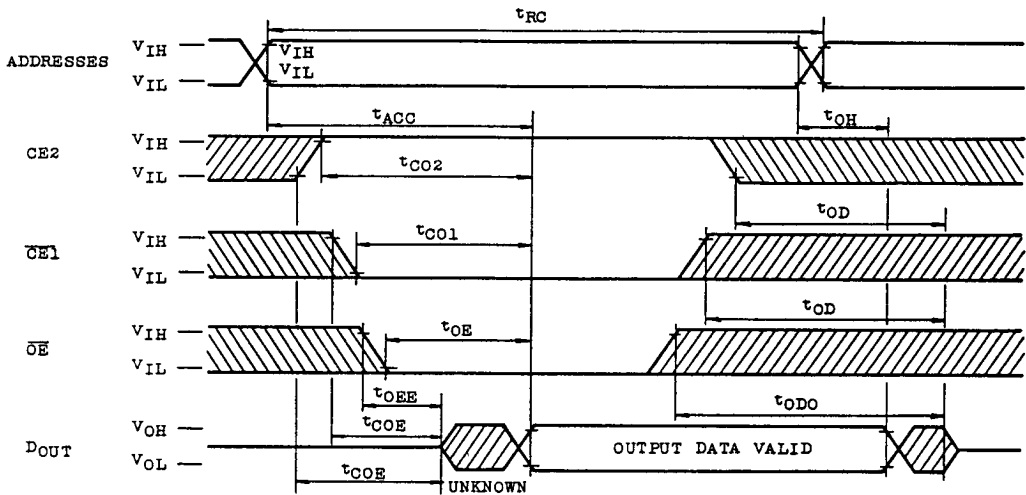
## WRITE CYCLE

| SYMBOL    | PARAMETER                      | TC5563APL-10L |      | TC5563APL-12L |      | TC5563APL-15L |      | UNIT |
|-----------|--------------------------------|---------------|------|---------------|------|---------------|------|------|
|           |                                | MIN.          | MAX. | MIN.          | MAX. | MIN.          | MAX. |      |
| $t_{WC}$  | Write Cycle Time               | 100           | -    | 100           | -    | 150           | -    | ns   |
| $t_{WP}$  | Write Pulse Width              | 60            | -    | 70            | -    | 90            | -    |      |
| $t_{CW}$  | Chip Selection to End of Write | 80            | -    | 85            | -    | 100           | -    |      |
| $t_{AS}$  | Address Set up Time            | 0             | -    | 0             | -    | 0             | -    |      |
| $t_{WR}$  | Write Recovery Time            | 0             | -    | 0             | -    | 0             | -    |      |
| $t_{ODW}$ | R/W to Output High-Z           | -             | 35   | -             | 40   | -             | 50   |      |
| $t_{OEW}$ | R/W to Output Low-Z            | 5             | -    | 5             | -    | 5             | -    |      |
| $t_{DS}$  | Data Set up Time               | 40            | -    | 50            | -    | 60            | -    |      |
| $t_{DH}$  | Data Hold Time                 | 0             | -    | 0             | -    | 0             | -    |      |

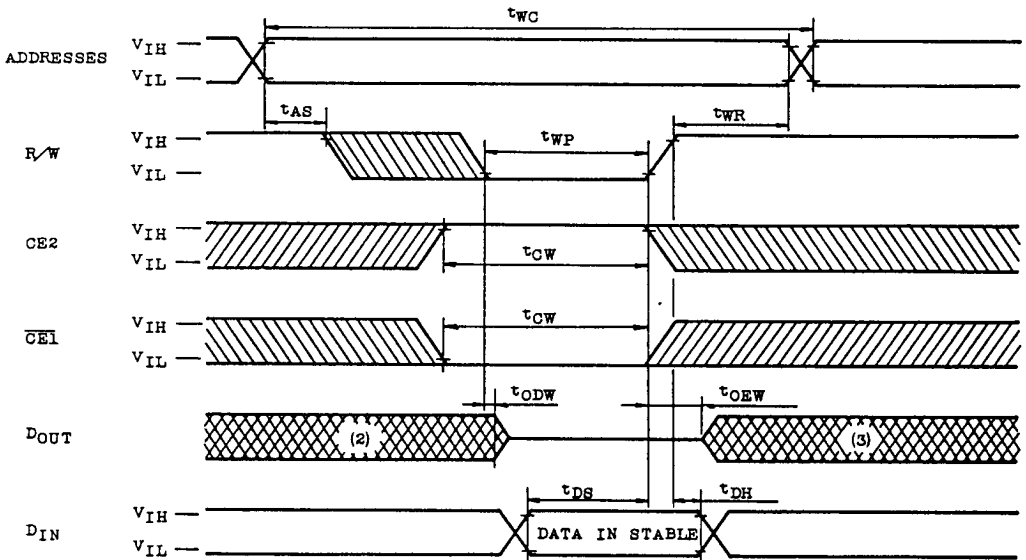
## A.C. TEST CONDITION

Output Load : 100pF + 1 TTL Gate  
 Input Pulse Level : 0.6V, 2.4V  
 Timing Measurement  $V_{IN}$  : 0.8V, 2.2V  
 Reference Level  $V_{OUT}$  : 0.8V, 2.2V  
 $t_r, t_f$  : 5ns

TIMING WAVEFORMS  
READ CYCLE (1)

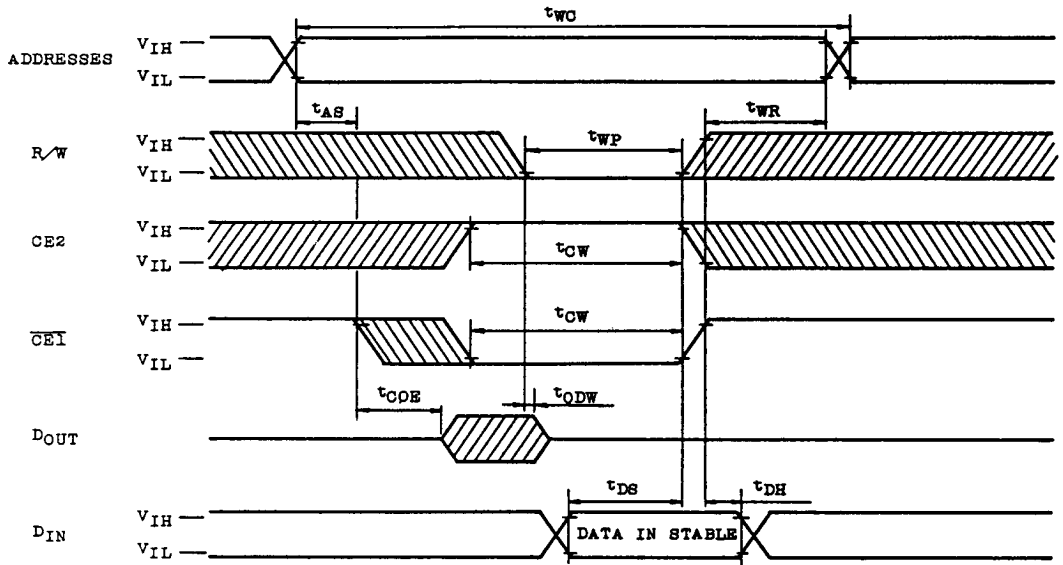


WRITE CYCLE 1 (4) (R/W Controlled Write)

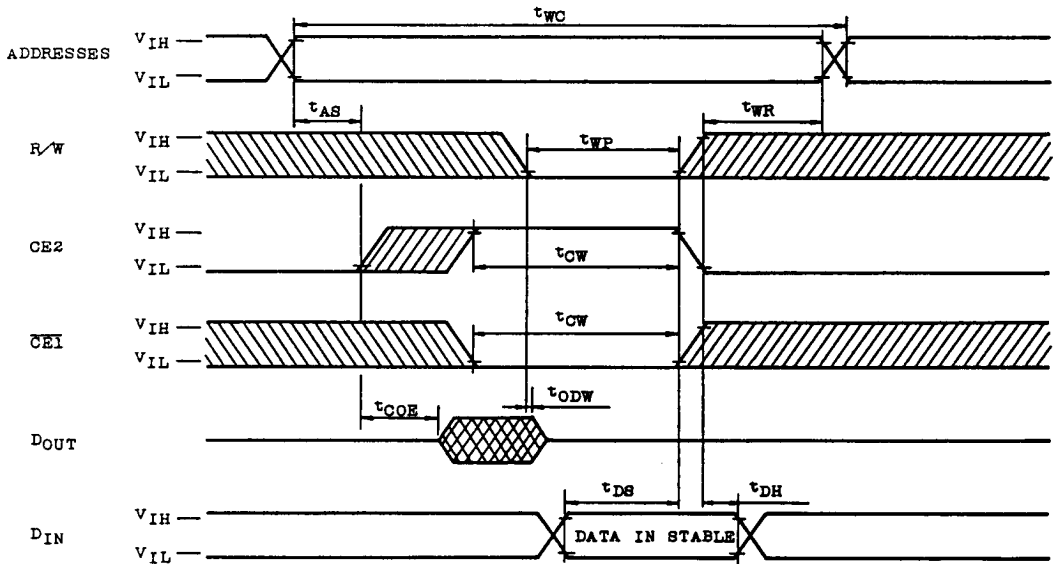


TC5563APL-10L, TC5563APL-12L  
 TC5563APL-15L

WRITE CYCLE 2 (4) ( $\overline{\text{CE1}}$  Controlled Write)



WRITE CYCLE 3 (4) ( $\text{CE2}$  Controlled Write)



Note 1. R/W is High for Read Cycle.

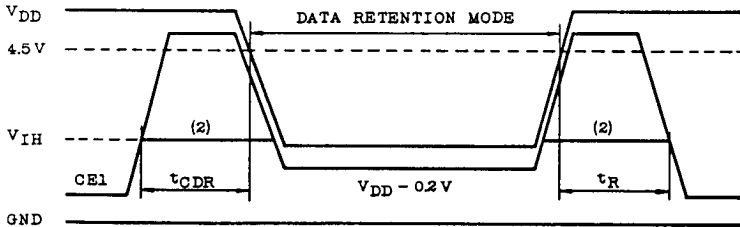
2. Assuming that  $\overline{CE1}$  Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE1}$  High transition or CE2 Low transition occur coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ~ 70°C)

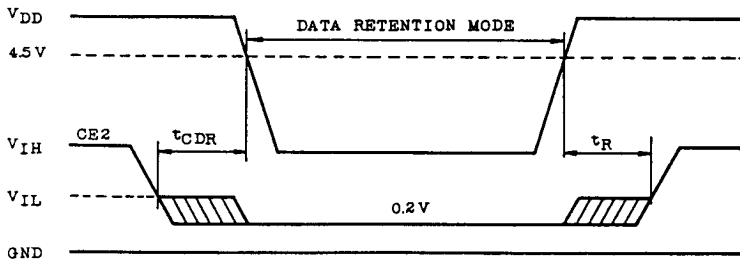
| SYMBOL           | PARAMETER                               | MIN.                  | TYP. | MAX. | UNIT |
|------------------|---|-----------------------|------|------|------|
| V <sub>DH</sub>  | Data Retention Supply Voltage           | 2.0                   | -    | 5.5  | V    |
| I <sub>DD2</sub> | Standby Supply Current                  | V <sub>DD</sub> =3.0V | -    | 15   | μA   |
|                  |   | V <sub>DD</sub> =5.5V | -    | 30   |      |
| t <sub>CDR</sub> | Chip Deselection to Data Retention Mode | 0                     | -    | -    | μs   |
| t <sub>R</sub>   | Recovery Time                           | t <sub>R</sub> C*     | -    | -    | μs   |

\*: Read cycle time.

$\overline{CE1}$  Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

- Note 1: In  $\overline{CE1}$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE2 \leq 0.2V$  or  $CE2 \geq V_{DD}-0.2V$ .
- 2: If the  $V_{IH}$  of  $\overline{CE1}$  is 2.2V in active operation,  $I_{DDS1}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.4V.
- 3: In  $CE2$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE2 \leq 0.2V$ .

## DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on  $V_{DD}/GND$  lines. Thus the use of about 0.1 $\mu$ F decoupling capacitor for every device is recommended to eliminate such noise.

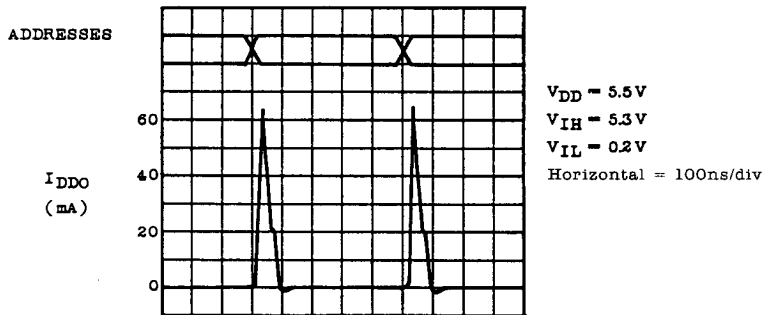
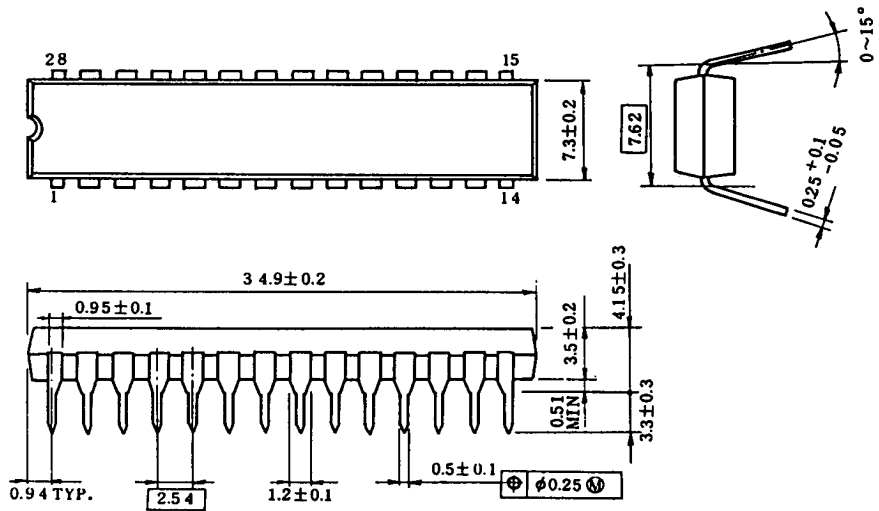


Fig. Typical Current Waveforms



OUTLINE DRAWINGS (DIP28-P-300B)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.