Signetics

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FAST Products	

FAST 74F1760 4-Way Latched Address Multiplexer

T-66-21-57

FEATURES

- Consists of 10 bit wide 4-1 multiplexer
- Separate address latch input for each channel
- 3-state address outputs
- Designed for address multiplexing of dynamic RAMs and other applications

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1760	5.5ns	55 mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A=0°C to 70°C
64-Pin Plastic DIP	74F1760N
68-Pin PLCC	74F1760A

PRODUCT DESCRIPTION

The 'F1760 is a 10 bit wide 4-1 multiplexer. Each 10-bit channel has a separate address latch enable pin thus eliminating the need for external address latches. The 'F1760 has a common pair of Select (SEL_0, SEL_1) inputs to select between channels and a common Output Enable ($\overline{OE}$) pin to control the 3-State outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
B_0-B_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
C_0-C_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
D_0-D_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
SEL_0-SEL_1	Select Inputs	1.0/1.0	20 µA/0.6 mA
ALE_A	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
ALE_B	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
ALE_C	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
ALE_D	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
$\overline{OE}$	Output Enable Input	1.0/1.0	20 µA/0.6 mA
Q_0-Q_9	Address Outputs	N/A	15 mA/24 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.

4-Way Latched Address Multiplexer

FAST 74F1760

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PIN CONFIGURATION

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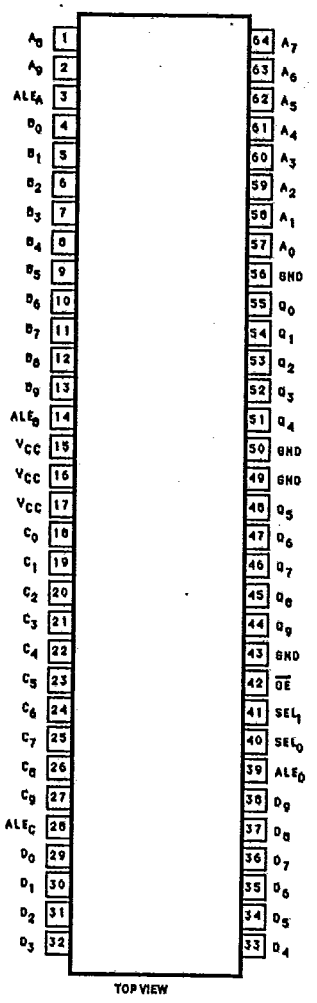
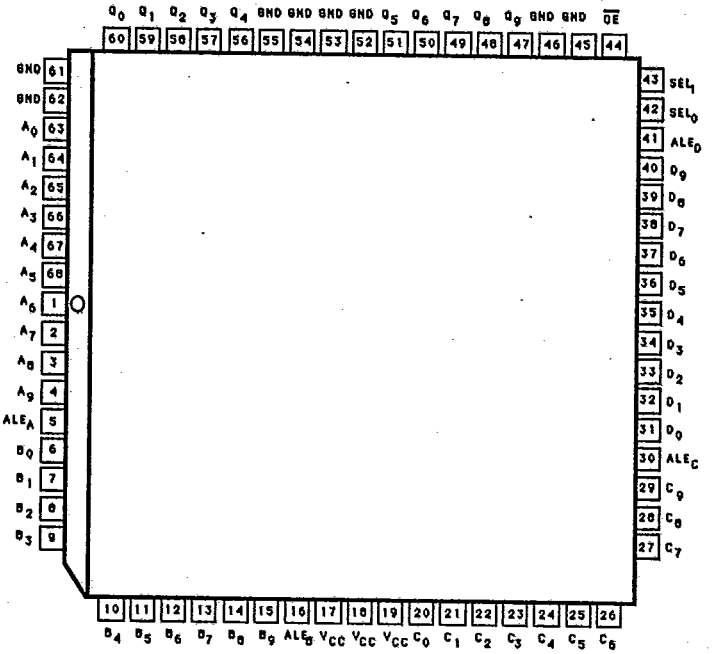
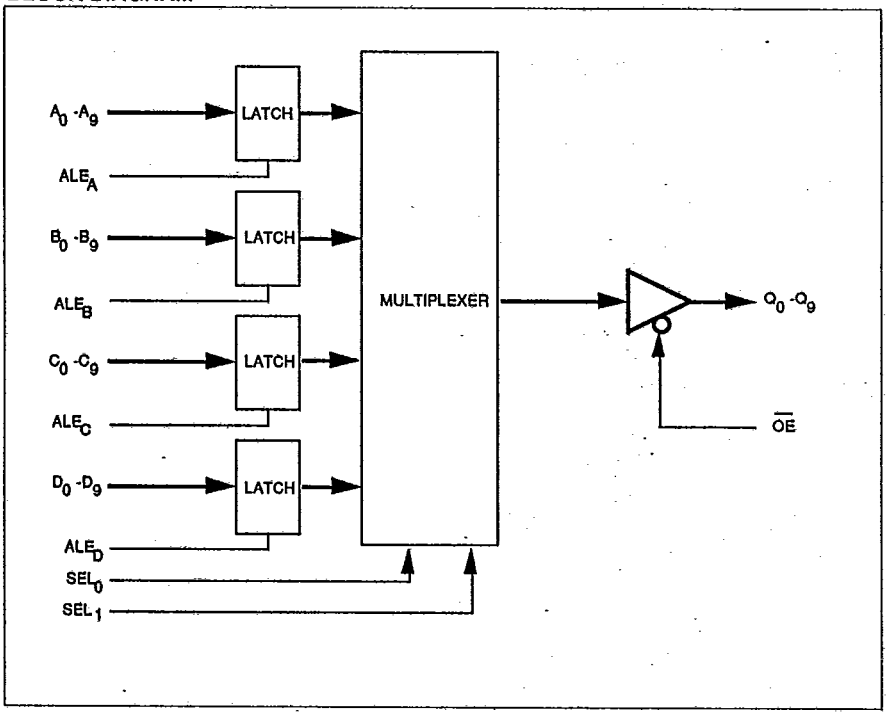




PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_0-A_9	57-64, 1-2	63-68, 1-4	Inputs	Address inputs
B_0-B_9	4-13	6-15	Inputs	Address inputs
C_0-C_9	18-27	20-29	Inputs	Address inputs
D_0-D_9	29-38	31-40	Inputs	Address inputs
ALE_A	3	5	Input	Address Latch Enable for A_0-A_9
ALE_B	14	16	Input	Address Latch Enable for B_0-B_9
ALE_C	28	30	Input	Address Latch Enable for C_0-C_9
ALE_D	39	41	Input	Address Latch Enable for D_0-D_9
SEL_0	40	42	Input	Select input
SEL_1	41	43	Input	Select input
$\overline{OE}$	42	44	Input	Output Enable input
Q_9-Q_0	44-48, 51-55	47-51, 56-60	Outputs	Address outputs

BLOCK DIAGRAM



FUNCTION TABLE

A_0-A_9	ALE_A	B_0-B_9	ALE_B	C_0-C_9	ALE_C	D_0-D_9	ALE_D	SEL_0	SEL_1	Q_0-Q_9	$\overline{OE}$	COMMENTS
XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	Hi-Z	High	Outputs 3-stated
a_0-a_9	↓	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	A-inputs latched into latch A
a_0-a_9	Note	XX	XX	XX	XX	XX	XX	Low	Low	a_0-a_9	Low	a_0-a_9 appear on Y_0-Y_9 outputs
XX	XX	b_0-b_9	↓	XX	XX	XX	XX	XX	XX	XX	XX	B-inputs latched into latch B
XX	XX	b_0-b_9	Note	XX	XX	XX	XX	High	Low	b_0-b_9	Low	b_0-b_9 appear on Y_0-Y_9 outputs
XX	XX	XX	XX	c_0-c_9	↓	XX	XX	XX	XX	XX	XX	C-inputs latched into latch C
XX	XX	XX	XX	c_0-c_9	Note	XX	XX	Low	High	c_0-c_9	Low	c_0-c_9 appear on Y_0-Y_9 outputs
XX	XX	XX	XX	XX	XX	d_0-d_9	↓	XX	XX	XX	XX	D-inputs latched into latch A
XX	XX	XX	XX	XX	XX	d_0-d_9	Note	High	High	d_0-d_9	Low	d_0-d_9 appear on Y_0-Y_9 outputs

NOTE:
ALE_n may be High (transparent mode) or Low (if data has been latched previously by a High to Low transition on ALE_n.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current[1]			-15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transcient currents will exceed these values in actual operation

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±10%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current[5]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX				55	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{os}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.

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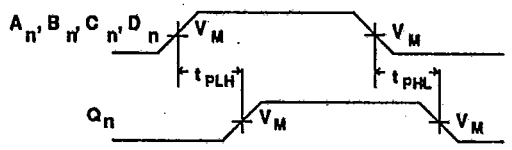
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n, D_n to Q_n	Waveform 1	4.0 4.0	4.5 4.5	8.0 8.0	4.0 4.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL_n to Q_n	Waveform 2	4.0 4.0	5.5 4.5	8.0 8.0	4.0 4.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	2.0 4.0	3.0 5.0	4.0 7.0	2.0 4.0	4.0 7.0	ns
t_{PZH} t_{PZL}	Output Disable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	2.0 2.0	3.0 3.5	4.0 5.5	2.0 2.0	4.0 5.5	ns

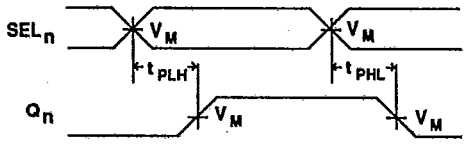
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L =300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L =300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n, C_n, D_n to ALE_n	Waveform 3	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n, C_n, D_n to ALE_n	Waveform 3	2.0 2.0			2.0 2.0		ns

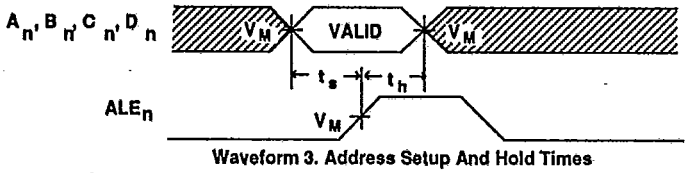
AC WAVEFORMS



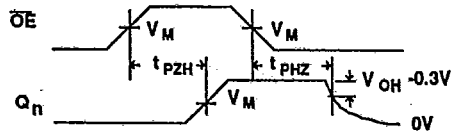
Waveform 1. Propagation Delay, Address Input to Output



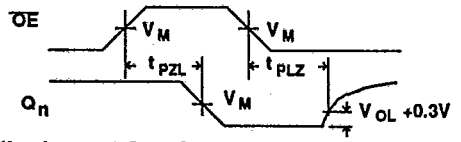
Waveform 2. Propagation Delay, SEL_n Inputs to Address Outputs



Waveform 3. Address Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

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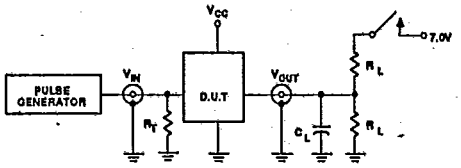


Test Circuit For 3-State Outputs

SWITCH POSITION

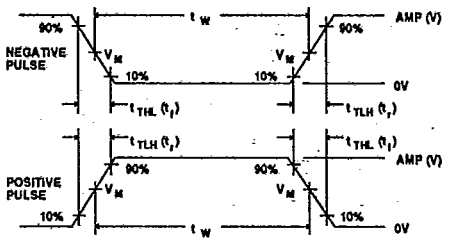
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns