Field-programmable microcontroller peripheral PSD303

T-49-19-63

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{BHE}$ pin for byte select in 16-bit mode
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1 M bit of UV EPROM
  - — Configurable as 128K x 8 or as 64K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8 or 8K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD303 and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLCC and CLCC
- ❑ Simple Menu-Driven Software: Configure the PSD303 on an IBM PC
- ❑ Pin and Function Compatible with the PSD301 and PSD302

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

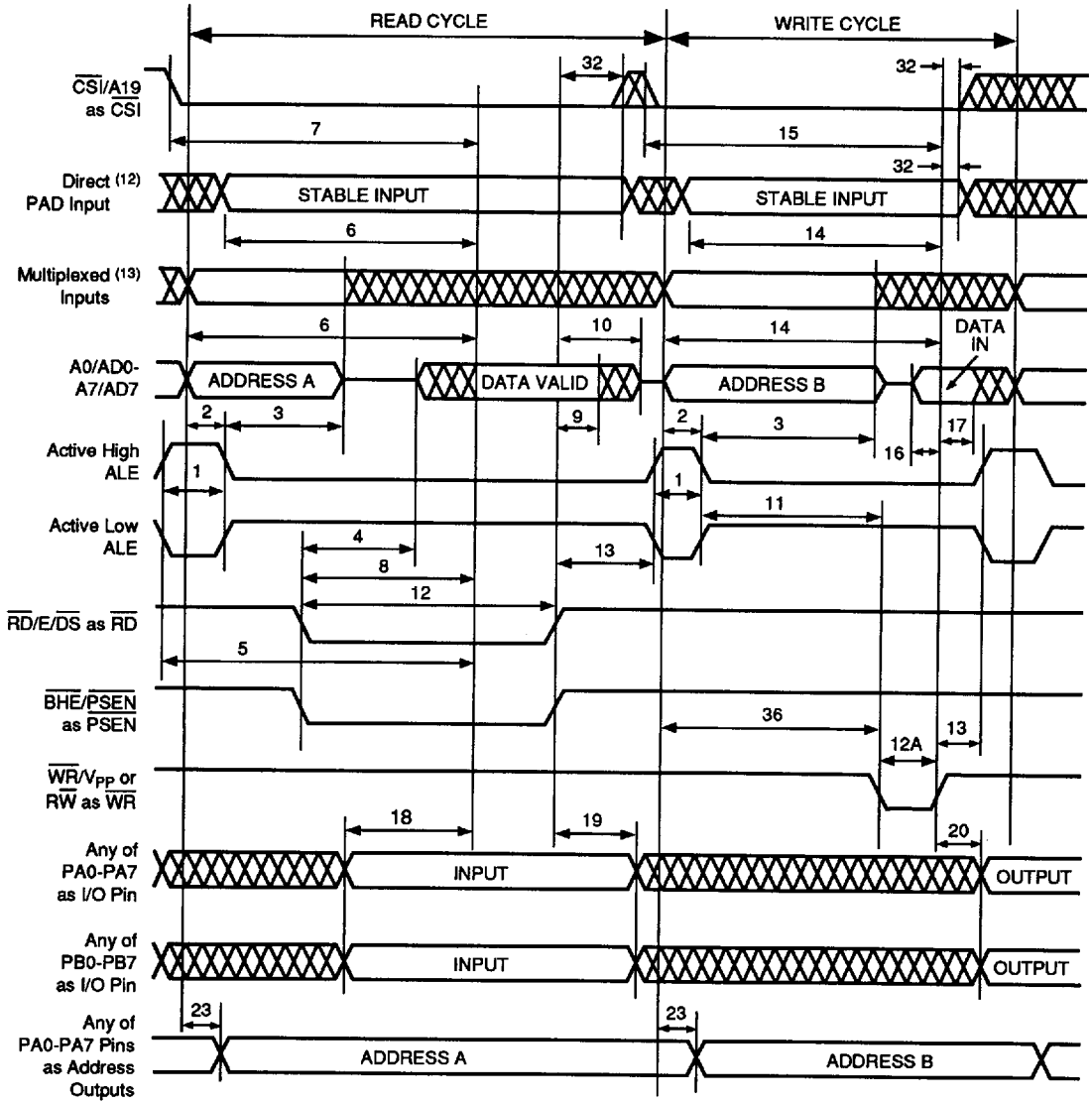
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		9		12		15		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		130		160		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		130		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		32		32		35		40	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		35		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		30		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	50	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	50	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		20		30		40		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

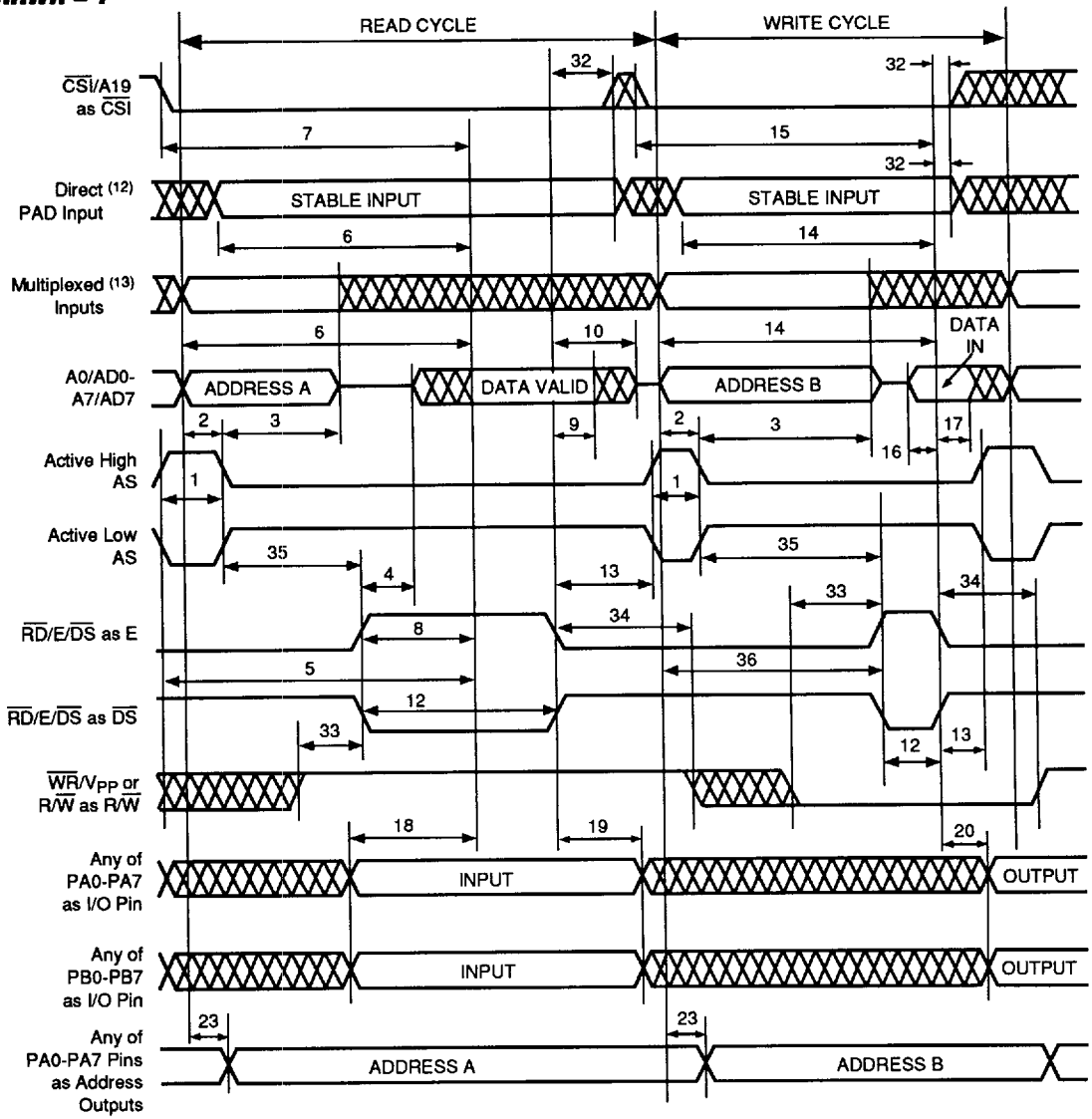
NOTES:
8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



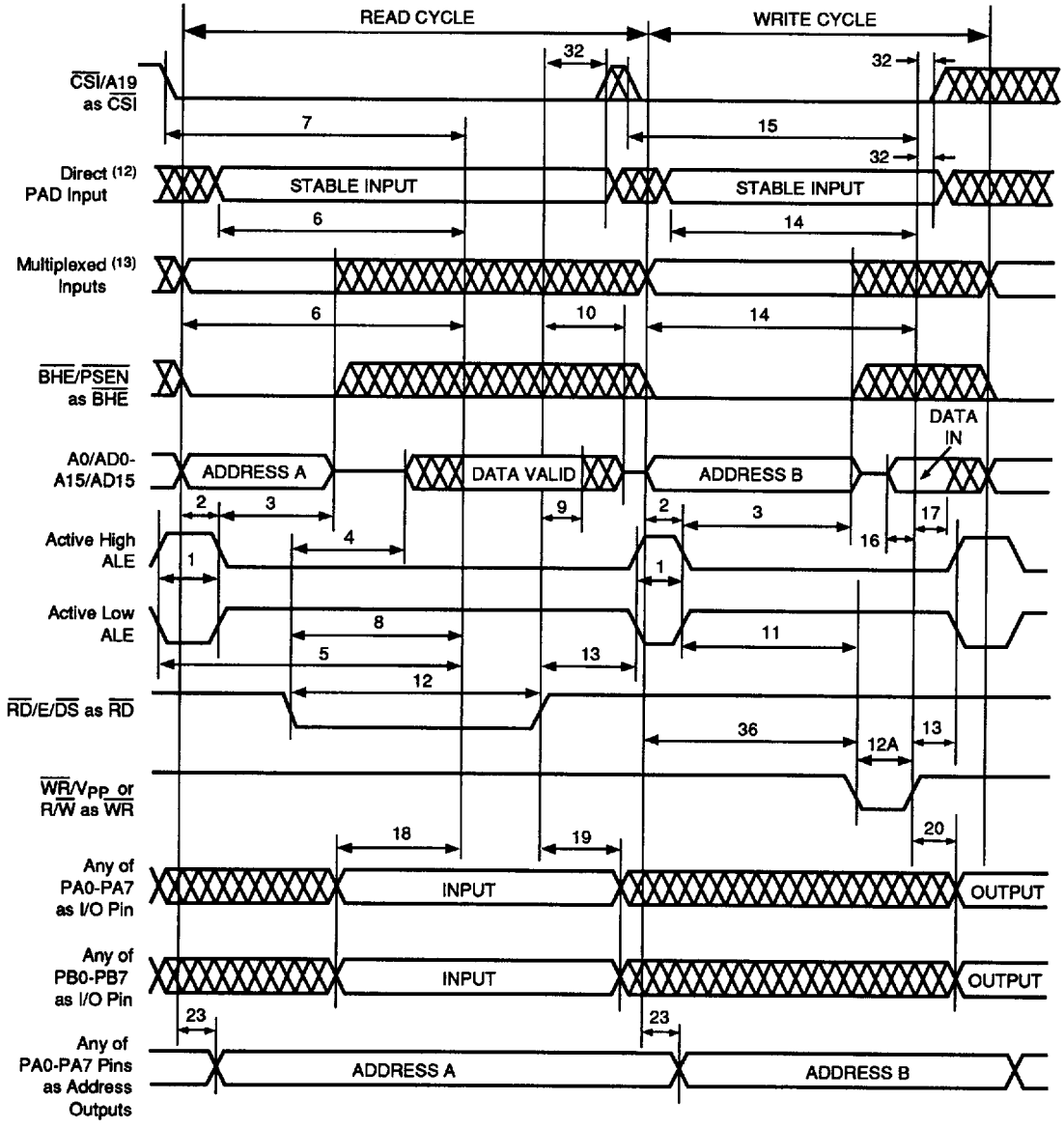
See referenced notes on page 128.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



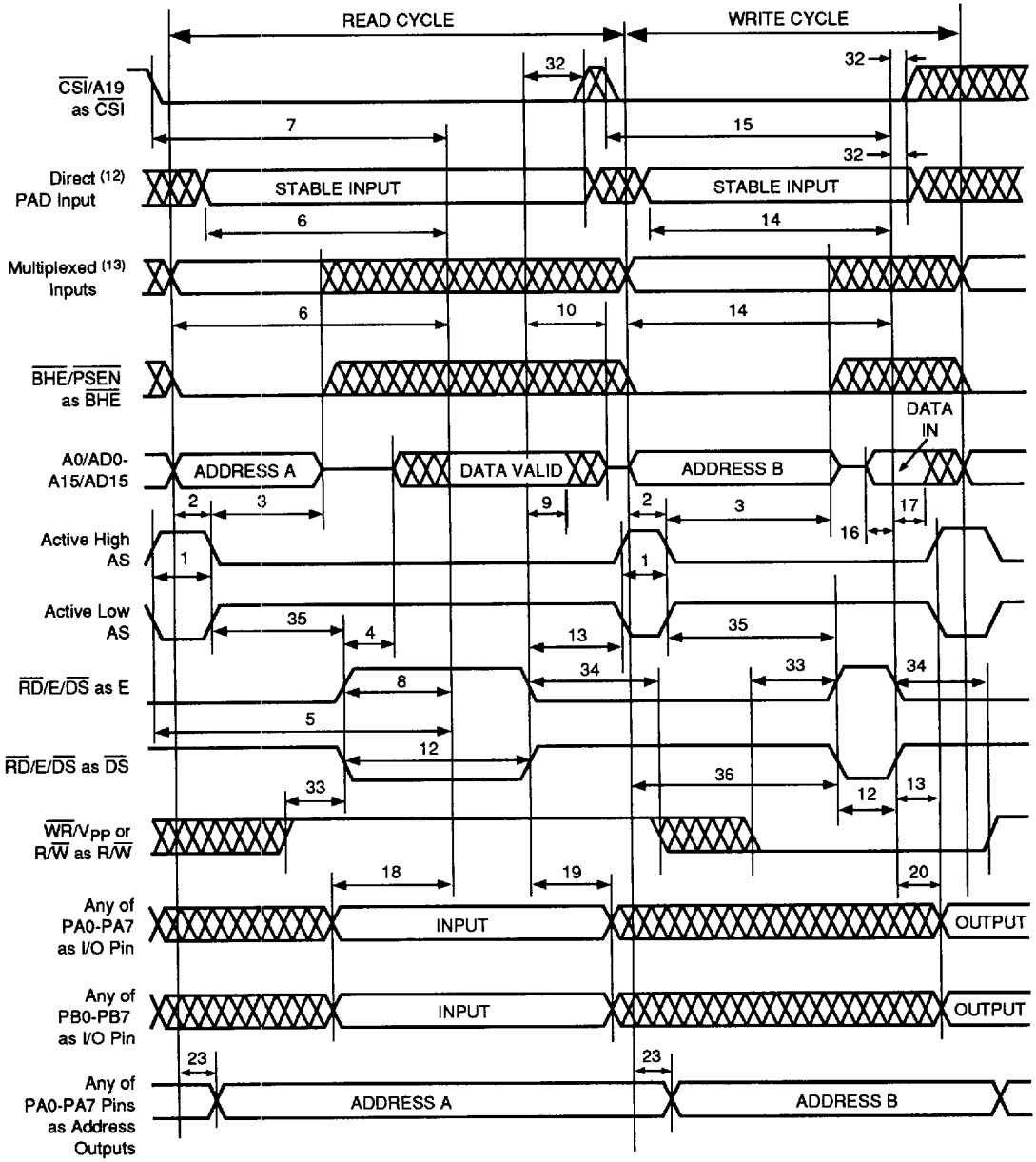
See referenced notes on page 128.

Figure 3. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 0



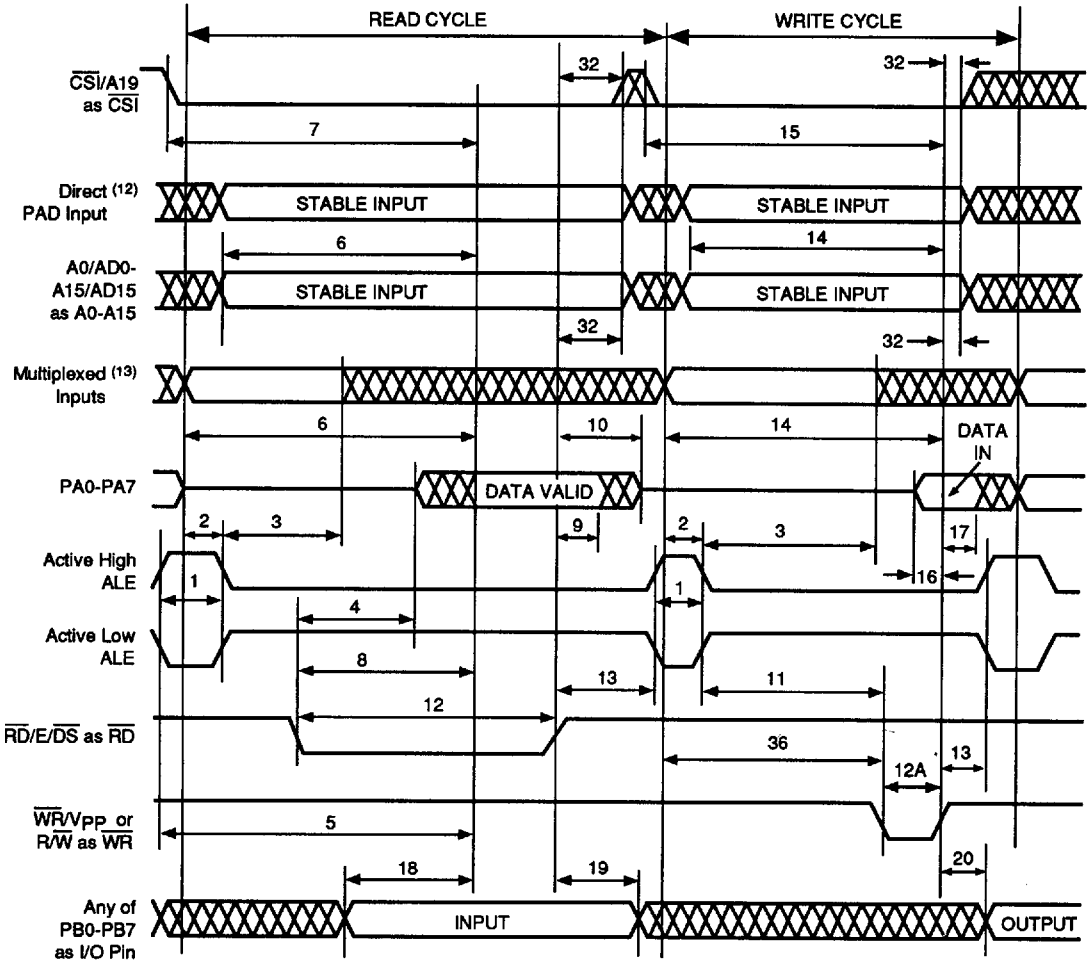
See referenced notes on page 128.

Figure 4. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 1



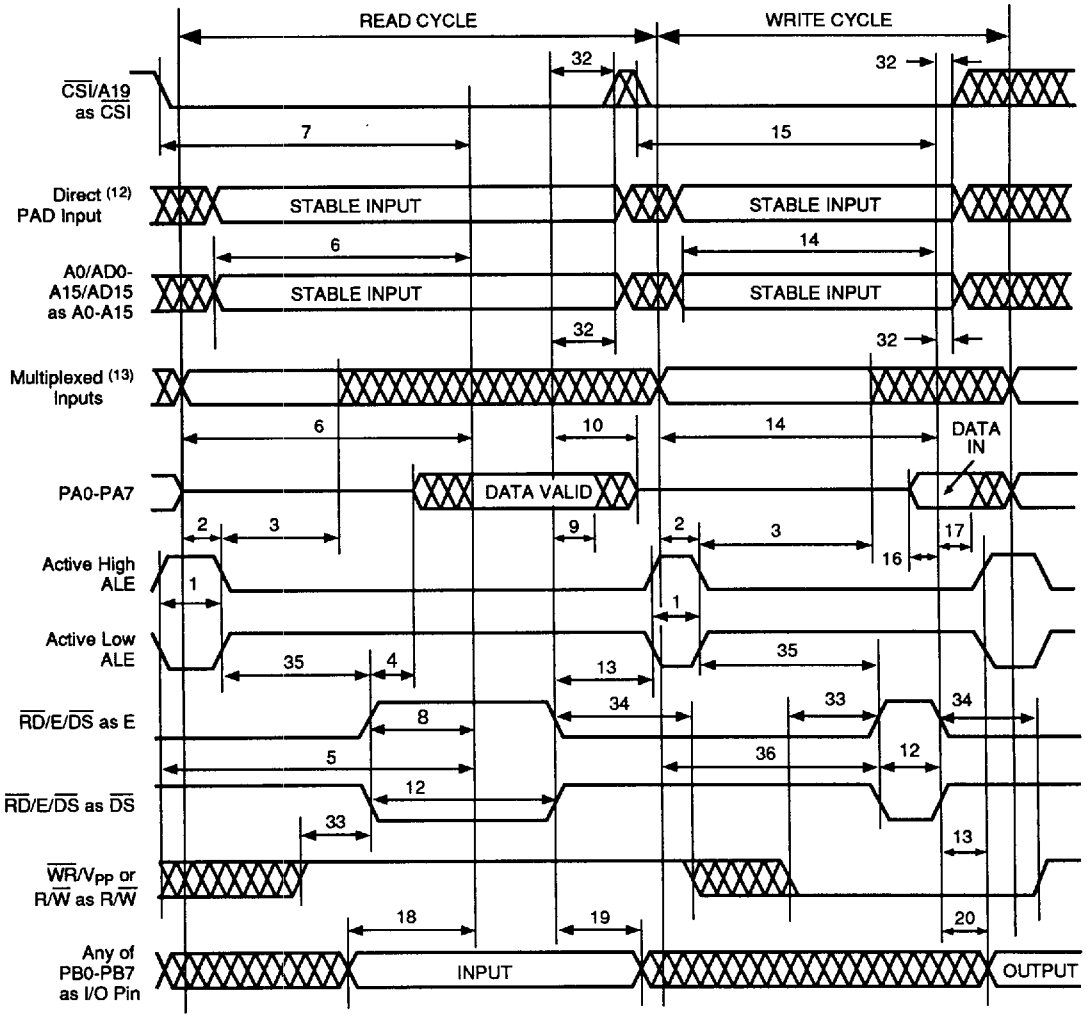
See referenced notes on page 128.

Figure 5. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



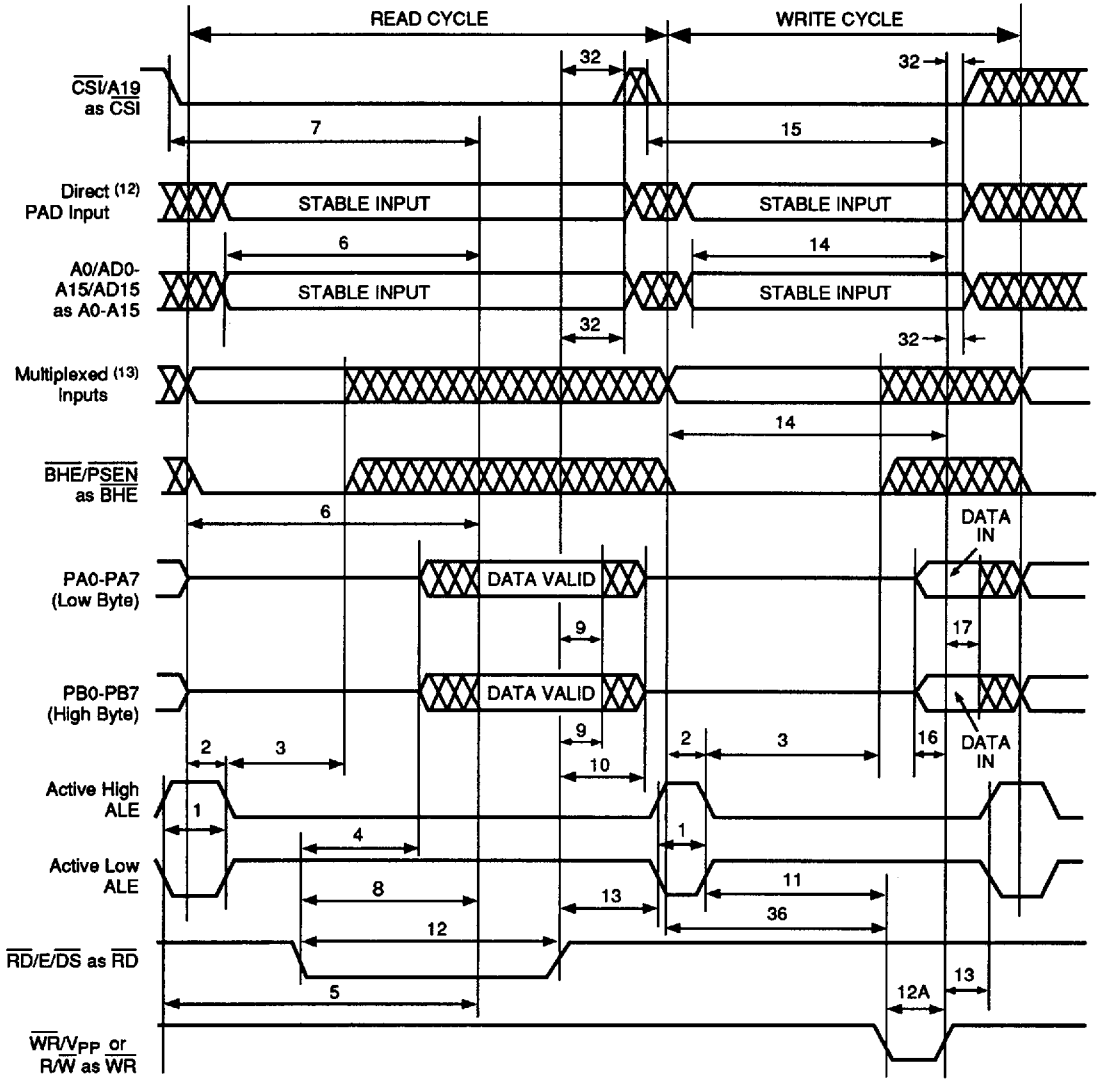
See referenced notes on page 128.

Figure 6. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



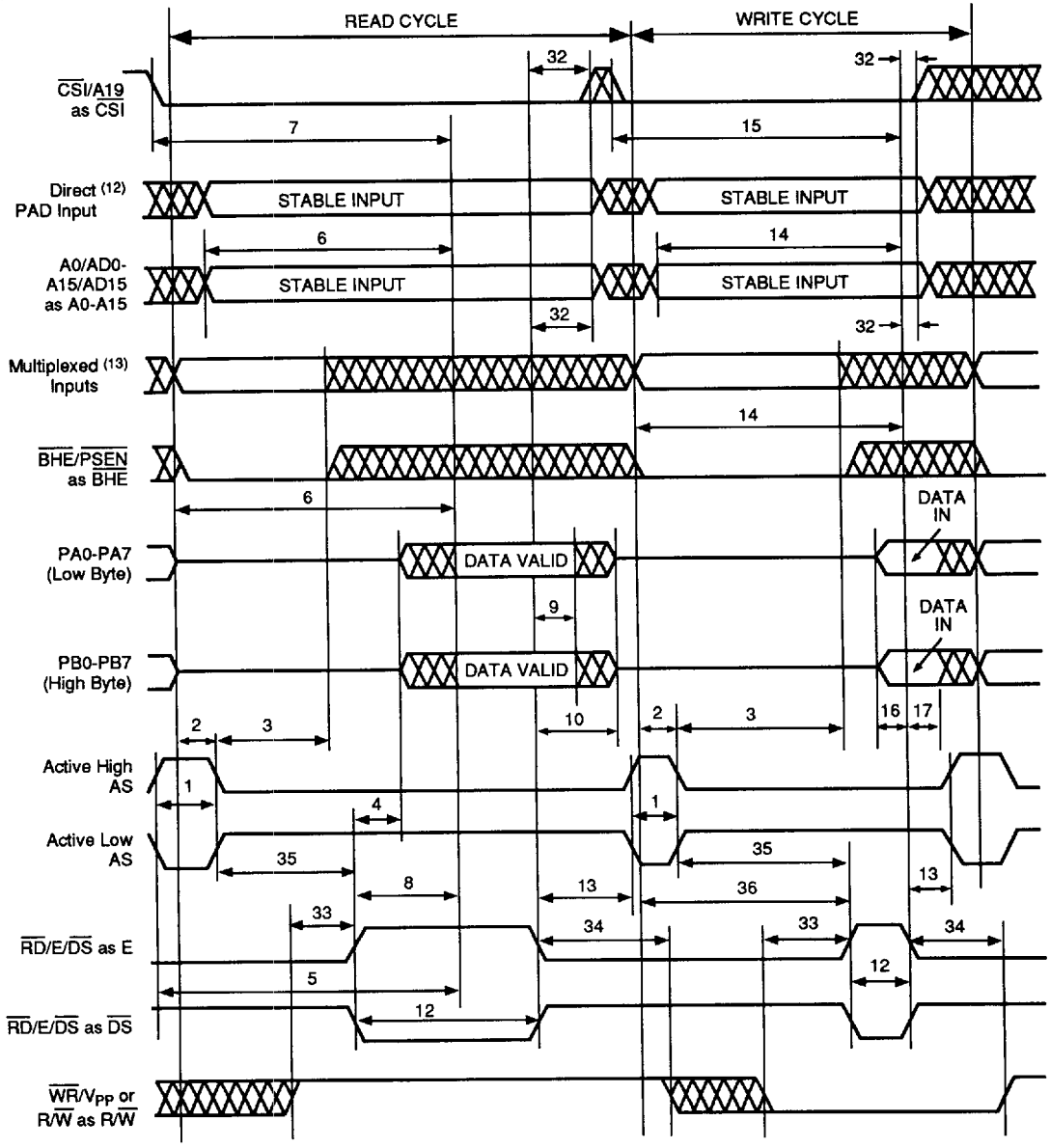
See referenced notes on page 128.

Figure 7. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 0



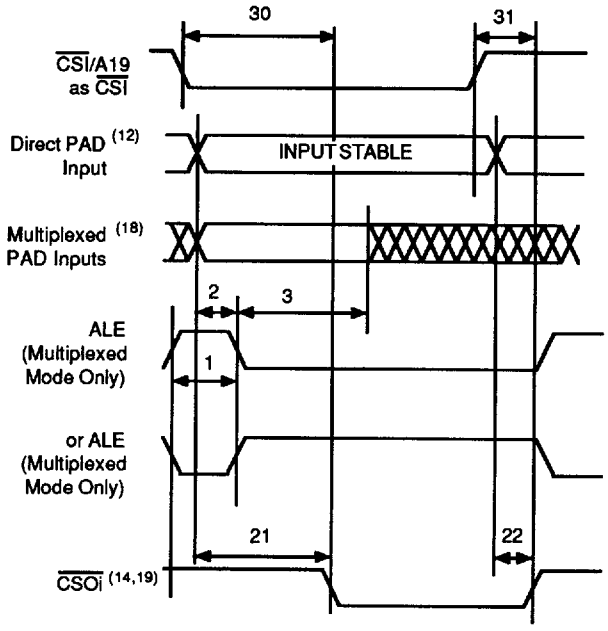
See referenced notes on page 128.

Figure 8. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 1



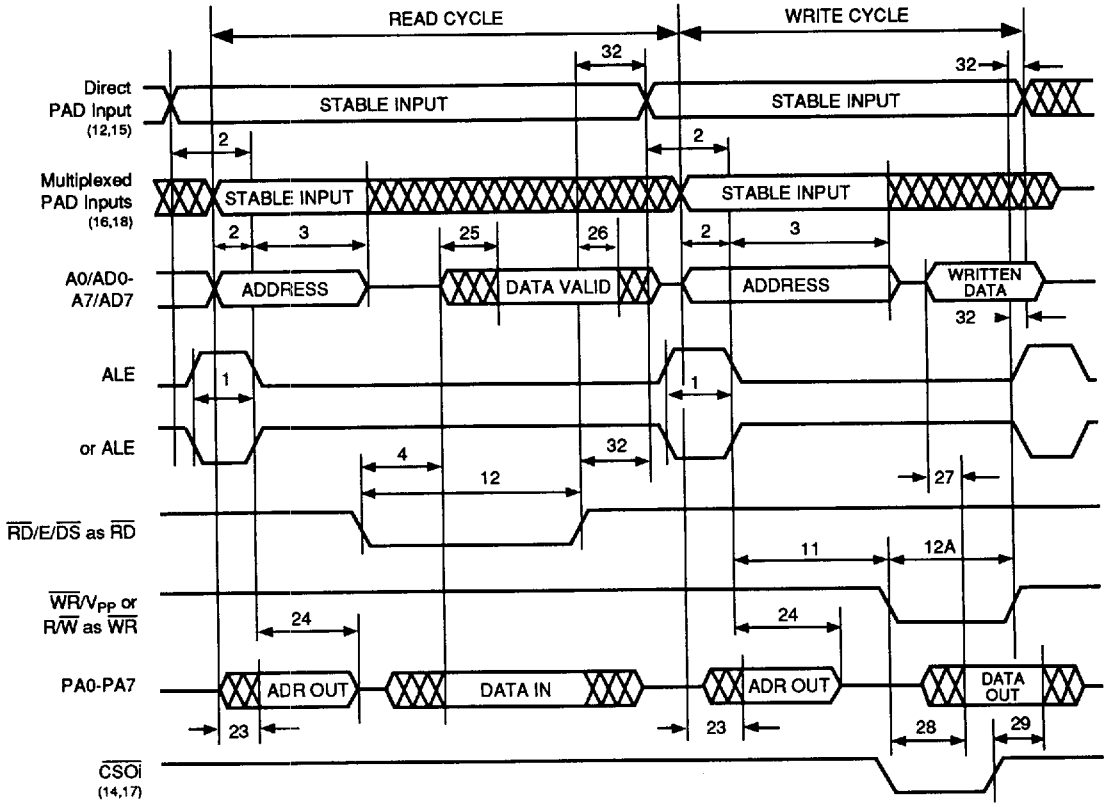
See referenced notes on page 128.

Figure 9. Chip-Select Output Timing



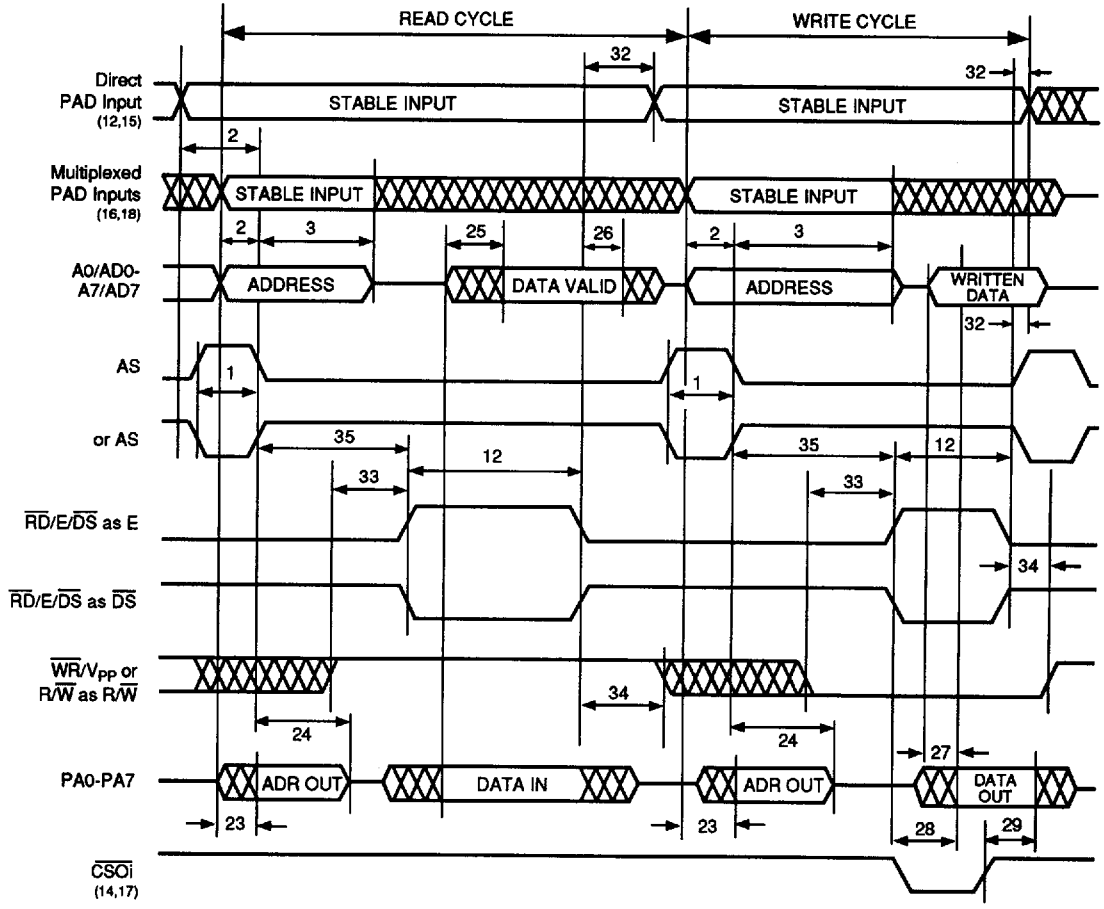
See referenced notes on page 128.

Figure 10. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 128.

Figure 11. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the CSOi expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. CSOi product terms can include any of the PAD input signals except for reset and CSI.

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Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 12. AC Testing Input/Output Waveform

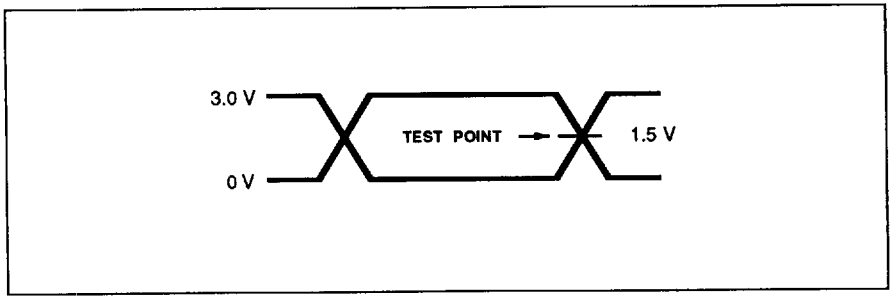
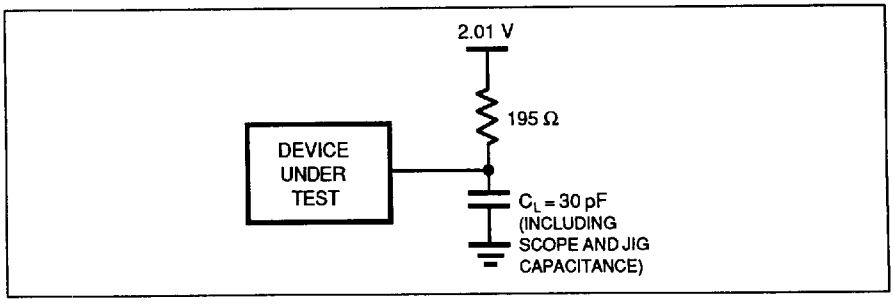


Figure 13. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming.

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Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{BHE}/\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2
RESET	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}/E/\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
AD8/A8	31
AD9/A9	32
AD10/A10	33
GND	34
AD11/A11	35
AD12/A12	36
AD13/A13	37
AD14/A14	38
AD15/A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

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Package Information

Figure 1. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

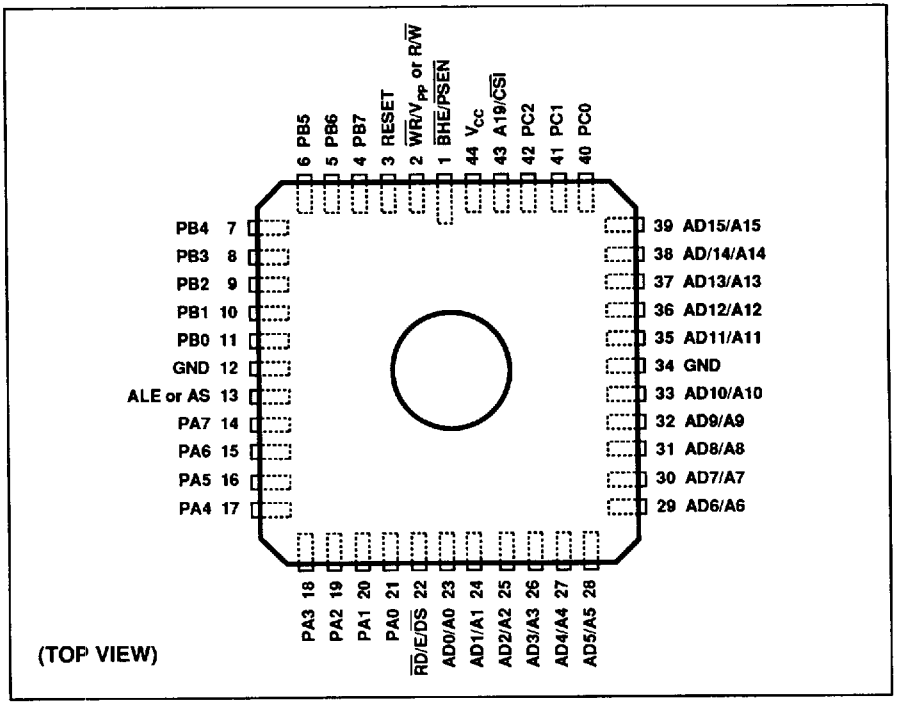
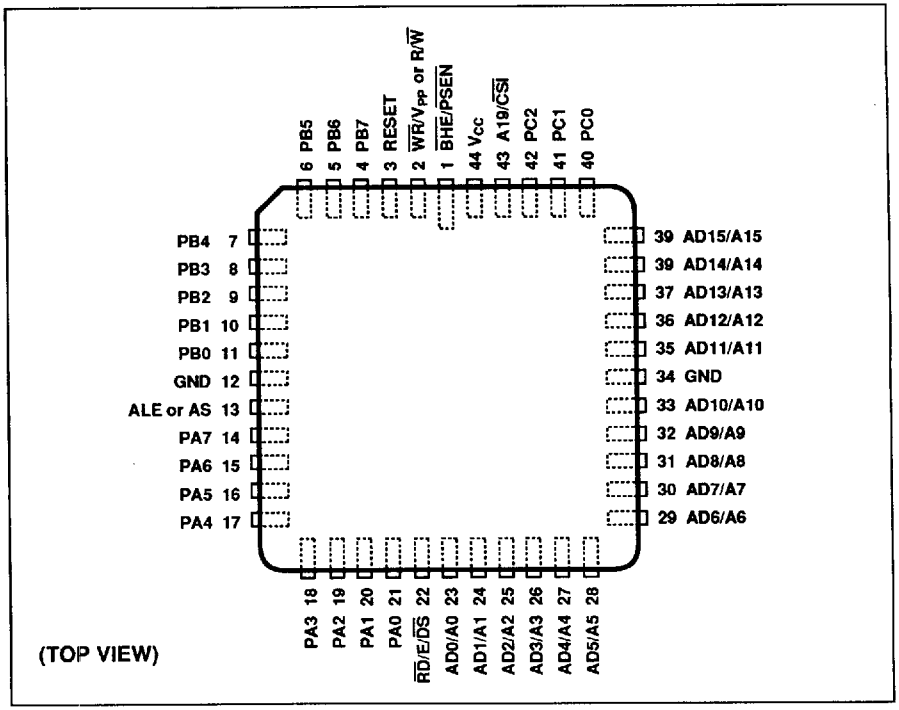


Figure 2. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)



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Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD303-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD303-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD303-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD303-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD303-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD303-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD303-15KA	150	44-pin CLCC	L4	Commercial	Standard
PSD303-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD303-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD303-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD303-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD303-20I KA	200	44-pin CLCC	L4	Industrial	Standard