

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM2365P

DESCRIPTION

The TMM2365P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.

The TMM2365P is fully compatible with a 64 K bits EPROM TMM2764D, so completely replace EPROM socket.

The TMM2365P also features an automatic stand-by power mode. When deselected by Chip Enable

($CE_1 \sim 3 / \overline{CE}_1 \sim 3$), the operating current is reduced from 100mA (MAX) to 25mA (MAX). Output Enable (\overline{OE}) is effective in preventing data confliction of a common bus line.

The TMM2365P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2365P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation

Average Current: 100mA max.

Standby Current: 25mA max.

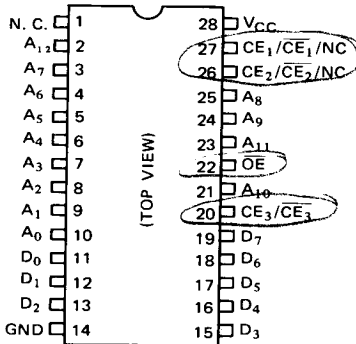
- Input and Output: TTL Compatible

- Three State Outputs: Wired OR Capability
- Output Buffer Control: \overline{OE}
- Programmable Chip Enable: $CE_1 / \overline{CE}_1, CE_2 / \overline{CE}_2, CE_3 / \overline{CE}_3$

Easy Memory Expansion

- Compatible with 64K EPROM TMM2764D

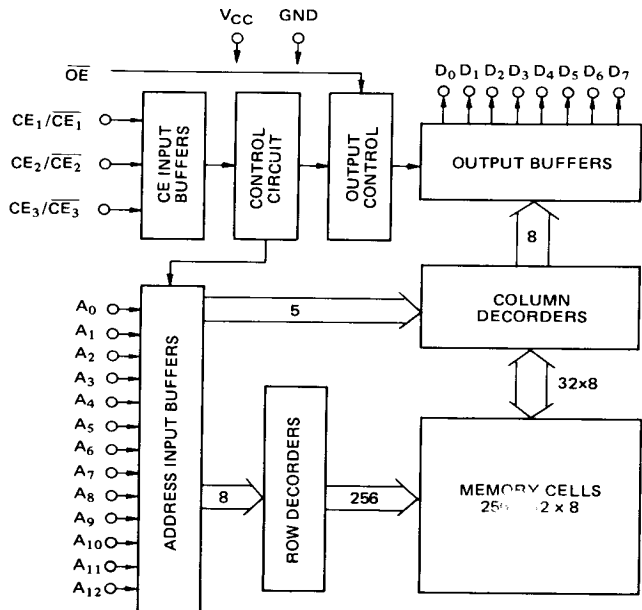
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
\overline{OE}	Output enable input
$CE_1 / \overline{CE}_1, CE_2 / \overline{CE}_2, CE_3 / \overline{CE}_3$	Chip enable inputs
N. C.	No connection
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



TMM2365P

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN} , V _{OUT}	Input and Output Voltage	-0.5 ~ 7.0	V
T _{OPR}	Operating Temperature	0 ~ 70	°C
T _{STG}	Storage Temperature	-55 ~ 150	°C
T _{SD}	Soldering Temperature • Time	260 • 10	°C • sec
P _D	Power Dissipation (T _a = 70°C)	1.0	W

D.C. OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	—	2.0	—	V _{CC} +1	V
V _{IL}	Input Low Voltage	—	-0.5	—	0.8	V
V _{CC}	Power Supply Voltage	—	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IH}	Input High Current	V _{IN} = 5.5V	—	10	μA
I _{IL}	Input Low Current	V _{IN} = GND	—	-10	μA
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	—	V
V _{OL}	Output Low Voltage	I _{OL} = 3.2mA	—	0.4	V
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC}	-10	10	μA
I _{CC1}	Standby Current	CE = 2.0V, CE = 0.8V	—	25	mA
I _{CC2}	Average Current	t _{CYC} = 200ns, I _{OUT} = 0mA	—	100	mA

A.C. CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t _{ACC}	Access Time	—	200	ns
t _{CE}	Output Delay Time from CE _{1~3} /CE _{1~3}	—	200	ns
t _{OE}	Output Delay Time from OE	—	70	ns
t _{OD}	Output Turn off Delay	—	60	ns
t _{CYC}	Cycle Time	200	—	ns

A.C. TEST CONDITIONS

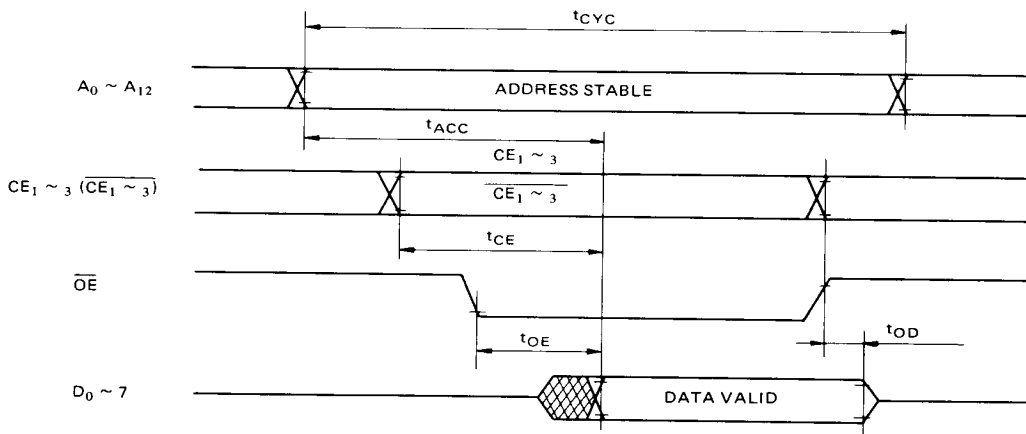
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels : Input ; 1V and 2.0V
Output; 0.8V and 2.0V

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{A.C. GND}$	—	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{A.C. GND}$	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



Note: t_{OD} is specified from \overline{OE} or CE/\overline{CE} , whichever occurs first.

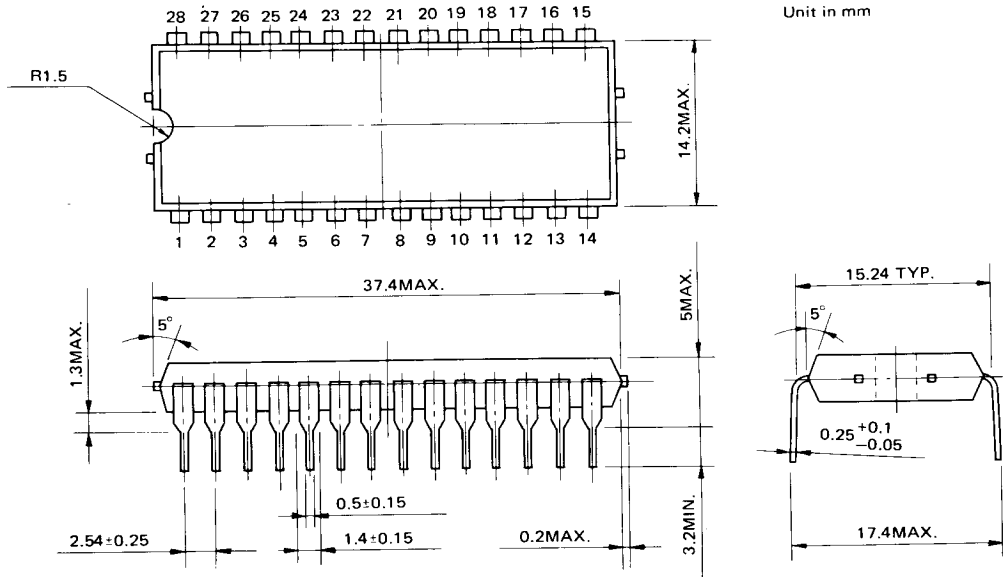
POWER ON

The TMM2365 has self substrate-bias generator internally. So a minimum $100\mu\text{s}$ time delay is

required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

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OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No.28 leads.