NEC

NEC Electronics Inc.

MC-41256A4
262,144 x 4-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATON

April 1986

Description

The MC-41256A4 is a 262,144-word by 4-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A4 operates like four μPD41256 standard 256K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes four μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

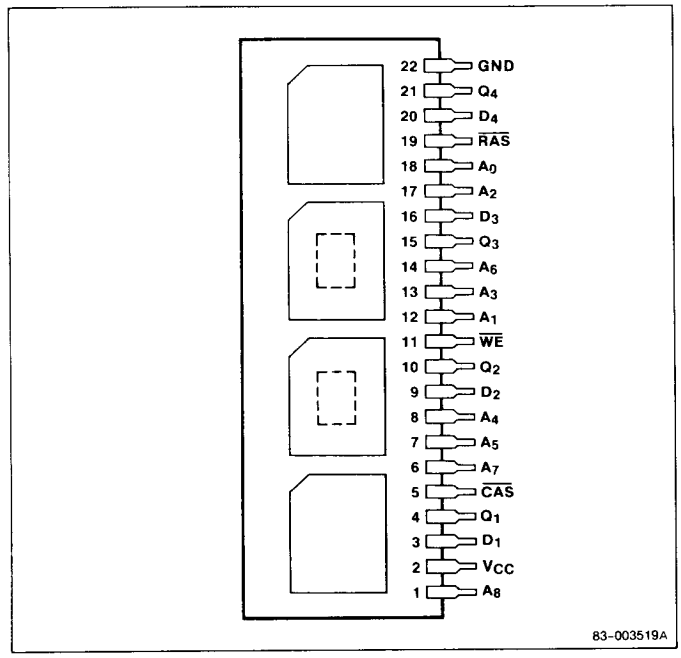
- ☐ 262,144-word by 4-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 22-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates four 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 110 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

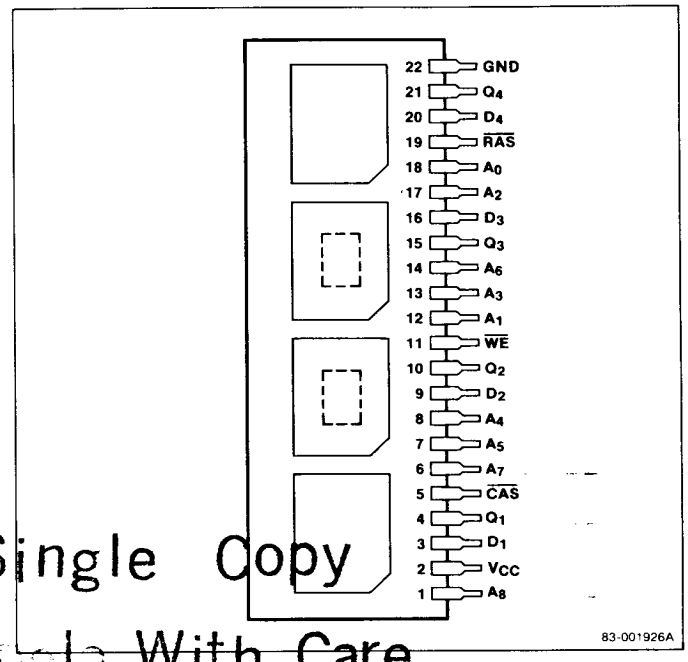
Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A4-12	120 ns	220 ns	120 ns
MC-41256A4-15	150 ns	260 ns	145 ns

Pin Configuration

22-Pin SIMM, MC-41256A4A
(Glass-epoxy Substrate)



22-Pin SIMM, MC-41256A4C
(Ceramic Substrate)



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Pin Identification

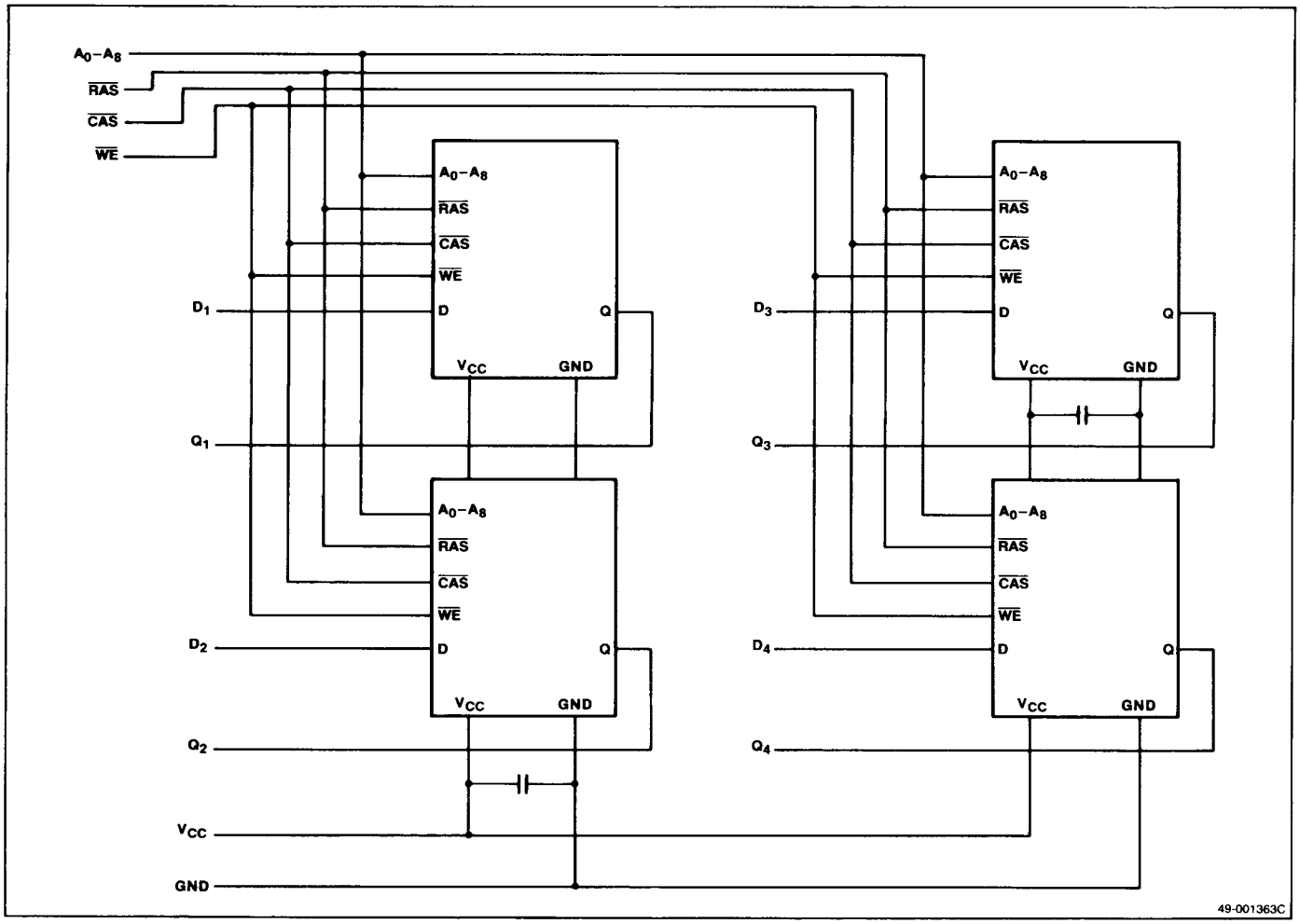
No.	Symbol	Function
1, 6-8, 12-14, 17, 18	A_0-A_8	Address inputs
2	V_{CC}	Power supply (+5.0 V)
3, 9, 16, 20	D_1-D_4	Data inputs
4, 10, 15, 21	Q_1-Q_4	Data outputs
5	$\overline{CAS}$	Column address strobe
11	$\overline{WE}$	Write enable
19	$\overline{RAS}$	Row address strobe
22	GND	Ground

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	4.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			40	pF	A_0-A_8
Input capacitance	C_{IR}			50	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			50	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			15	pF	D_1-D_4, Q_1-Q_4 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			20.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−40		40	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Data input leakage current	$I_{IL(D)}$	−10		10	μA	For D_1-D_4; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	Max	MC-41256A4-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		332		280	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Operating current, refresh mode, average	I_{CC3}		260		212	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Operating current, page mode, average	I_{CC4}		180		140	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		270		225	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	MC-41256A4-12 Max	MC-41256A4-15 Min	MC-41256A4-15 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

AC Characteristics (cont)

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

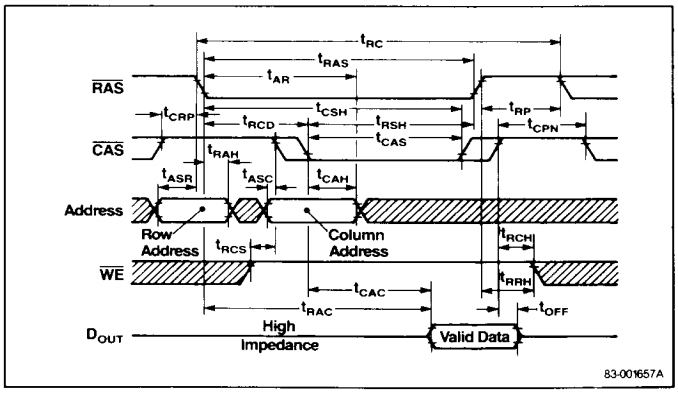
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

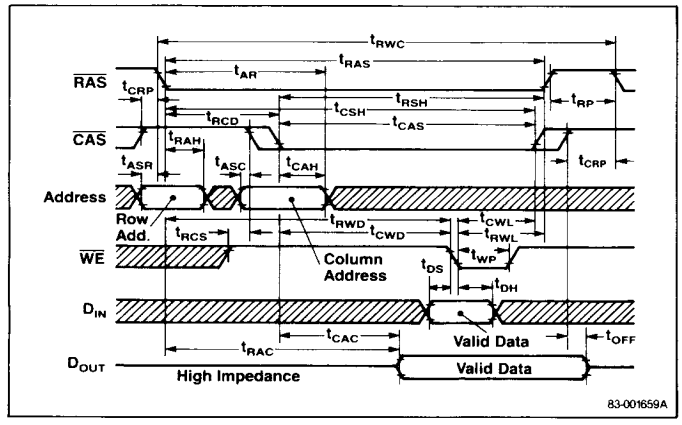
(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

Timing Waveforms

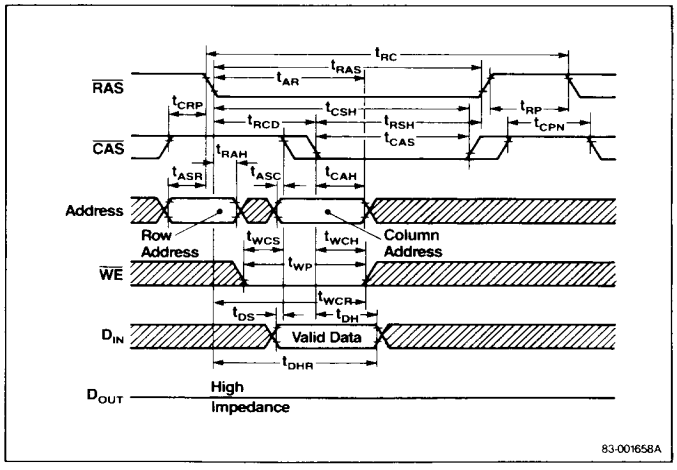
Read Cycle



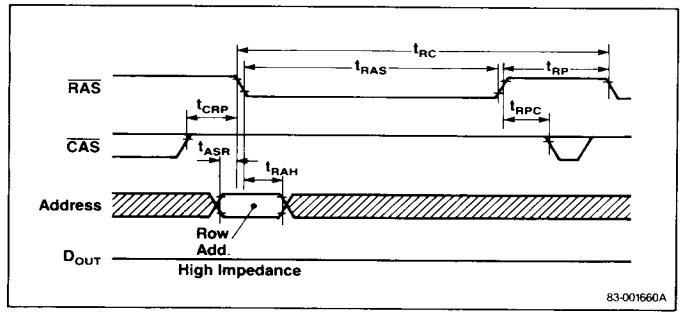
Read-Write/Read-Modify-Write Cycle



Write Cycle (Early Write)

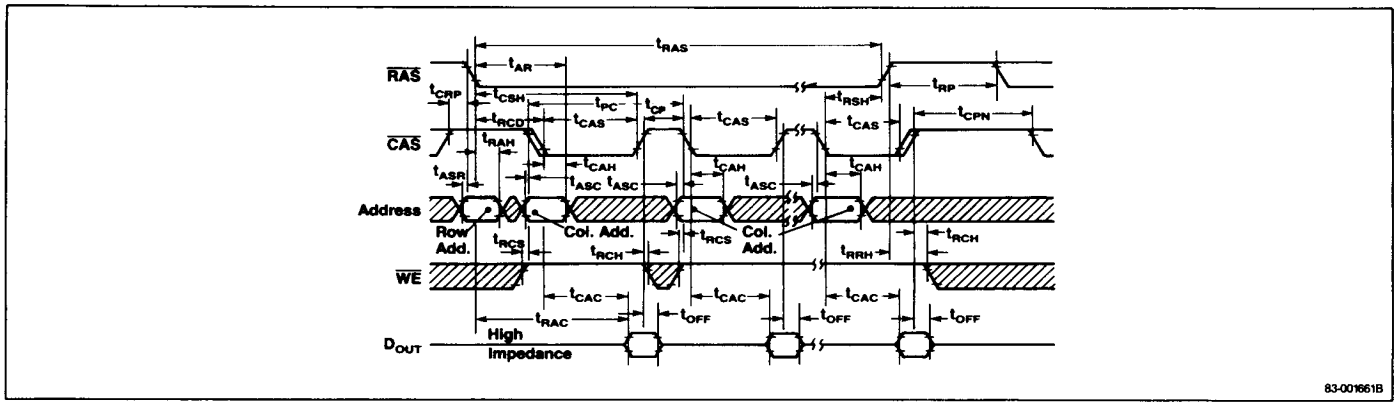


$\overline{RAS}$-Only Refresh Cycle

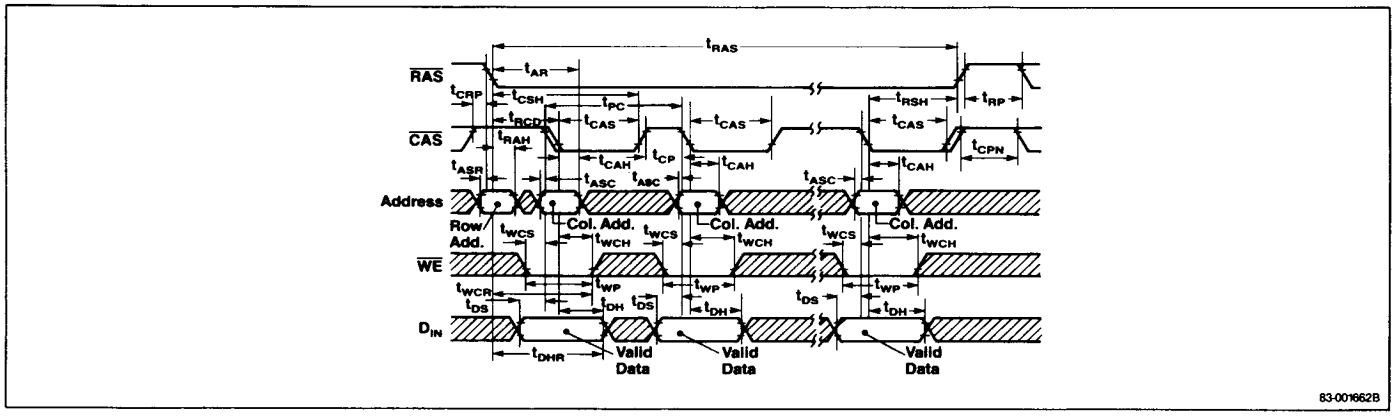


Timing Waveforms (cont)

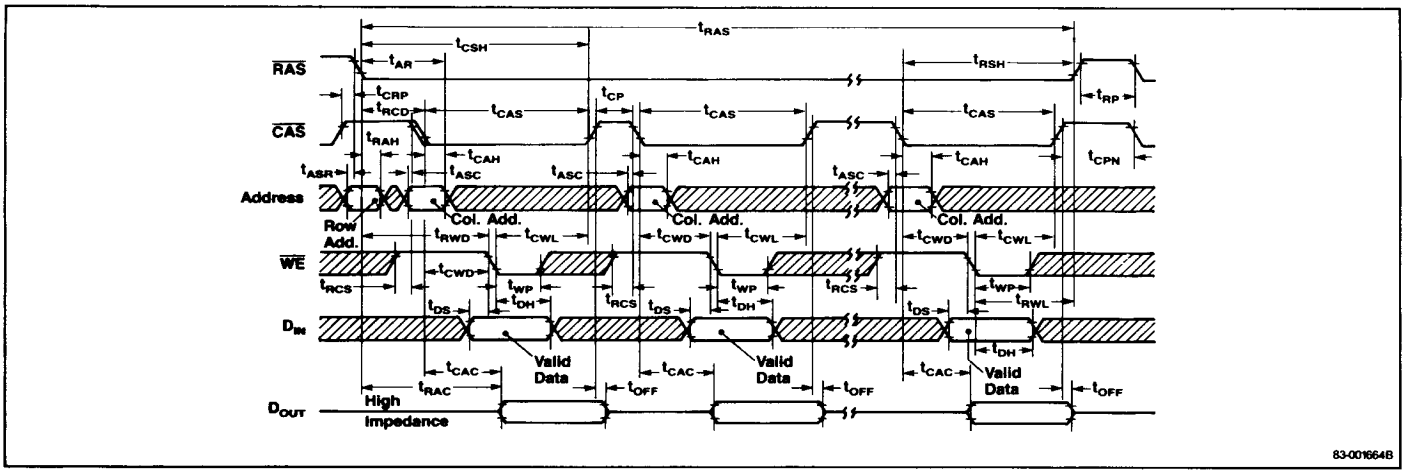
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

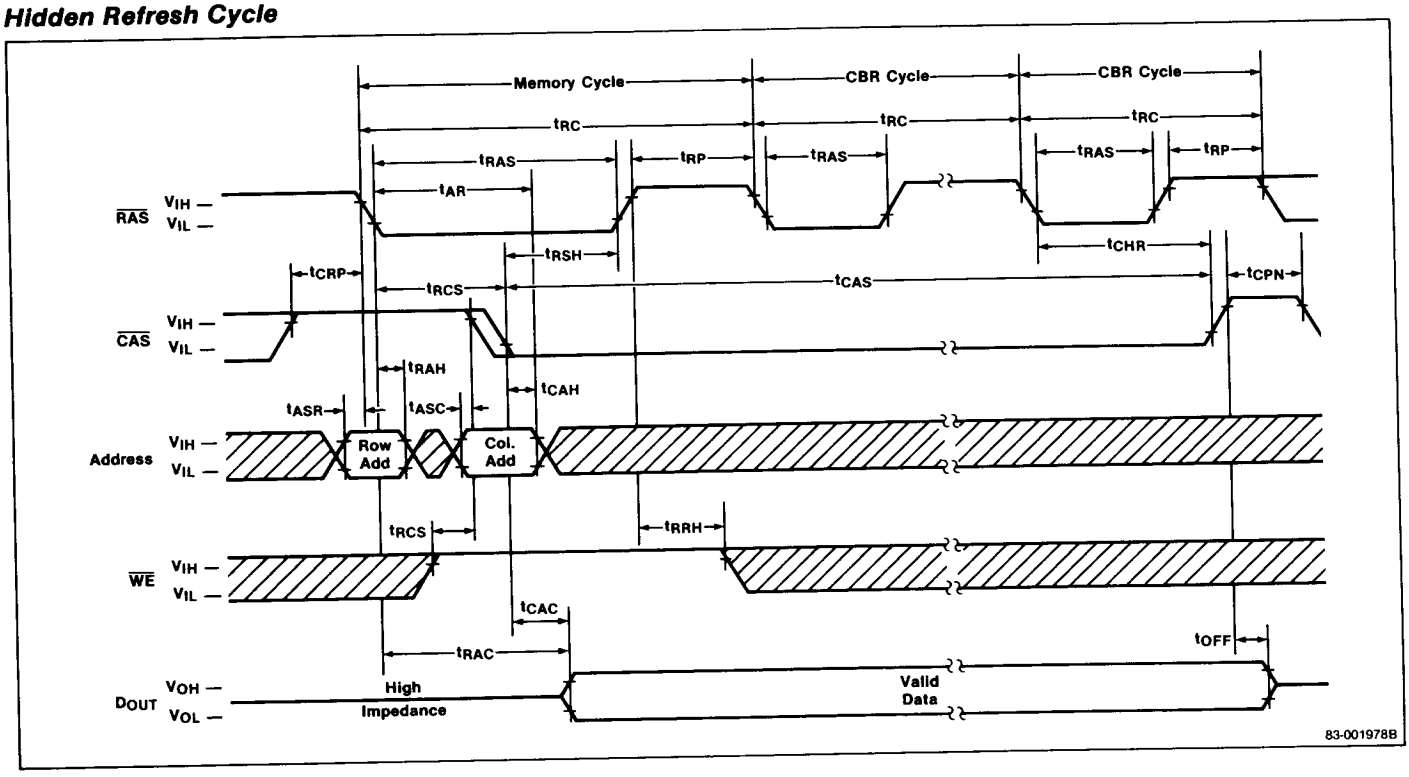


Page Mode Read-Write/Read-Modify-Write Cycle

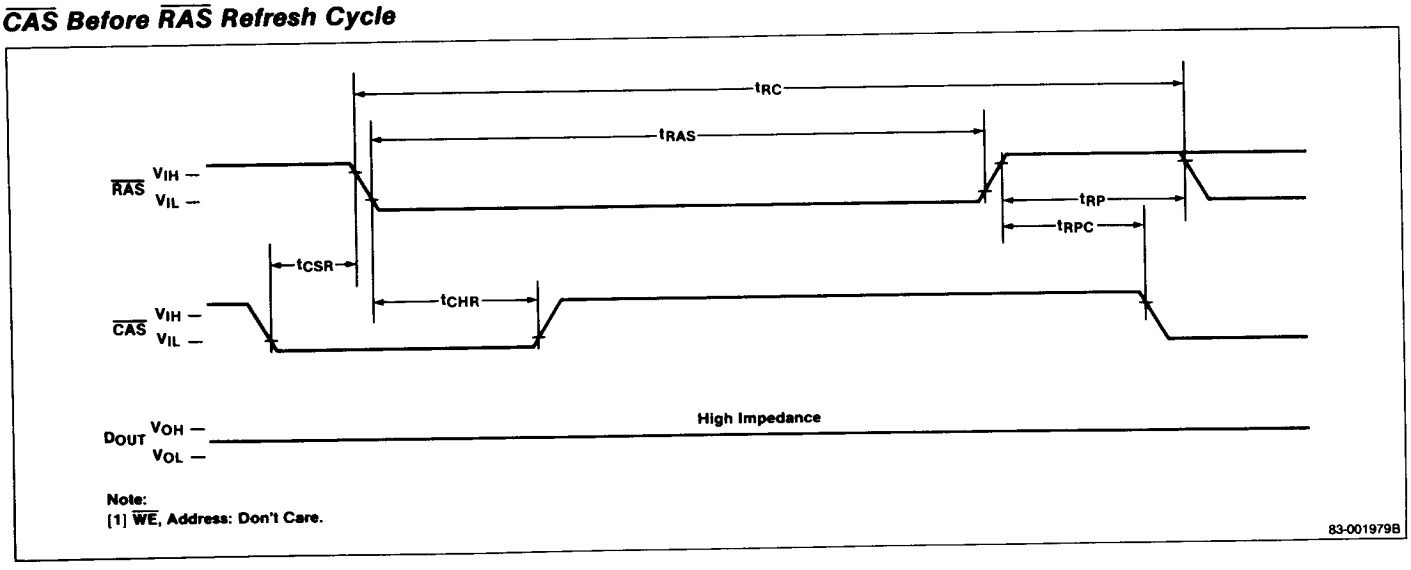


Timing Waveforms (cont)

Hidden Refresh Cycle



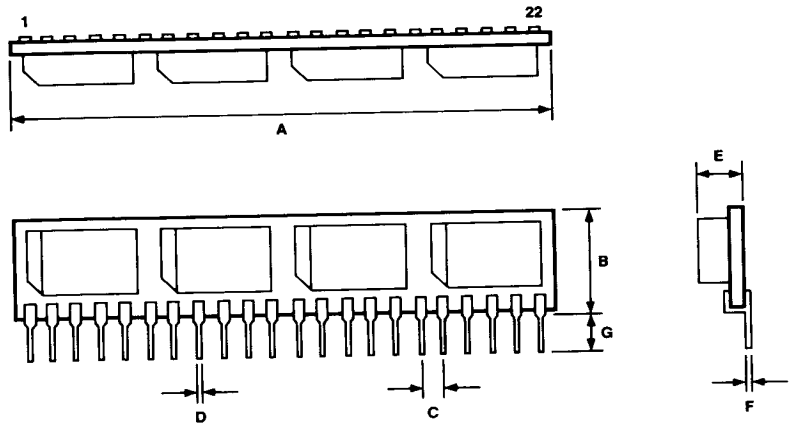
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Packaging Information

22-Pin SIMM, MC-41256A4A (Glass-epoxy Substrate)

Item	Millimeters	Inches
A	56.52	2.225
B	11.43 max	.450 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157



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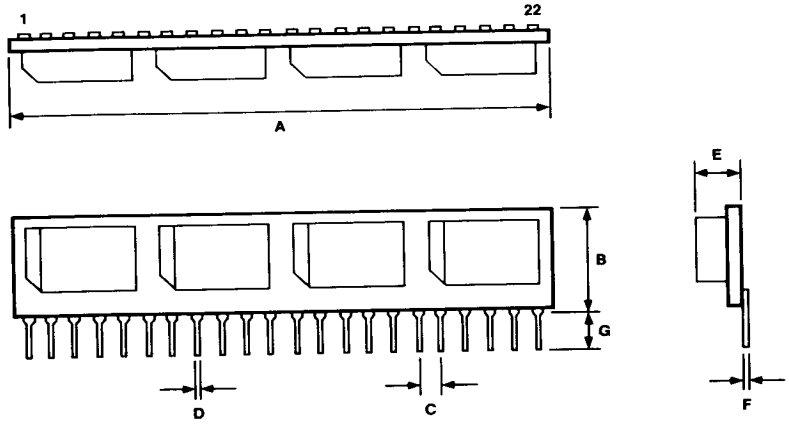
22-Pin SIMM, MC-41256A4C (Ceramic Substrate)

Item	Millimeters	Inches
A	56.52	2.225
B	9.70 max	.382 max
C	2.54	.100
D	.45	.018
E	5.08 max	.200 max
F	.25	.010
G	4.00	.157



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