# 74LS429 FIFO RAM Controller (FRC)

**Preliminary Specification** 

#### **Logic Products**

#### **FEATURES**

- Direct addressing up to 64K
- Cascadable for addressing beyond 64K
- Asynchronous Read/Write operation
- 3-State address outputs
- Selectable FIFO length in multiples of 2
- Specially designed for use with high-speed SRAMs
- TTL input and output
- 16mA address-drive capability
- Programmable half-full signal
- Programmable Read, Write and Status counters

#### DESCRIPTION

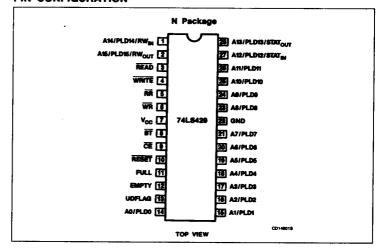
The FRC is an address and status generator designed to implement high-speed/high-capacity First-In First-Out (FIFO) memory buffers utilizing high-speed SRAMs. The FRC can control up to 65,536 (64K) words of buffer memory. The Address Length Register and the Read, Write, and Status Counters are fully programmable. There is also a user-definable status flag to aid in block transfers. The device is cascadable if FIFO buffers in excess of 64K are desired. In the cascade mode, two devices can address up to 16 Mega-words of memory.

| TYPE    | TYPICAL TRANSFER<br>RATE | TYPICAL SUPPLY<br>CURRENT |
|---------|--------------------------|---------------------------|
| 74LS429 | 20MHz                    | 185mA                     |

#### ORDERING INFORMATION

| DESCRIPTION        | COMMERCIAL RANGE<br>V <sub>CC</sub> = 5V ± 5%, T <sub>A</sub> = 0°C to +70°C |
|--------------------|--|
| 28-Pin Plastic DIP | N74LS429N  |

#### PIN CONFIGURATION



#### **ARCHITECTURE**

The FRC (Figure 1) is made up of three 16-bit counters, arbitration logic, mux/latch circuitry and the necessary control logic to generate status flags and control the device. Two of the counters (Read and Write) are up counters and are used to generate addresses for the memory. The third counter (Status) is an up/down counter and is used to generate the status flags, i.e, FULL, EMPTY and User-Defined Flag (UDFLAG).

The Read (RR) and Write (WR) requests may occur asynchronously, but only one operation (either Read or Write) will be serviced by the FRC. This decision is made by the arbitration logic.

In the normal mode the device has a maximum of 16 address outputs. A Write request will cause the contents of the Write Counter to be transferred to these outputs and the

WRITE output to go Low. After the request is removed the Write and Status counters will be updated so that they will be ready when the next Write request occurs. A Read request will cause the contents of the Read Counter to be transferred to the address outputs and the READ output to go Low. After the request is removed, Read and Status counters are updated. The device may also be used in cascade mode. When used in this way the most significant four-address outputs (A12-A15) are no longer address outputs but are used instead for transferring the conditions of the three internal counters from one device to the next. Two devices cascaded will have a combined address length of 24bits which can address 16 mega-words of memory.

The Burst Transfer Mode allows the device to be exclusively used as either a Write address or Read address generator by disabling the

complementary operation (Read or Write). An example of when this mode might be used is the case where a fast processor and a slow peripheral are both accessing the FIFO buffer at the same time. The processor could block the peripheral from accessing the FIFO by forcing the Burst Transfer (BT) input Low (while it is making a request) and then continue reading or writing without having to interleave cycles with the slower peripheral. When the processor completes its operation, it will force the BT input High, allowing the peripheral to access the FIFO.

The two internal registers (Address Length and UDFLAG) and the three counters (Read, Write, and Status) are fully programmable.

The control logic automatically compensates for address lengths less than 16 bits (per device); therefore, the status flags (FULL, EMPTY, and UDFLAG) are always generated to reflect the appropriate condition.

#### PIN DESCRIPTION

| PIN NO. | SYMBOL | TYPE | DESCRIPTION   |
|---------|--------|------|---|
| 5       | RR     | 1    | READ REQUEST for Read cycle: A High-to-Low transition causes the contents of the Read Counter to be transferred to the address outputs followed by assertion of the READ output. The Read and Status Counters are incremented and decremented respectively on the Low-to-High transition. READ output is also negated at this time, but the address bus is held in the stable state. This input is used as a control pin when presetting the internal counters and registers (see Table 1).   |
| 6       | WR     | ı    | WRITE REQUEST for Write cycle: A High-to-Low transition causes the contents of the Write Counter to be transferred to the address outputs followed by assertion of the WRITE output. The Write and Status Counters are incremented on the Low-to-High transition. WRITE output is also negated at this time, but the address bus is held in the stable state. This input is used as a control pin when presetting the internal counters and registers (see Table 1).  |
| 10      | RESET  | 1    | RESET: A Low-to-High transition on this input resets the Read, Write and Status Counters. The address is programmed to the desired FIFO depth and the UDFLAG Register is set to reflect a Half-Full condition. MUX/LATCHs are also cleared. A Low on this pin will 3-State the address bus. CE has to be Low in order to perform any of the above functions. This input is used as a control pin when presetting the internal counters and registers (see Table 1).   |
| 9       | CE     |      | CHIP ENABLE: FRC is enabled when this input is Low. When High READ, WRITE and address outputs will be 3-Stated. This pin is also used as a Write input (data clocked on the Low-to-High edge) when presetting the internal counters and registers (see Table 1).  |
| 8       | BT     | 1    | BURST TRANSFER: When Low it will allow either the Read or Write operation to function without having to interleave cycles with the other operation by disabling the other input. Resetting the device when this input is High will cause the FRC to operate in the normal (non-cascade) mode. Resetting when a Low level is present on this pin will initialize the device to operate in the cascade mode.  |
| 3       | READ   | 0    | READ: This output goes Low after a Read request is selected to be serviced. It returns to the High state when the Read Request is removed. This pin is 3-Stated if either CE is High or RESET is Low.   |
| 4       | WRITE  | 0    | WRITE: This output goes Low after a Write Request is selected to be serviced. It returns to the High state when the Write Request is removed. This pin is 3-Stated if either CE is High or RESET is Low.  |
| 11      | FULL   | 1/0  | FULL: This open-collector output becomes active-High when the used bits (adjusted for address length) of the Status Register are all ones. After a FULL condition is reached, any additional Writes will cause the FRC to scroll the memory (Read and Write Counters will increment together). A Read will always remove the FULL condition causing this output to go Low. If this pin is forced Low after a FULL condition is reached, the device will operate normally (no scrolling). The next Write after the pin is forced Low will remove the FULL condition and this output will remain Low until all of the Status Counter bits are ones again. |

### PIN DESCRIPTION (Continued)

| PIN NO.        | SYMBOL                     | TYPE | DESCRIPTION  |
|----------------|----------------------------|------|--|
| 12             | EMPTY                      | 1/0  | EMPTY: This open-collector output becomes active-High when the used bits of the Status Register are all zeroes. After an EMPTY condition is reached, any additional Reads will cause the FRC to scroll the memory. A Write will always remove the EMPTY condition causing this output to go Low. If this pin is forced Low after an EMPTY condition is reached, the device will operate normally (no scrolling). The next Read after the pin is forced Low will remove the EMPTY condition and this output will remain Low until all of the Status Counter bits are zeroes again.  |
| 13             | UDFLAG                     | 0    | UDFLAG: If not predefined by the user, this open-collector output will become active-High when the most significant bit (adjusted for address length) of the Status Register is High and all other bits are zero (i.e. reflecting a Half-Full condition). If predefined, it will go High when the value of the Status Register is equal to the defined value (see Initialization/programming mode).  |
| 14-21<br>23-26 | A0/PLD0<br>to<br>A11/PLD11 | 1/0  | ADDRESS/PRELOAD DATA: active-High data input and address output pins. When used as address outputs, they will either contain a Read or a Write address depending upon the input request. These outputs can be 3-Stated during normal operation by forcing CE High. A0 is the least significant address bit. These pins are used as active-High data inputs when programming the internal counters and registers of the device. PLD0 is the least significant preload data bit.   |
| 27             | A12/PLD12<br>STATIN        | 1/0  | ADDRESS 12/ PRELOAD DATA 12/ STATUS INput: This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 12 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing CE High. When preloading the internal counters and registers of the device, this pin becomes bit 12 of the preload data. This is an active-High input. When the device is used in the cascade mode, this pin becomes an active-High STATus INput. The status input is used to receive information for the previous device so that the Status Counter may be incremented or decremented property. This pin should be hardwired to V <sub>CC</sub> for the least significant device.            |
| 28             | A13/PLD13<br>STATOUT       | 1/0  | ADDRESS13/ PRELOAD DATA13/ STATUS OUTput: This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 13 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing CE High. When preloading the internal counters and registers of the device, this pin becomes Bit 13 of the preload data. This is an active-High input. When the device is used in the cascade mode, this pin becomes an active-High STATus OUTput. The status output is used to send information to the next device so that the Status Counter may be incremented or decremented property.   |
| 1              | A14/PLD<br>14/<br>RWIN     | 1/0  | ADDRESS 14/ PRELOAD DATA 14/ READ WRITE INput: This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 14 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing CE High. When preloading the internal counters and registers of the device, this pin becomes Bit 14 of the preload data. This is an Active-High input. When the device is used in the cascade mode, this pin becomes an active-High Read Write INput. The Read Write INput is used to receive information from the previous device so that the Read and Write counters may be incremented or decremented properly. This pin should be hard wired to VCC for the least significant device. |
| 2              | A 15/PLD<br>15/<br>RWOUT   | 1/0  | ADDRESS 15/ PRELOAD DATA 15/ READ WRITE OUTput: This pin has three different functions depending upon the mode the device is in. When used in the normal mode this pin is an active-High output containing Bit 15 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing CE High. When preloading the internal counters and registers of the device, this pin becomes Bit 15 of the preload data. This is an active-High input. When the device is used in the cascade mode this pin becomes an active-High Read Write OUTput. The Read Write OUTput is used to send information to the next device so that the Read and Write counters of the next device may be incremented properly.  |
| 7              | Vcc                        | ı    | Power supply 5V ± 5%   |
|                |                            |      |  |

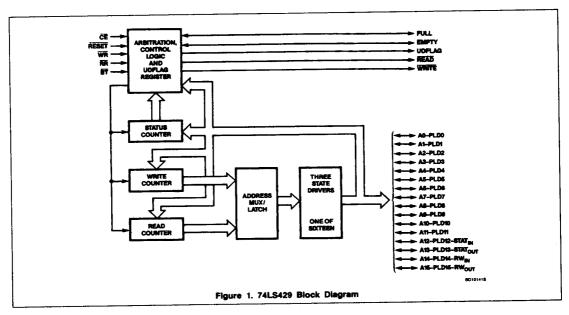


Table 1. Preload/Reset Truth Table

| RESET | CE | WR  | RA | BT | OPERATING MODE                      |  |  |  |
|-------|----|-----|----|----|-------------------------------------|--|--|--|
| ×     | 1  | ×   | ×  | Х  | Disabled                            |  |  |  |
| t     | 1  | ×   | ×  | х  | Disabled, the device will not reset |  |  |  |
| 1     | 0  | ×   | ×  | 1  | Reset and operate in normal mode    |  |  |  |
| t     | 0  | ×   | ×  | 0  | Reset and operate in cascade mode   |  |  |  |
| 0     | 1  | 0   | 0  | х  | Preload Status Register             |  |  |  |
| 0     | 1  | 0   | 1  | х  | Preload Read Counter                |  |  |  |
| 0     | 1  | 1 1 | 0  | ×  | Preload Write Counter               |  |  |  |
| 0     | 1  | 1   | 1  | ×  | Set UDFLAG Register                 |  |  |  |

x = Don't care

1 = High state † = Rising edge

<sup>0 =</sup> Low state

#### **FUNCTIONAL OPERATION**

The FRC may operate either in the normal or the cascade mode. The following description will apply to both of these modes unless otherwise specified. However, a more detailed operation in the cascade mode is included under the Cascade Mode Operation

The FRC operates in either of the two basic modes; Write into the FIFO buffer memory or Read from the FIFO buffer memory. However, the device may also be in the initialization (programming) or arbitration phase.

#### INITIALIZATION/PROGRAMMING MODE

The FRC does not wake-up in a defined state and, therefore, the user must provide a power-up reset to ensure proper operation of the device. The length of the FIFO is programmable (in multiples of 2) and is accomplished by grounding the unused address outputs through a 1K resistor. It is necessary to reset the device, each time the FIFO length is changed.

The FRC has programmable Read, Write and Status Counters. The user can initialize these counters to any desired value. When programming these counters, A0 - A15 address outputs will become inputs and should contain the pre-load data that will be written into the selected counter. The UDFLAG output of the device is also programmable and, therefore, can be set to become active at any desired time (Table 1).

Asserting a RESET after programming the above counters and UDFLAG will reset the device, i.e., Read, Write and Status Counter will be reset, UDFLAG will be set to reflect a half full condition, and address mux/latch will be cleared.

#### **ARBITRATION MODE**

Because of the asynchronous nature of the RR and WR signals, it is necessary to provide arbitration between these two to avoid the possibilities of operational conflicts. The arbitration logic in the FRC is implemented such that the WR input dominates the selection process. The RR has to occur a specified amount of time before the WR in order to be selected. If the  $\overline{WR}$  occurs before the  $\overline{RR}$ , the WR will always be selected.

If both RR and WR occur at the same time, WR will be selected. Neither RR nor WR are latched internally.

#### WRITE CYCLE

To perform a write operation, WR must be Low and selected by the arbitration logic. This

December 1987

will cause the contents of the Write Address Counter to be output on the address bus. followed by assertion of the WRITE output. Normally, the WRITE output will be asserted after the address outputs are stable.

When the Write cycle is ended (WR is forced High), WRITE output will be negated, but the address outputs will be latched and held in the stable state until the next Read or Write Request is made

Forcing WR High will increment both the Write and Status counters, but the Read counter will remain unchanged. The incremented value of the Write Counter will not be enabled on to the address bus until the next Write Request.

#### READ CYCLE

To perform a read operation RD must be Low and selected by the arbitration logic. This will cause the contents of the Read Counter to be output on the address bus, followed by assertion of the READ output. Normally, the READ output will be asserted after the address outputs are stable. When the read cycle is ended (RR is forced High), READ output will be negated, but the address outputs will be latched and held in the stable state until the next Read or a Write Request is made Forcing RR High will increment the Read Counter, decrement the Status Counter and leave the Write Counter unchanged. The incremented value of the Read Counter will not be enabled on to the address bus until the next Read Request.

#### CONTROL LOGIC

In addition to all the necessary internal timing, this section of the FRC is also responsible for the generation of FULL, EMPTY, UDFLAG, and the signals necessary for cascade mode operation.

#### CASCADE MODE INTERFACE

For applications that require more than 64K of addressing capability, two or more FRCs may be used in the cascade mode. The cascade mode circuitry is activated by resetting the device while holding the BT input Low. When the device is in the cascade mode the most significant four address outputs (A12 - A15) are used to transfer register information to the next most significant device and therefore are no longer address outputs. A0 of the next most significant device will now be A12 of the address bus and so on. It is important to distinguish between the least significant and the most significant devices. The FRC automatically makes this decision when a RESET is issued while BT is Low. The device with Pin 27 (A12/PLD12/STATIN) tied

to V<sub>CC</sub> is selected as the Least Significant Device (LSD) and the device with Pin 28 (A13/PLD13/STATOUT) tied to ground is selected as the Most Significant Device (MSD). In a typical configuration (see Figure 2) STATIN and RWIN of the LSD will be connected to V<sub>CC</sub> and STATOUT of the MSD will be connected to ground. RWOUT of the LSD will be connected to RWIN of the next MSD, but the RWOUT of the MSD may be left floating. RESET, CE, BT, WR, and RR of all the devices will be connected to each other's corresponding inputs. Similarly FULL, EMPTY and UDFLAG outputs of all the devices will be connected to each other's corresponding outputs. The READ and WRITE outputs from either of the devices may be used to assert a read and/or a write to the memory.

#### **CASCADE MODE OPERATION**

After two or more devices have been interfaced as explained in the previous section and a RESET is issued while BT is held Low, all devices will be initialized. This will also cause the devices to distinguish themselves in their respective order in the system, i.e., least significant, next most significant and most significant. At this time STATOUT and RWOUT of all the devices connected to STATIN and RWIN of the next device will be

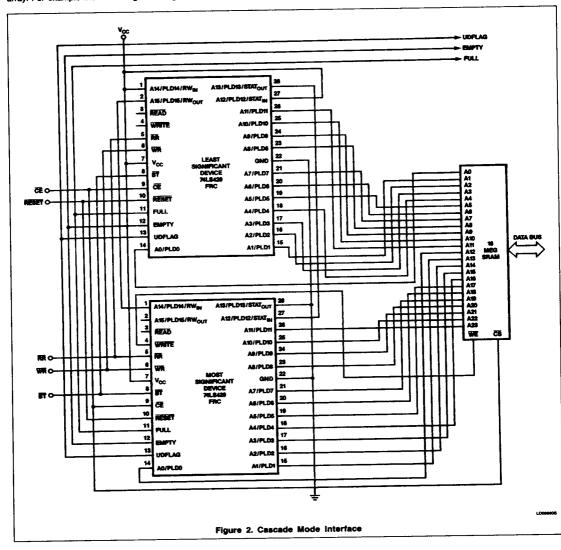
The user may at this point desire to preload the internal registers of the devices. This can be done exactly as if a single device was being programmed (see Initialization/Programming Mode). The only distinction that has to be kept in mind this time is that PLD12 of the LSD should now be presented to PLD0 of the next most significant device and so on. When programmed for cascade mode operation, Read, Write and Status Counters of the FRC are inhibited from clocking for as long as STATIN and RWIN inputs are Low. Since STATIN and RWIN of only the LSD are High at RESET, it will be the only device with Read, Write and Status Counters enabled. When the Read or Write counters of the LSD are empty or full, respectively, the next Lowto-High transition of the RR or WR will generate RWOUT. This will cause the RWIN input of the next MSD to be High, hence enabling the Read and Write counters of that device. Similarly, the STATOUT pin of the LSD will go High when the Status counter is full and a WR is made or when it is empty and a RR is made.

This will produce a High at the STATIN pin of the next MSD, hence enabling its Status Counter to increment or decrement as the case might be.

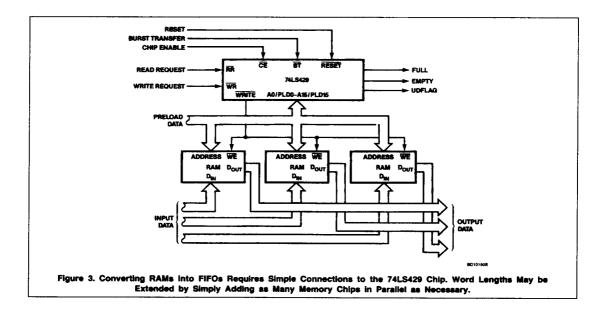
3-42

The Status flags (FULL, EMPTY and UDarray. For example the FULL flag will not go of all the devices are open-collector and

High when the LSD represents a full condi-FLAG) will go High only when the condition tion, but the next Most Significant Devices they represent is true across the entire FRC don't. This is because the Status Flag outputs wired together. Therefore, any of these flag outputs will only go High when that condition holds for all the devices.



3-43



### ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

| PARAMETER      | RATING   | UNIT   |
|----------------|--|--|
| Supply voltage | -0.5 to +7.0   | V  |
|                | -0.5 to +7.0   | V  |
|                | -30 to +1.0  | mA   |
|                | -0.5 to +V <sub>CC</sub>   | V  |
|                | 0 to +70   | ္  |
|                | -65 to +150  | •¢   |
|                | Supply voltage Input voltage Input current Voltage applied to output in High output state Operating free-air temperature range Storage temperature | Supply voltage         -0.5 to +7.0           Input voltage         -0.5 to +7.0           Input current         -30 to +1.0           Voltage applied to output in High output state         -0.5 to +V <sub>CC</sub> Operating free-air temperature range         0 to +70 |

## RECOMMENDED OPERATING CONDITIONS

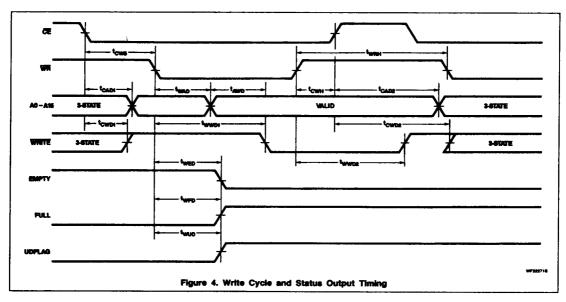
|                               | PARAMETER                            |  |     | LIMITS |     |      |  |
|-------------------------------|--------------------------------------|--|-----|--------|-----|------|--|
| SYMBOL                        |                                      |  |     | Nom    | Mex | UNIT |  |
| Vcc                           | Supply voltage                       | 4.75                                     | 5.0 | 5.25   | ٧   |      |  |
| VIH                           | High-level input voltage             |  | 2.0 |        |     | V    |  |
| VIL                           | Low-level input voltage              |  |     |        | 0.8 | ٧    |  |
| IK                            | Input clamp current                  |  |     |        | -18 | mA   |  |
| loH                           | High-level output current            |  |     |        | -3  | mA   |  |
| ·On                           |                                      | FULL, EMPTY, UDFLAG                      |     |        | 8   | mA   |  |
| I <sub>OL</sub> Low-level out | Low-level output current             | vel output current A0 - A15, WRITE, READ |     |        | 16  | mA   |  |
| TA                            | Operating free-air temperature range |  | 0   |        | 70  | •c   |  |

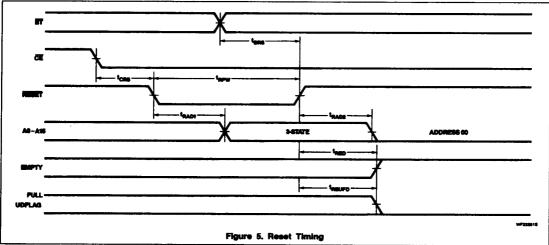
## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

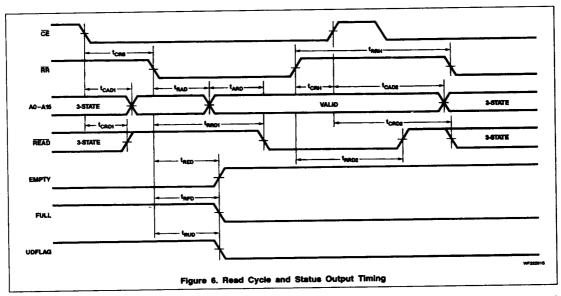
|                               | PARAMETER  |                         | TEST CONDITIONS                                  |                                  |          | LIMITS           |          |          |
|-------------------------------|--|-------------------------|--|----------------------------------|----------|------------------|----------|----------|
| SYMBOL                        |  |                         |  |                                  | Min      | Typ <sup>2</sup> | Max      | UNIT     |
| V <sub>OH</sub>               | High-level output vol                                  | tage                    | V <sub>CC</sub> = MIN,<br>V <sub>IH</sub> = MIN, | 2.7                              |          |                  | <b>v</b> |          |
| Vol. Low-level output voltage | FULL, EMPTY UDFLAG                                     | V <sub>CC</sub> = MIN,  | I <sub>OL</sub> = 8mA                            |                                  |          | 0.5              | ٧        |          |
|                               |  | READ, WRITE<br>A0 - A15 |  | I <sub>OL</sub> = 16mA           |          |                  | 0.5      | ٧        |
| VIK                           | Input clamp voltage                                    |                         | V <sub>∞</sub> =                                 | I <sub>I</sub> = I <sub>IK</sub> | <b>_</b> | <u> </u>         | -1.5     | <u> </u> |
| l <sub>l</sub>                | Input current at max input voltage                     | imum                    | V <sub>CC</sub> = MAX                            | , ∨ <sub>1</sub> = 7.0∨          |          |                  | 100      | μА       |
| I <sub>IH</sub>               | High-level input current                               |                         | V <sub>CC</sub> = MAX                            | , V <sub>I</sub> = 2.7V          |          | <u> </u>         | 20       | μΑ       |
| l <sub>IL</sub>               | Low-level input curre                                  | ent                     | V <sub>CC</sub> = MAX                            | , V <sub>I</sub> = 0.4V          |          |                  | -0.4     | mA       |
| lozh                          | OFF-state output current<br>High-level voltage applied |                         | V <sub>CC</sub> = MAX                            | , V <sub>O</sub> = 2.4V          |          | <u> </u>         | 20       | μА       |
| lozL                          | OFF-state output current Low-level voltage applied     |                         | V <sub>CC</sub> = MAX                            | , V <sub>O</sub> = 0.5V          |          |                  | -20      | μА       |
| los                           | Short-circuit output current <sup>3</sup>              |                         |  | MAX                              | -15      | <del>  </del>    | -100     | mA       |
| loc                           | Supply current (total                                  |                         | V <sub>CC</sub> =                                | MAX                              |          | <u> </u>         | 210      | mA       |

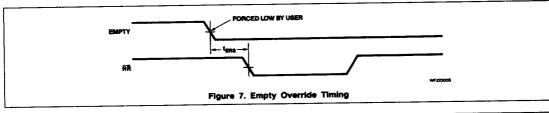
- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ . 3.  $I_{OS}$  is tested with  $V_{OUT} = +0.5V$  and  $V_{CC} = V_{CC}$  Max +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

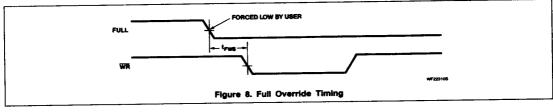
3-45

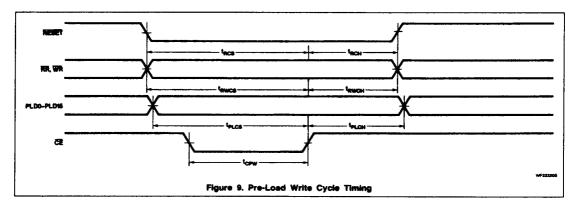


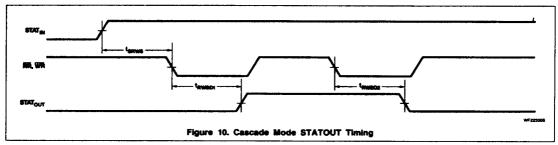


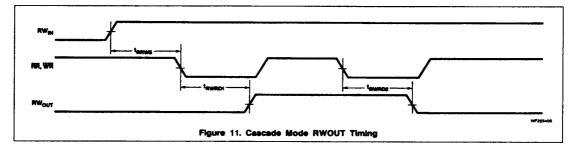








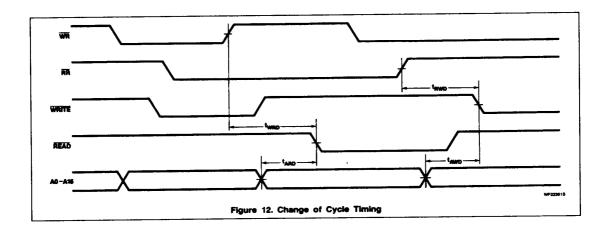




3-48

## FIFO RAM Controller (FRC)

74LS429



### AC ELECTRICAL CHARACTERISTICS TA = 25°C, VCC = 5V ± 5%

|                   | BARAMETERS              |                 | LIN | UNIT |      |
|-------------------|-------------------------|-----------------|-----|------|------|
| SYMBOL            | PARAMETERS              | TEST CONDITIONS | Min | Max  | UNIT |
| Write cyc         | cle timing              |                 |     |      |      |
| tcws              | CE setup to WR          |                 |     |      | ns   |
| twan              | WR↑ to WR↓ hold         |                 | 14  |      | ns   |
| t <sub>CWH</sub>  | CE Hold after WR ↑      |                 |     |      | ns   |
| t <sub>CAD1</sub> | CE ↓ to address delay   |                 |     |      | ns   |
| t <sub>CAD2</sub> | CE↑ to 3-State address  |                 |     |      | ns   |
| t <sub>CWD1</sub> | CE ↓ to WRITE delay     |                 |     |      | ns   |
| t <sub>CWD2</sub> | CE↑ to WRITE 3-State    | AC Waveforms    |     |      | ns   |
| twwD1             | WR ↓ to WRITE ↓ delay   |                 |     | 26   | ns   |
| twwD2             | WR↑ to WRITE↑ delay     |                 |     | 11.5 | กร   |
| twap              | WR↓ to address valid    |                 |     |      | ns   |
| t <sub>AWD</sub>  | Address valid to WRITE↓ |                 |     | 3    | ns   |
| tweD              | WR ↓ to EMPTY ↓ delay   |                 |     |      | ns   |
| t <sub>WFD</sub>  | WR ↓ to FULL ↑ delay    |                 |     |      | ns   |
| twup              | WR ↓ to UDFLAG ↑ delay  | 7               |     |      | ns   |
| Read cyc          | ile timing              |                 |     |      |      |
| t <sub>CRS</sub>  | CE setup to RR          |                 |     |      | ns   |
| tarh              | RR↑ to RR↓ hold         |                 | 14  |      | ns   |
| t <sub>CRH</sub>  | CE hold after RR 1      |                 |     |      | ns   |
| t <sub>CAD1</sub> | CE ↓ to address delay   |                 |     |      | ns   |
| t <sub>CAD2</sub> | ČĒ↑ to 3-State address  |                 |     |      | ns   |
| t <sub>CRD1</sub> | CE ↓ to READ delay      |                 |     |      | ns   |
| t <sub>CRD2</sub> | CE ↑ to READ 3-State    | AC Waveforms    |     |      | ns   |
| t <sub>RRD1</sub> | RR ↓ to READ ↓ delay    |                 |     | 26   | ns   |
| t <sub>RRD2</sub> | RR↑ to READ↑ delay      |                 |     | 11.5 | ns   |
| t <sub>RAD</sub>  | RR ↓ to address valid   |                 |     |      | ns   |
| tARD              | Address valid to READ ↓ |                 |     | 3    | ns   |
| t <sub>RED</sub>  | RR ↓ to EMPTY ↑ delay   |                 |     |      | ns   |
| t <sub>RFD</sub>  | RR ↓ to FULL ↓ delay    |                 |     |      | ns   |
| t <sub>RUD</sub>  | RR ↓ to UDFLAG ↓ delay  | 7               |     |      | ns   |
| Override          | timing                  |                 |     |      |      |
| t <sub>ERS</sub>  | EMPTY setup to RR↓      |                 |     |      | ns   |
| tews              | FULL setup to WR↓       | AC Waveforms    |     | T    | ns   |

#### NOTE:

<sup>1.</sup> See Test Loading Circuits for loading.

## AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25^{\circ}C$ , $V_{CC} = 5V \pm 5\%$

|                    |                             |                 | LIM  | UNIT     |          |
|--------------------|-----------------------------|-----------------|------|----------|----------|
| SYMBOL             | PARAMETERS                  | TEST CONDITIONS | Min  | Max      | UNIT     |
| Reset tim          | ing                         |                 |      |          | <b>.</b> |
| tapw               | RESET pulse width           |                 |      |          | ns       |
| tcas               | CE setup to RESET ↓         |                 |      | ļ        | ns       |
| teas               | BT setup to RESET ↑         |                 |      |          | ns       |
| t <sub>RAD1</sub>  | RESET ↓ to 3-State address  | AC Waveforms    |      |          | ns       |
| t <sub>RAD2</sub>  | RESET ↑ to all 00 address   |                 |      |          | ns       |
| tRED               | RESET 1 to EMPTY 1          |                 |      |          | ns       |
| †AEUFD             | RESET ↑ to FULL ↓           |                 |      |          | ns       |
| Pre-load           | data write cycle timing     |                 |      |          |          |
| tcpw               | CE pulse width              |                 | L    |          | ns       |
| tacs               | RESET setup to CE 1         |                 |      |          | ns       |
| tawcs              | RR, WR setup to CE↑         | 1               |      |          | ns       |
| tpLCS              | PLD0 - PLD15 setup to CE↑   | AC Waveforms    |      |          | ns       |
| t <sub>RCH</sub>   | RESET hold after CE 1       |                 |      |          | ns       |
| t <sub>RWCH</sub>  | RR, WR hold after CE 1      |                 |      |          | ns       |
| t <sub>PLCH</sub>  | PLD0-PLD15 hold after Œ ↑   |                 |      |          | ns       |
| Cascade            | mode timing                 |                 |      |          |          |
| tsaws              | STATIN setup to RR↓, WR↓    |                 |      |          | ns       |
| t <sub>RWSD1</sub> | RR↓, WR↓ to STATOUT↑ delay  |                 |      |          | ns       |
| t <sub>RWSD2</sub> | RR↓, WR↓ to STATOUT↓ delay  |                 |      |          | ns       |
| tanws              | RWIN setup to RR ↓, WR ↓    | AC Waveforms    |      |          | ns       |
| t <sub>RWRD1</sub> | RR↓, WR↓ to RWOUT ↑ delay   |                 |      | <u> </u> | ns       |
| t <sub>RWRD2</sub> | RR ↓, WR ↓ to RWOUT ↓ delay |                 |      |          | ns       |
| Change o           | of cycle timing             |                 | ···· |          |          |
| twnp               | WR↑ to READ↓                |                 |      |          | ns       |
| t <sub>RWD</sub>   | RR ↑ to WRITE ↓             |                 |      |          | ns       |
| tARD               | Address valid to READ ↓     | AC Waveforms    |      | 3        | ns       |
| tawp               | Address valid to WRITE↓     |                 |      | 3        | ns       |

#### NOTE:

<sup>1.</sup> See Test Loading Circuits for loading.

#### **TEST LOADING CIRCUITS**

