

## 3.5A SWITCHING REGULATOR

ADVANCE DATA

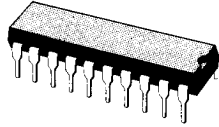
- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHZ
- THERMAL SHUTDOWN

### DESCRIPTION

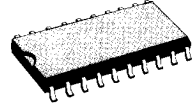
The L4972 is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972 include reset and power fail for microprocessors,

### MULTIPOWER BCD TECHNOLOGY



**POWERDIP**  
(16 + 2 + 2)

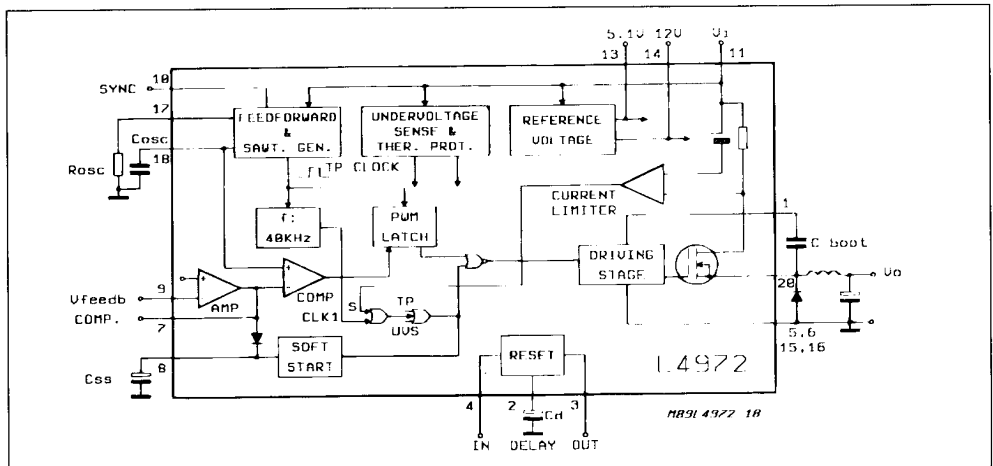


**SO20L**

**ORDER CODE** : L4972 (Powerdip)  
 L4972D (SO20L)

feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

### BLOCK DIAGRAM



March 1989

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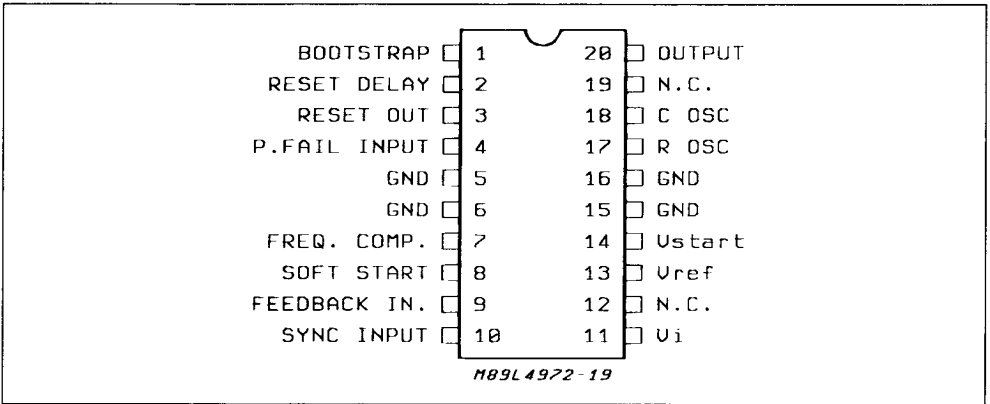
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>11</sub>	Input Voltage	55	V
V <sub>11</sub>	Input Operating Voltage	50	V
V <sub>20</sub>	Output DC Voltage	- 1	V
	Output Peak Voltage at t = 0.1μs f = 200KHz	- 5	V
I <sub>20</sub>	Maximum Output Current	Internally Limited	
V <sub>1</sub>	Bootstrap Voltage	65	V
	Bootstrap Operating Voltage	V <sub>11</sub> + 15	V
V <sub>4</sub> , V <sub>8</sub>	Input Voltage at Pins 4, 12	12	V
V <sub>3</sub>	Reset Output Voltage	50	V
I <sub>3</sub>	Reset Output Sink Current	50	mA
V <sub>2</sub> , V <sub>7</sub> , V <sub>9</sub> , V <sub>10</sub>	Input Voltage at Pin 2, 7, 9, 10	7	V
I <sub>2</sub>	Reset Delay Sink Current	30	mA
I <sub>7</sub>	Error Amplifier Output Sink Current	1	mA
I <sub>8</sub>	Soft Start Sink Current	30	mA
P <sub>tot</sub>	Total Power Dissipation at T <sub>PINS</sub> < 80°C	5	W
T <sub>j</sub> , T <sub>stg</sub>	Junction and Storage Temperature	- 40 to 150	°C

**PIN CONNECTION (top view)**



**THERMAL DATA**

			Powerdip	SO20L
Rth j-pins	Thermal Resistance Junction-pins	Max	12°C/W	15°C/W
Rth j-amb	Thermal Resistance Junction-ambient	Max	80°C/W	-

## PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A $C_{boot}$ capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
2	RESET DELAY	A $C_d$ capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30K $\Omega$ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972's are synchronized by connecting pin 13 inputs together or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	$V_{ref}$	5.1 $V_{ref}$ Device Reference Voltage
14	$V_{start}$	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	$R_{osc}$ . External resistor connected to ground determines the constant charging current of $C_{osc}$ .
18	OSCILLATOR	$C_{osc}$ . External capacitor connected to ground determines (with $R_{osc}$ ) the switching frequency.
20	OUTPUT	Regulator Output

## CIRCUIT OPERATION

The L4972 is a 2A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

## BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to  $5.1V \pm 2\%$ , soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise  $5.1V \pm 2\%$  on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by

an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor,  $C_{ss}$ , and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about  $150^{\circ}\text{C}$  and has a hysteresis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

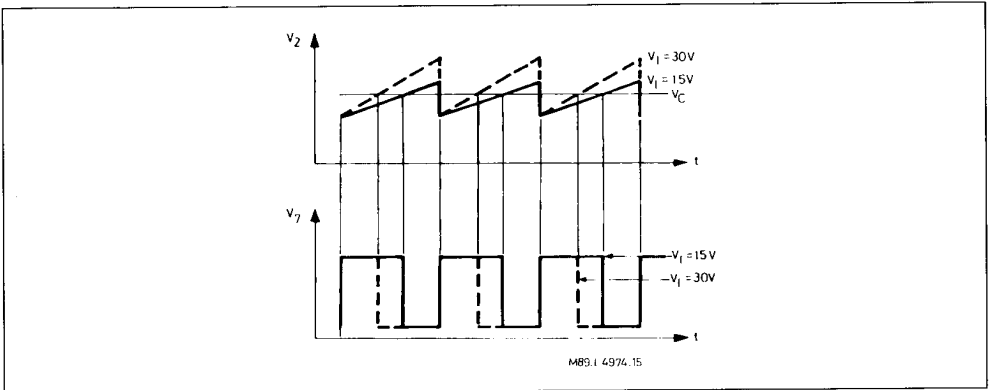


Figure 2 : Soft Start Function.

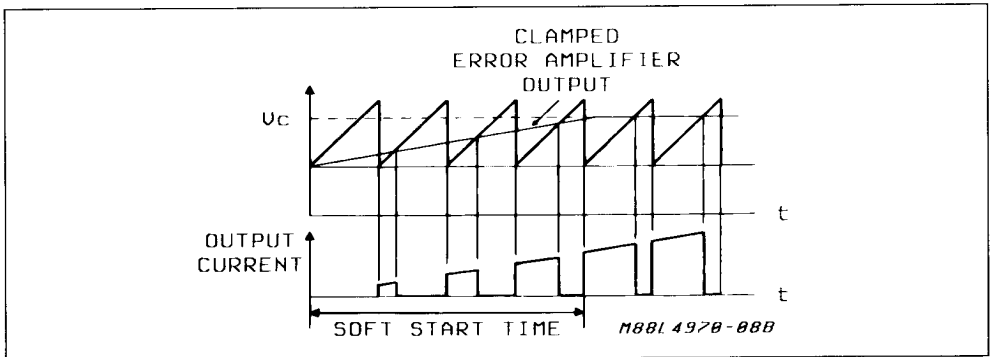


Figure 3 : Limiting Current Function.

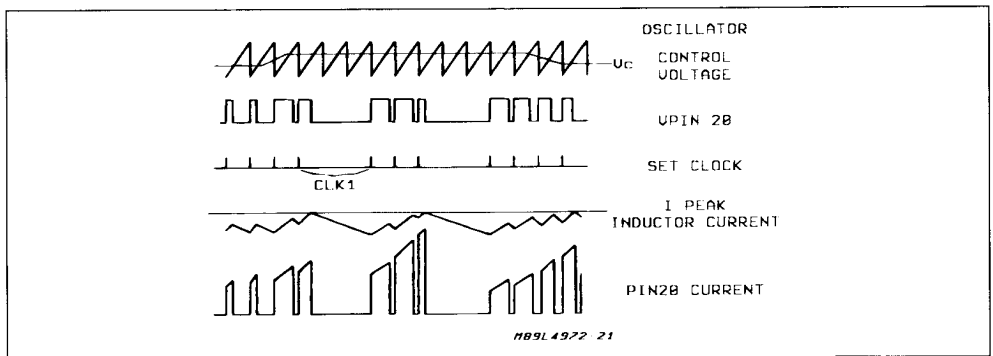
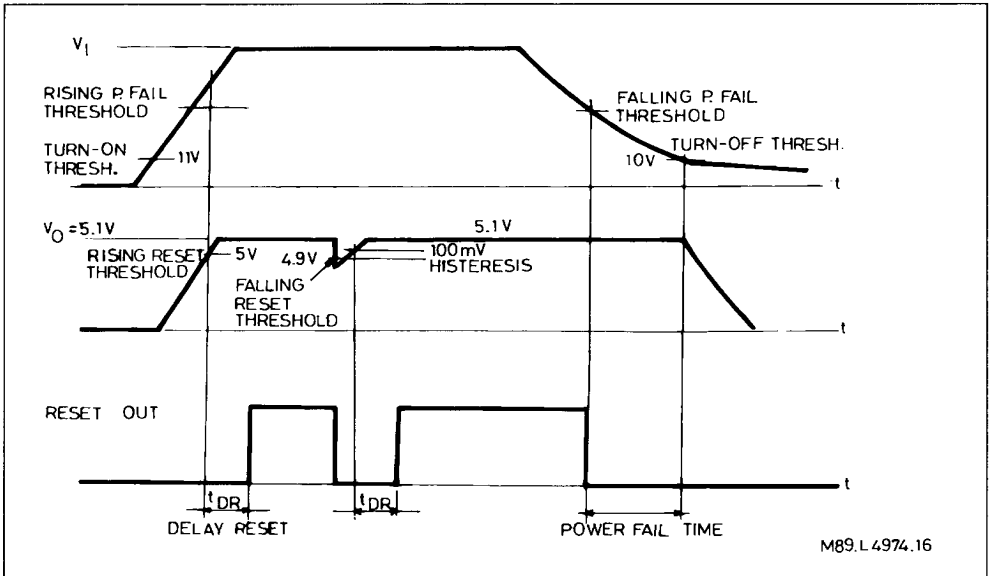
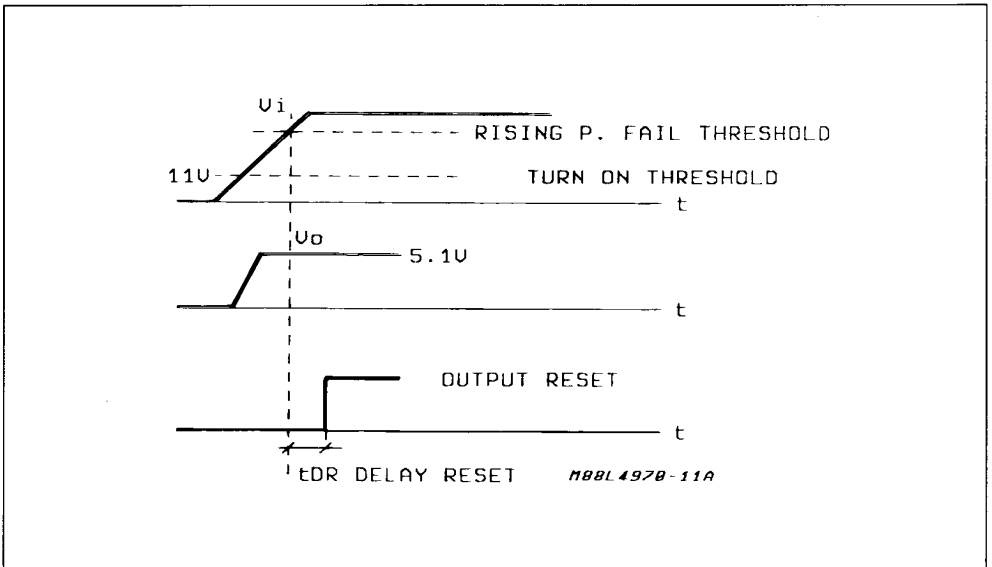


Figure 4 : Reset and Power Fail Functions.

A



B



**ELECTRICAL CHARACTERISTICS**(refer to the test circuit,  $T_j = 25^\circ\text{C}$ ,  $V_i = 35\text{V}$ ,  $R_4 = 33\text{k}\Omega$ ,  $C_9 = 2.2\text{nF}$ ,  $f_w = 100\text{kHz}$  typ, unless otherwise specified)

### DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_i$	Input Volt. Range (pin 11)	$V_o = V_{ref}$ to 40V $I_o = 2\text{A}$	15		50	V	5
$V_o$	Output Voltage	$V_i = 15\text{V}$ to 50V $I_o = 1\text{A}$ ; $V_o = V_{ref}$	5	5.1	5.2	V	5
$\Delta V_o$	Line Regulation	$V_i = 15\text{V}$ to 50V $I_o = 0.5\text{A}$ ; $V_o = V_{ref}$		12	30	mV	
$\Delta V_o$	Load Regulation	$V_o = V_{ref}$ $I_o = 0.5\text{A}$ to 2A		7	20	mV	
$V_d$	Dropout Voltage between Pin 11 and 20	$I_o = 2\text{A}$		0.25	0.4	V	
$I_{20L}$	Max Limiting Current	$V_i = 15\text{V}$ to 50V $V_o = V_{ref}$ to 40V	2.5	2.8	3.1	A	
$\eta$	Efficiency	$I_o = 2\text{A}$ , $f = 100\text{kHz}$ $V_o = V_{ref}$ $V_o = 12\text{V}$	80	85 90		%	
SVR	Supply Voltage Ripple Rejection	$V_i = 2\text{VRMS}$ ; $I_o = 1\text{A}$ $f = 100\text{Hz}$ ; $V_o = V_{ref}$	56	60		dB	5
$f$	Switching Freq.		90	100	110	kHz	5
$\Delta f/\Delta V_i$	Volt. Stability of Switching Freq.	$V_i = 15\text{V}$ to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stability of Switch. Freq.	$T_j = 0$ to $125^\circ\text{C}$		1		%	5
$f_{max}$	Max. Operating Switch. Freq.	$V_o = V_{ref}$ $R_4 = 15\text{k}\Omega$ $I_o = 2\text{A}$ $C_9 = 2.2\text{nF}$	200			kHz	5

### $V_{REF}$ SECTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{REF}$	Reference Voltage		5	5.1	5.2	V	7
$\Delta V_{REF}$	Line Regulation	$V_i = 15\text{V}$ to 50V $V_B = 0$		10	25	mV	7
$\Delta V_{REF}$	Load Regulation	$I_{REF} = 0$ to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	$T_j = 0^\circ\text{C}$ to $125^\circ\text{C}$		0.4		mV/C	7
$I_{REF}$	Short Circuit Curr. Limit	$V_{REF} = 0$		70		mA	7

### $V_{START}$ SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{ref}$	Reference Voltage	$P_B = 0\text{V}$	11.4	12	12.6	V	7
$\Delta V_{ref}$	Line Regulation	$P_B = 0\text{V}$ ; $V_i = 15$ to 50V		0.4	1	V	7
$\Delta V_{ref}$	Load Regulation	$I_{ref} = 0$ to 1mA $P_B = 0\text{V}$		50	200	mV	7
$I_{ref}$	Short Circuit Curr. Limit	$P_B = 0\text{V}$ ; $P_{14} = 0\text{V}$		80		mA	

**ELECTRICAL CHARACTERISTICS** (continued)

## DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{11on}$	Turn-on Thresh.		10	11	12	V	7A
$V_{11Hyst}$	Turn-off Hyster.			1		V	7A
$I_{11Q}$	Quiescent Current	$V_8 = 0$ ; $S1 = D$ $S2 = C$ ; $S4 = A$		10	16	mA	7A
$I_{11OQ}$	Operating Quiescent Curr.	$V_8 = 0$		16	20	mA	7A
$I_{20L}$	Out Leak Current	$V_i = 55V$ ; $S3 = A$ ; $V_8 = 0V$ ;			2	mA	7A

## SOFT START (pin 8)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$I_8$	Soft Start Source Current	$V_8 = 3V$ ; $V_9 = 0V$	70	100	130	$\mu A$	7B
$V_{8s}$	Output Saturation Voltage	$I_{8s} = 20mA$ ; $V_{11} = 10V$			0.7	V	7B

## ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{7H}$	High Level out Voltage	$I_7 = -50\mu A$ ; $S2 = A$ $P_9 = 0V$ ; $S1 = C$	6			V	7C
$V_{7L}$	Low Level out Voltage	$I_7 = 50\mu A$ ; $S2 = A$ $P_9 = 6V$ ; $S1 = C$			0.7	V	7C
$I_9$	Input Bias Current	$V_9 = 5V$ ; $S1 = B$ ; $R_S = 10K\Omega$		2	10	$\mu A$	7C
VOS	Input off Voltage	$P_9 = Vos$ ; $R_S = 50\Omega$ ; $S1 = A$		2	10	mV	7C
$G_V$	DC Open Loop Gain	$P_{VCM} = 4V$ ; $R_S = 50\Omega$ ; $S1 = A$	60			dB	7C
SVR	Supply Volt. Rejec.	$15 < V_i < 50V$	60	80		dB	7C



**ELECTRICAL CHARACTERISTICS** (continued)**RAMP GENERATOR** (pin 18)

Symbol	Parameter	Test Conditions	Min.	Typ.	max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	$V_i = 15V$ $V_i = 45V$		2.5 5.5		V V	7A
	Min Ramp Current	$S1 = A ; I_{17} = 100\mu A$		270	300	$\mu A$	7A
	Max Ramp Current	$S1 = A ; I_{17} = 1mA$	2.4	2.7		mA	7A

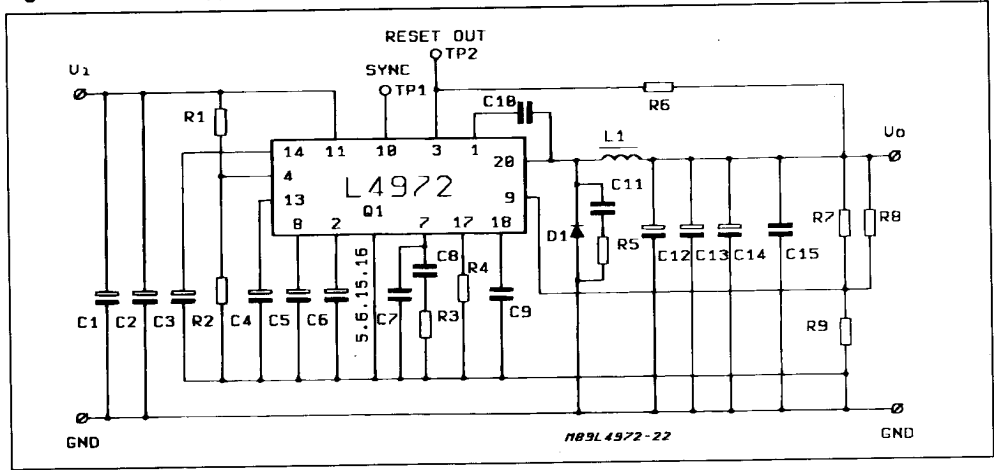
**SYNC FUNCTION** (pin 10)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	$V_i = 15$ to $50V$	- 0.3		0.9	V	
SYNC	High Input Voltage	$V_i = 0$	2.5		5.5	V	
- $I_{10L}$	Sync Input Current with Low Input Voltage	$V_{10} = 0.9V$			0.4	mA	
- $I_{10H}$	Input Current with High	$V_{10} = 2.5V$			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	$\mu s$	

**RESET AND POWER FAIL FUNCTIONS**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{9R}$	Rising Threshold Voltage (pin 9)	$V_i = 15$ to $50V$ $S1 = B$	$V_{ref} - 120$	$V_{ref} - 100$	$V_{ref} - 80$	V mV	7D
$V_{9F}$	Falling Threshold Voltage (pin 9)		4.77	$V_{ref} - 200$	$V_{ref} - 160$	V mV	7D
$V_{2H}$	Delay High Threshold Voltage	$S1 = B$	5	5.1	5.2	V	7D
$V_{2L}$	Delay Low Threshold Voltage	$S1 = B$	1	1.1	1.2	V	7D
$I_{2SO}$	Delay Source Current	$V_4 = 5.3V ; V_2 = 3V$ $S1 = A$	40	56	70	$\mu A$	7D
$I_{2SI}$	Delay SINK Current	$V_4 = 4.7V ; V_2 = 3V$ $S1 = A$	10			mA	7D
$V_{3S}$	Out Saturation Voltage	$I_3 = 15mA ; S2 = B$			0.4	V	7D
$I_3$	Output Leak Current	$V_3 = 50V ; S2 = A$			100	$\mu A$	7D
$V_{4S}$	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
$I_4$	Input Bias Current			1	3	$\mu A$	7D

Figure 5 : Test and Application Circuit.



**PART LIST**

- R<sub>1</sub> = 30K $\Omega$
- R<sub>2</sub> = 10K $\Omega$
- R<sub>3</sub> = 22K
- R<sub>4</sub> = 36K
- R<sub>5</sub> = 22 $\Omega$
- R<sub>6</sub> = 4.7K
- R<sub>7</sub> = see table A
- R<sub>8</sub> = OPTION
- R<sub>9</sub> = 4.7K

- \* C<sub>1</sub> = C<sub>2</sub> = 1000 $\mu$ F 63V EYF (ROE)
- C<sub>3</sub> = C<sub>4</sub> = C<sub>5</sub> = C<sub>6</sub> = 2,2 $\mu$ F 50V
- C<sub>7</sub> = 330pF Film
- C<sub>8</sub> = 22nF MKT 1837 (ERO)
- C<sub>9</sub> = 2.2nF KP 1830 (ERO)
- C<sub>10</sub> = 0.1 $\mu$ F Film
- C<sub>11</sub> = 1nF
- \*\* C<sub>12</sub> = C<sub>13</sub> = C<sub>14</sub> = 100 $\mu$ F 40V EKR (ROE)
- C<sub>15</sub> = 1 $\mu$ F Film

D = SBS 560 (OR EQUIVALENT)

L = 150 $\mu$ H  
 core 58310 MAGNETICS  
 45 TURNS 0.8mm (AWG 19)  
 COGEMA 949181

\* 2 capacitors in parallel to increase input RMS current capability.  
 \*\* 3 capacitors in parallel to reduce total output ESR.

**Table A.**

V <sub>0</sub>	R <sub>9</sub>	R <sub>7</sub>
12V	4.7K $\Omega$	6.2K $\Omega$
15V	4.7K $\Omega$	9.1K $\Omega$
18V	4.7K $\Omega$	12K $\Omega$
24V	4.7K $\Omega$	18K $\Omega$

Figure 6 : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available.

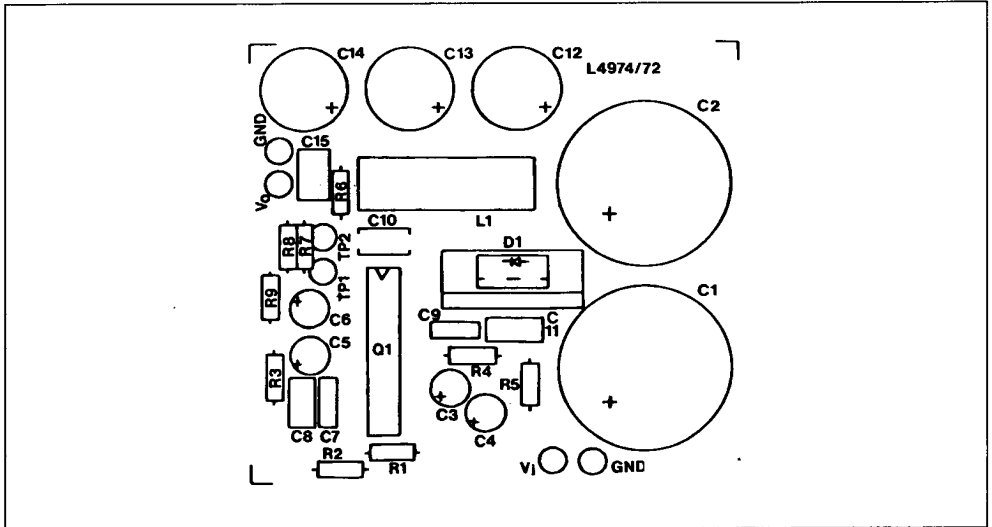


Figure 7 : DC Test Circuits.

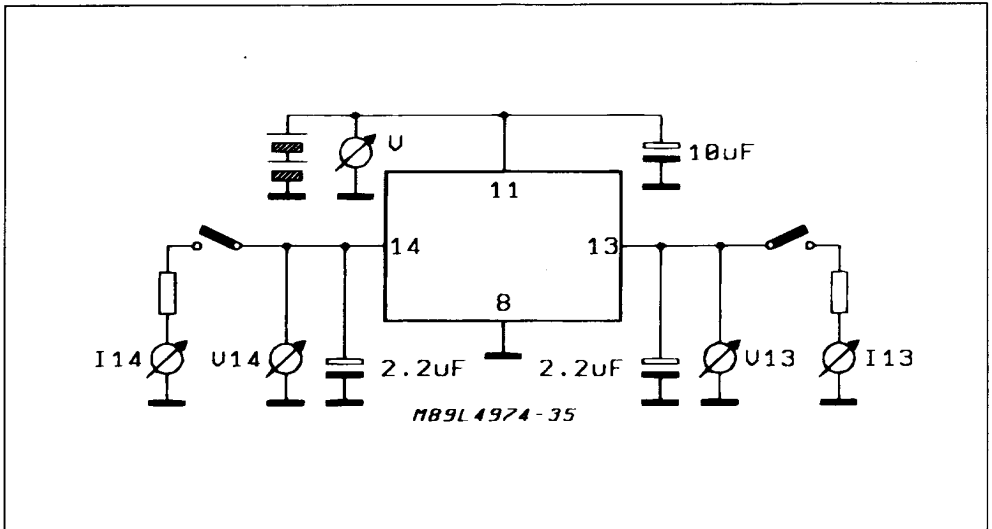


Figure 7A.

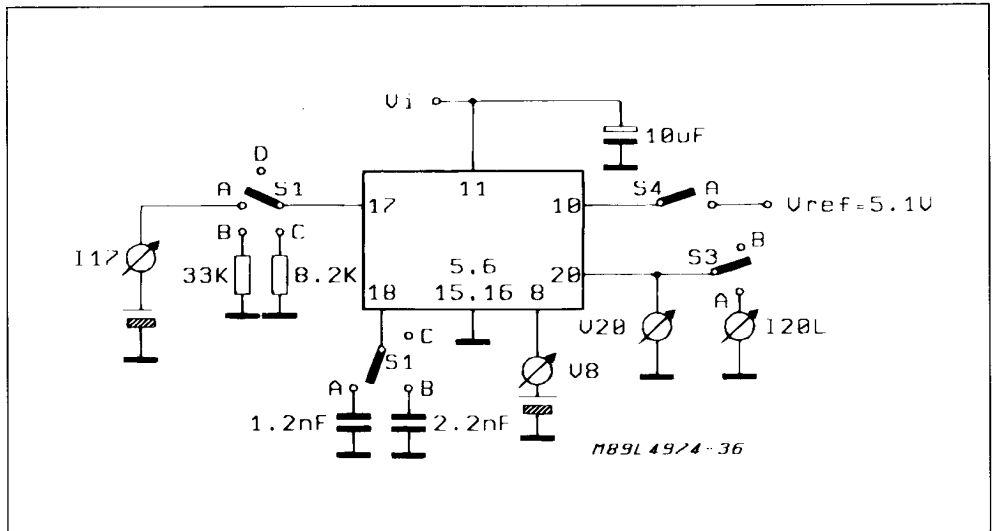
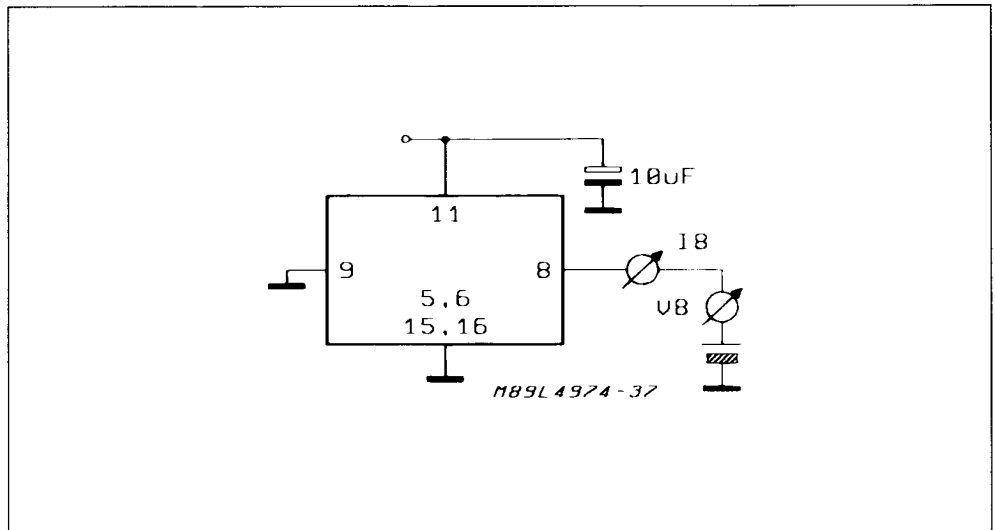
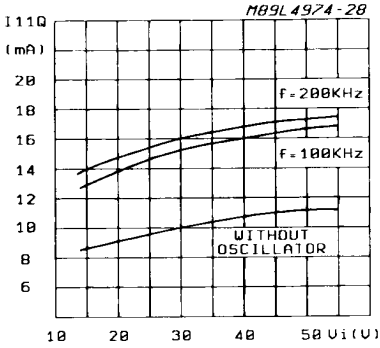


Figure 7B.

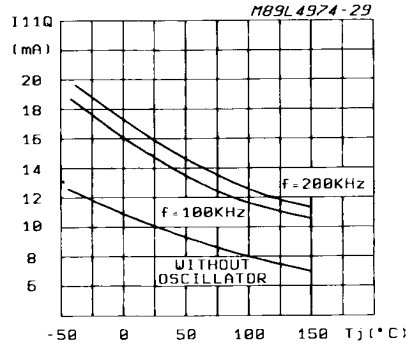




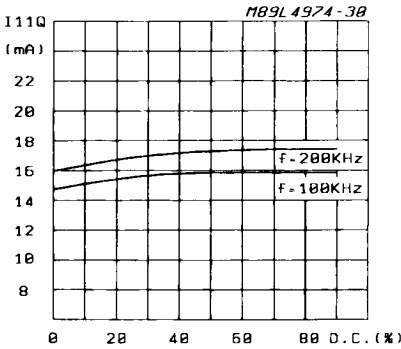
**Figure 8 :** Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).



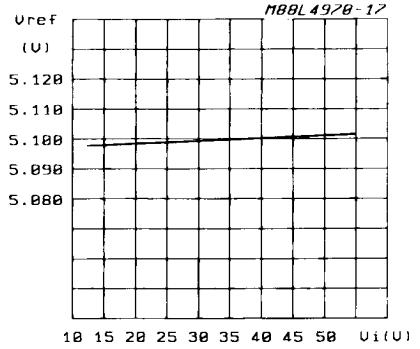
**Figure 9 :** Quiescent Drain Current vs. Junction Temperature (0% duty cycle).



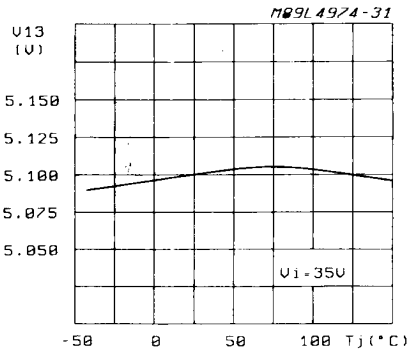
**Figure 10 :** Quiescent Drain Current vs. Duty Cycle.



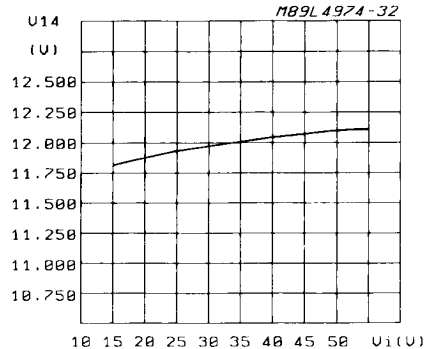
**Figure 11 :** Reference Voltage (pin 13) vs. Vi (see fig. 7).



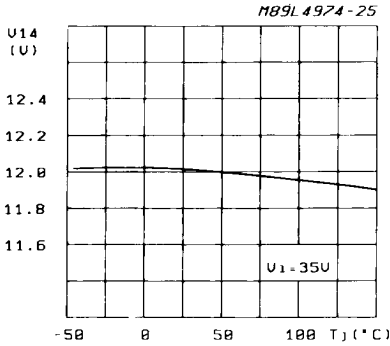
**Figure 12 :** Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).



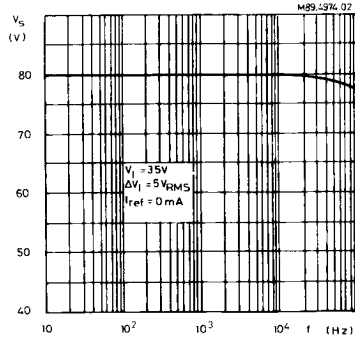
**Figure 13 :** Reference Voltage (pin 14) vs. Vi (see fig. 7).



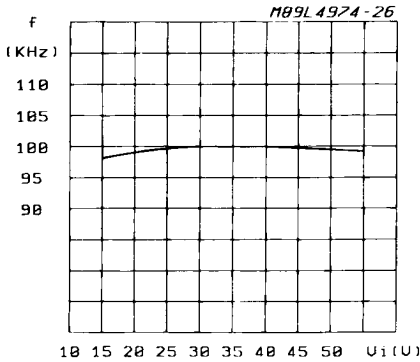
**Figure 14 :** Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).



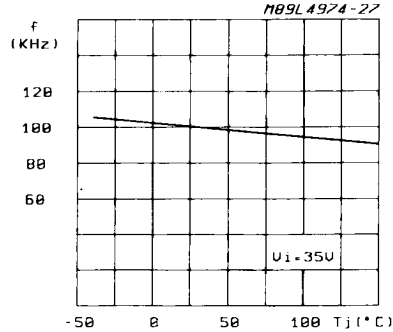
**Figure 15 :** Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Frequency.



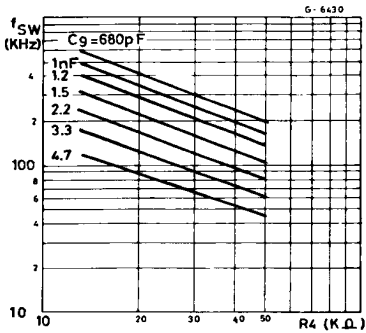
**Figure 16 :** Switching Frequency vs. Input Voltage (see fig. 5).



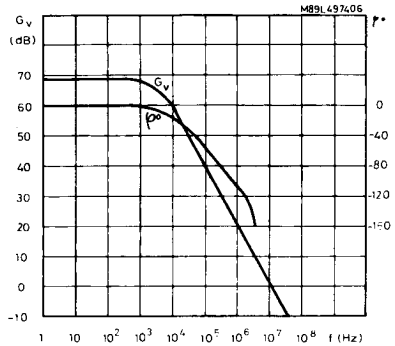
**Figure 17 :** Switching Frequency vs. Junction Temperature (see fig. 5).



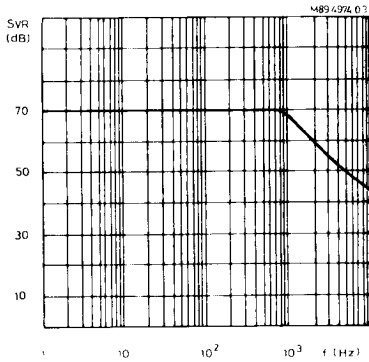
**Figure 18 :** Switching Frequency vs. R4 (see fig.5).



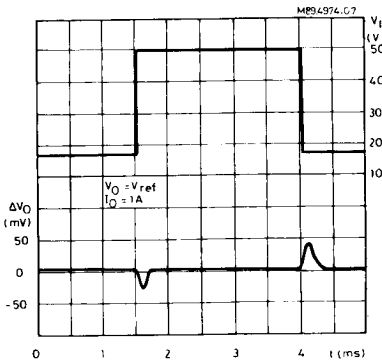
**Figure 19 :** Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).



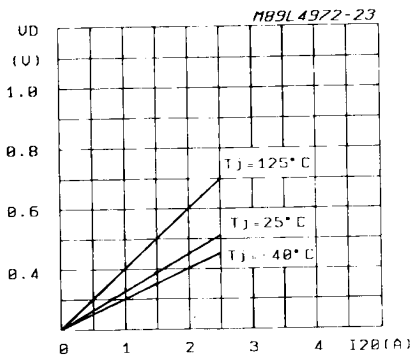
**Figure 20 :** Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).



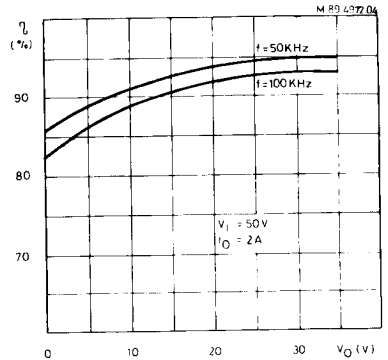
**Figure 22 :** Line Transient Response (see fig. 5).



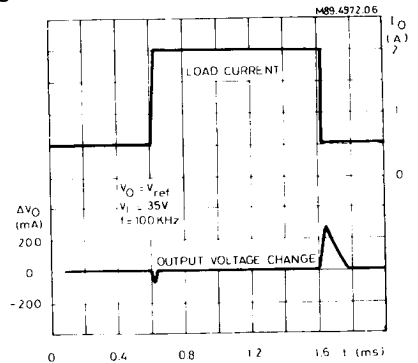
**Figure 24 :** Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.



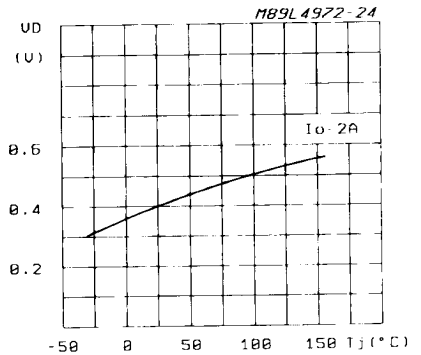
**Figure 21 :** Efficiency vs. Output Voltage.



**Figure 23 :** Load Transient Response (see fig. 5).

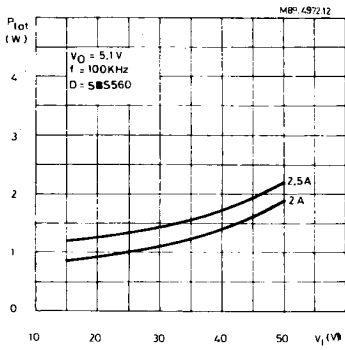


**Figure 25 :** Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

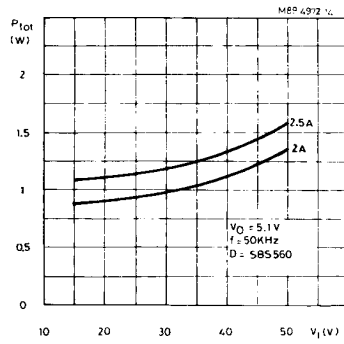




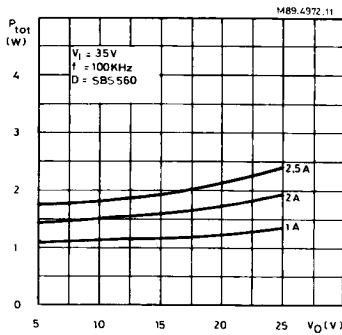
**Figure 26 : Power Dissipation (device only) vs. Input Voltage.**



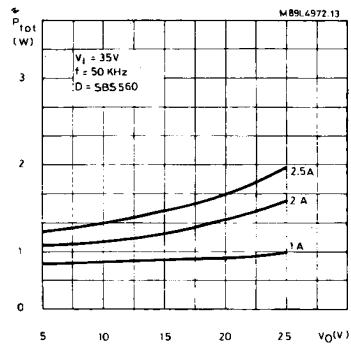
**Figure 27 : Power Dissipation (device only) vs. Input Voltage.**



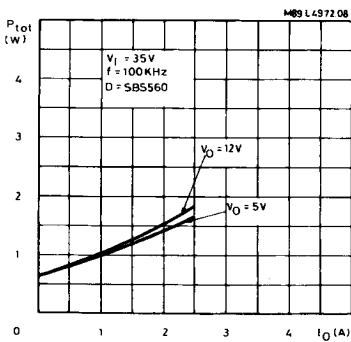
**Figure 28 : Power Dissipation (device only) vs. Output Voltage.**



**Figure 29 : Power Dissipation (device only) vs. Output Voltage.**



**Figure 30 : Power Dissipation (device only) vs. Output Current.**



**Figure 31 : Power Dissipation (device only) vs. Output Current.**

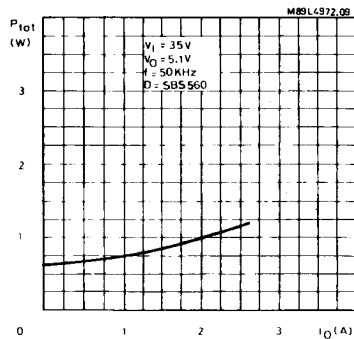


Figure 32 : Efficiency vs. Output Current.

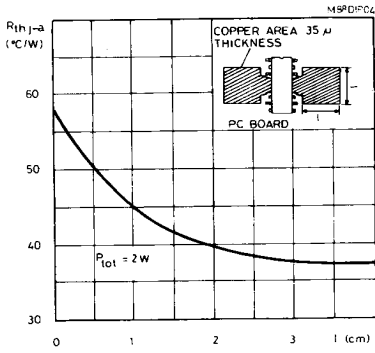


Figure 33 : Test PCB Thermal Characteristic.

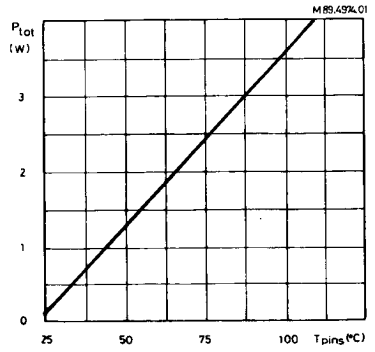


Figure 34 :  $R_{th}$  with two "on board" Square Heat Sinks vs. Side  $l$ .

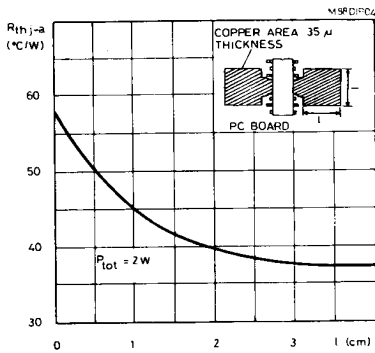
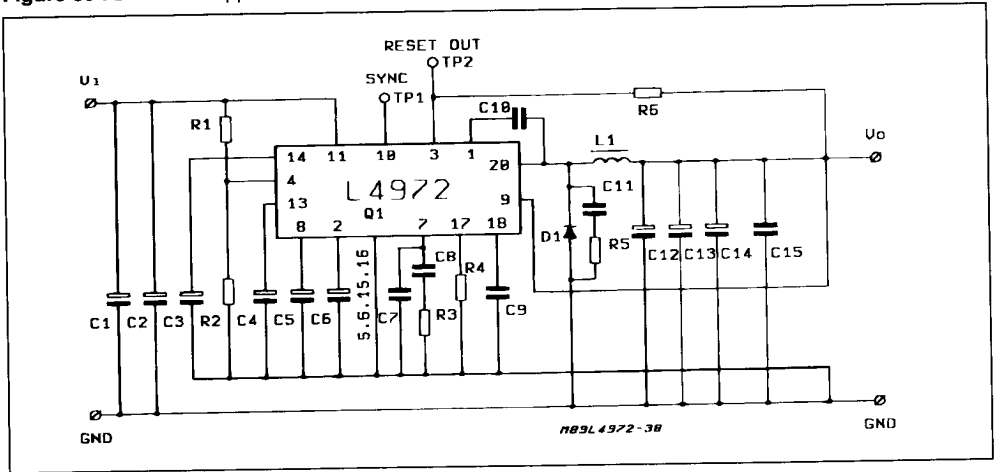


Figure 35 : 2A - 5.1V Application Circuit.



TYPICAL PERFORMANCE (using evaluation board) :

$\eta = 83\%$  ( $V_i = 35V$  ;  $V_o = V_{REF}$  ;  $I_o = 2A$  ;  $f_{sw} = 100KHz$ )

$V_o$  RIPPLE = 30mV (at 1A)

Line regulation = 12mV ( $V_i = 15$  to 50V)

Load regulation = 7mV ( $I_o = 0.5A$ ,  $I_o = 0.5 - 2A$ )

for component values Refer to the fig. 5 (Part list).

Figure 36 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972 and L4970.

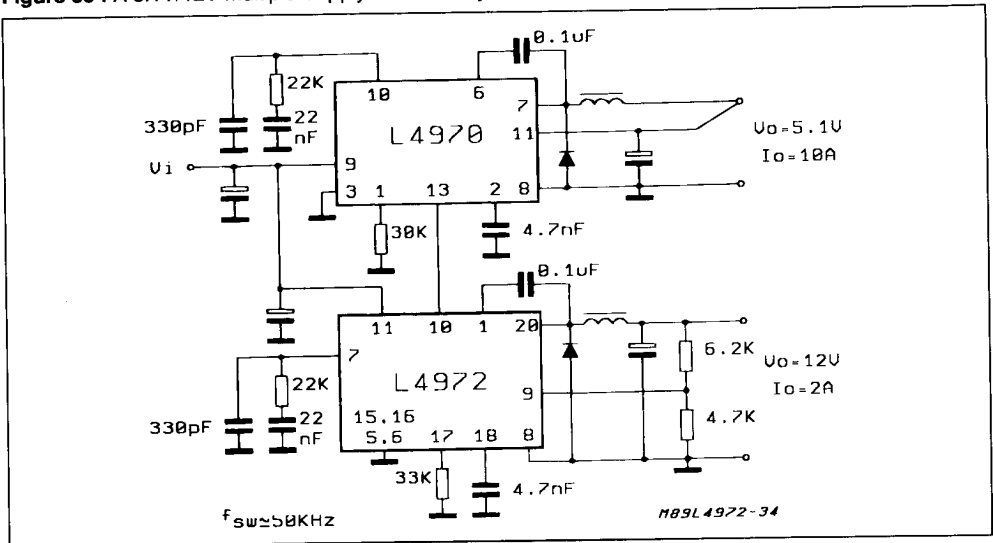


Figure 37 : L4972's Sync. Example.

