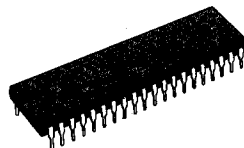


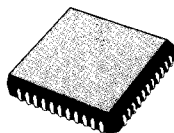
MULTI MODE MODEM ANALOG FRONT-END

ADVANCE DATA

- 12 BIT A/D AND D/A CONVERTERS WITH PROGRAMMABLE SAMPLING FREQUENCY : 7.2, 8.0, OR 9.6 kHz
- 6 TH ORDER SWITCHED CAPACITOR TRANSMIT FILTER
- TRANSMIT ATTENUATOR PROGRAMMABLE FROM 0 dB TO 22 dB WITH 2 dB STEP
- DUPLEXER OUTPUT AVAILABLE WITH PROGRAMMABLE ATTENUATION
- 15 TH ORDER SWITCHED CAPACITOR Rx FILTER (PROGRAMMABLE)
- TWO PROGRAMMABLE GAIN Rx AMPLIFIERS : FROM 0 dB TO 9 dB WITH 3 dB STEP BEFORE Rx FILTER AND FROM 0 dB TO 46.5 dB WITH 1.5 dB STEP AFTER Rx FILTER
- PROGRAMMABLE CARRIER LEVEL DETECTOR
- ON CHIP ANTI-ALIASING CELLS (TRANSMIT AND RECEIVE)
- TWO INDEPENDANT TRANSMIT AND RECEIVE DIGITAL PHASE LOCKED LOOPS (DPLLs)
- TERMINAL CLOCK INPUT FOR TRANSMIT SYNCHRONIZATION
- THREE AVAILABLE OUTPUT CLOCKS : BIT, BAUD AND CONVERSION CLOCKS
- DSP INTERFACE THROUGH 8 BIT STANDARD BUS FOR BOTH SIGNAL SAMPLES AND CONTROL REGISTER ACCESS
- AUTOMATIC RESET ON POWER-ON
- ± 5 V POWER SUPPLY
- 250 mW TYPICAL POWER CONSUMPTION



P
DIP40
 (Plastic Package)



FN
PLCC44
 (Plastic Package)

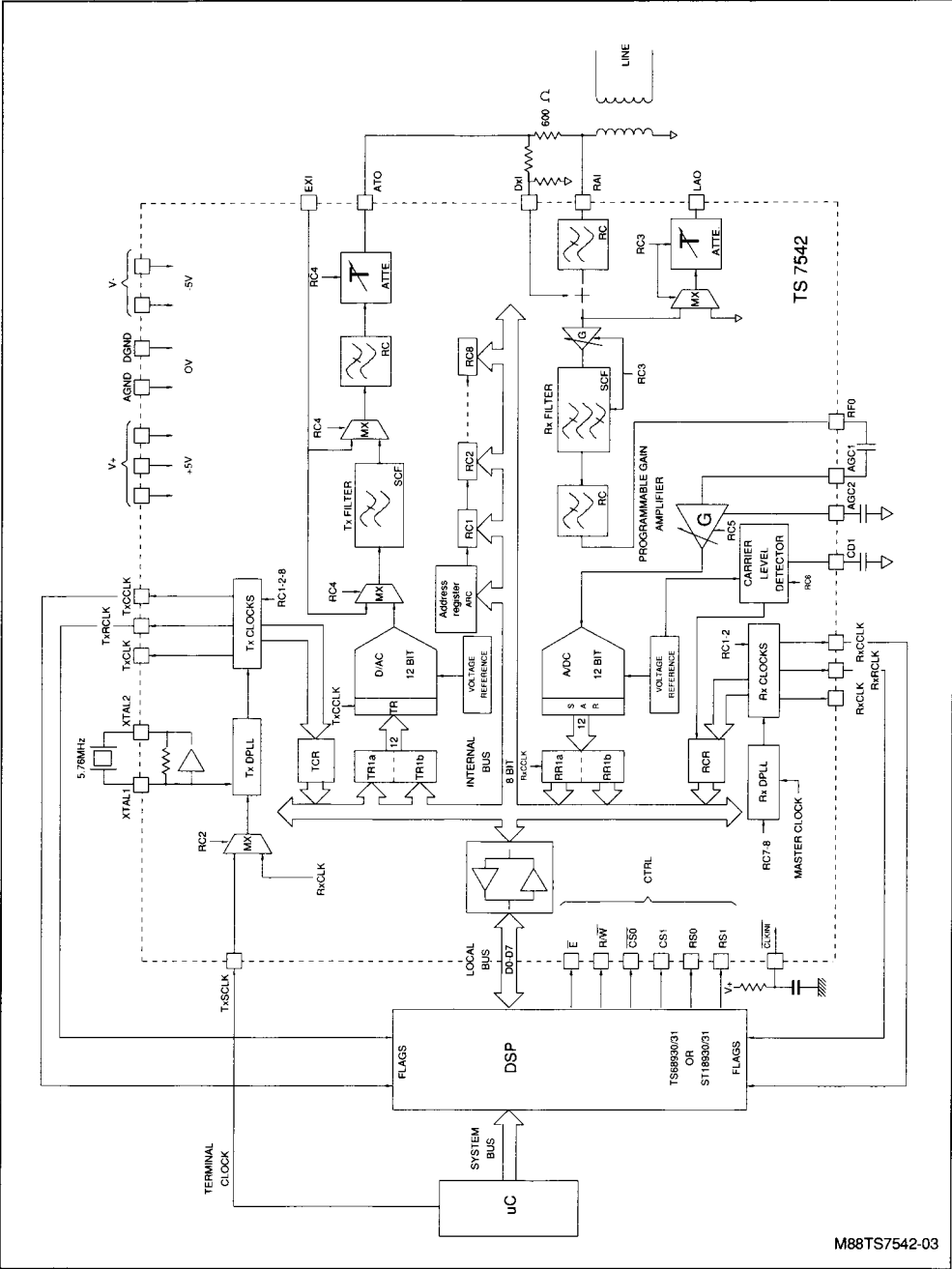
DESCRIPTION

The TS7542 is a single-chip analog front-end designed to implement high-performance voice-grade MODEMS. Associated with a Digital Signal Processor such as TS68930/31 or ST18930/31, it provides a cost-effective and powerful solution for implementation of multi-mode modems including CCITT V.21, V.22, V.22bis, V.23, V.26, V.27, V.29, V.33 and BELL 103, 202 and 212 A standards.

ORDERING INFORMATION

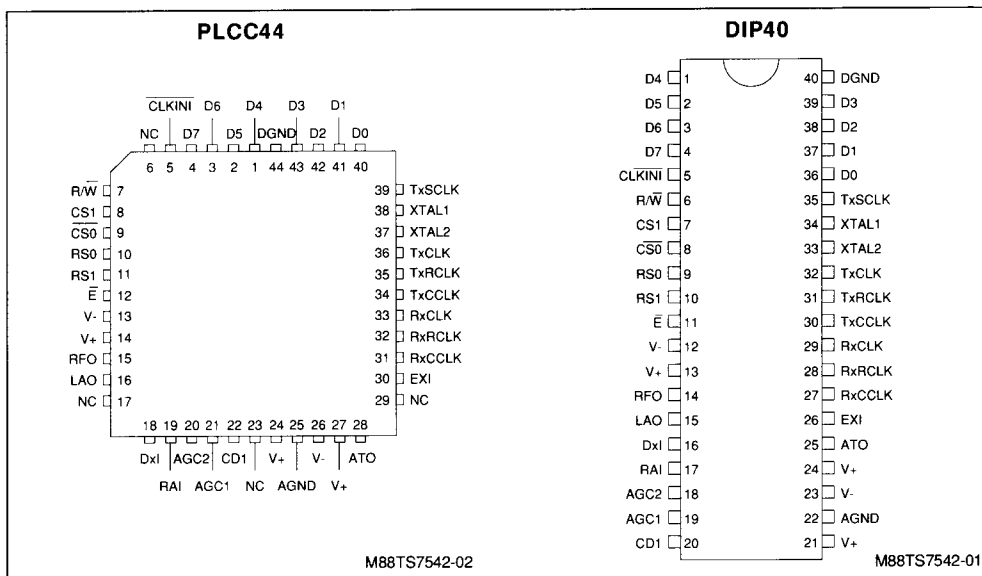
| Part Number | Temperature Range | Package |
|------------------|-------------------|---------|
| TS7542CP | 0 to 70 °C | DIP 40 |
| TS7542CFN | 0 to 70 °C | PLCC 44 |

BLOCK DIAGRAM



M88TS7542-03

PIN CONNECTIONS



PIN DESCRIPTION

| N° | Name | Description |
|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-4 | D4-D7 | Bidirectional Data Bus |
| 5 | CLKINI | Clock Initialization Input. Must be tied to V ⁺ during normal operation. |
| 6 | R/W | Read/Write Selection Input. This input indicates whether the current bus cycle is a read (high) or write (low) cycle. |
| 7-8 | CS1-CS0 | Chip Select Inputs. The chip is selected when CS0 = 0 and CS1 = 1. |
| 9-10 | RS0-RS1 | Register Select Inputs. Select the register involved in a read or write operation. |
| 11 | E | Enable Input. Enables selection inputs. Active on a low level for read operation. Active on a positive-going edge for write operation. |
| 12 | V ⁻ | Negative Supply Voltage. V ⁻ = - 5 V ± 5 % |
| 13 | V ⁺ | Positive Supply Voltage. V ⁺ = + 5 V ± 5 % |
| 14 | RFO | Receive Filter Analog Output. Designed to be connected to AGC1 input through a 1μF non polarized capacitor. |
| 15 | LAO | Line Attenuator Output. Duplexer analog output useful for line monitoring during call progress. |
| 16 | Dxl | Duplexer Input. Signal on that analog input will be subtracted from the receive anti-aliasing filter output to implement duplexer function. |
| 17 | RAI | Receive Analog Input. Analog input tied to the transmission line. |
| 18 | AGC2 | This pin must be connected to the analog ground through a 1μF non polarized capacitor, in order to cancel the offset voltage of the AGC amplifier. |
| 19 | AGC1 | Analog input of the AGC amplifier and of the carrier level detector. |

PIN DESCRIPTION (continued)

| | | |
|-------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20 | CD1 | This pin must be connected to the analog ground through a 1 μ F non polarized capacitor, in order to remove the offset voltage of the carrier level detector amplifier. |
| 21 | V ⁺ | Positive Power Supply Voltage |
| 22 | AGND | Analog Ground. All analog signals are referenced to this pin. |
| 23 | V ⁻ | Negative Supply Voltage |
| 24 | V ⁺ | Positive Supply Voltage |
| 25 | ATO | Analog Transmit Output. Capable of driving 1200 Ω load with 5 V peak to peak amplitude. |
| 26 | EXI | External Transmit Input. Can be programmed to be connected to the transmit filter or to the transmit attenuator input. |
| 27 | RxCCLK | Receive Conversion Clock Output |
| 28 | RxRCLK | Receive Baud Rate Clock Output |
| 29 | RxCLK | Receive Bit Rate Clock Output |
| 30 | TxCCLK | Transmit Conversion Clock Output |
| 31 | TxRCLK | Transmit Baud Rate Clock Output |
| 32 | TxCLK | Transmit Bit Rate Clock Output |
| 33 | XTAL2 | Crystal Oscillator Output. Nominal Frequency = 5.76 MHz. |
| 34 | XTAL1 | Crystal Oscillator or External Master Clock Input |
| 35 | TxSCLK | Transmit Synchronization Clock Input. Can be connected to an external terminal clock to phase lock the internal transmit clocks. When this pin is tied to a permanent logical level the transmit DPLL free-runs or can be phase locked on the receive clock system. |
| 36-39 | D0-D3 | Bidirectional Data Bus |
| 40 | DGND | Digital Ground. All digital signals are referenced to this pin. |

FUNCTIONAL DESCRIPTION

The TS7542 is generally used in conjunction with a DSP to realize the "data-pump" function of a high-speed modem. The circuit communicates with the DSP via an 8-bit bidirectional bus and mainly includes the following functions :

- the transmit analog channel with the D/A Converter, the transmit filter and the transmit attenuator.
- the receive analog channel with the local echo subtractor, the receive filter, the AGC amplifier, the A/D converter and the carrier level detector.
- the two independent transmit and receive clock generators using Digital Phase Locked Loops (DPLL).
- the 15 registers used to store the 12-bit transmit and receive digital samples, digital information for the DSP like the clock and the carrier level detector status, and the data needed to control the programmable functions or to synchronize the DPLLs.

TRANSMIT CHANNEL

The transmit channel converts the digital transmit signal coming from the DSP into the analog signal to be transmitted on the phone line. It includes a 12 bit digital to analog converter (DAC) operating at 7200, 8000 or 9600 samples per second according to the supported standard and the signal processing compromises made in the DSP. The maximum analog output signal amplitude is 5 V peak to peak, defined by the internal ± 2.5 V voltage reference. The DAC is monotonic and provides a guaranteed integral linearity better than 9 bit.

The transmit filter is a 6th order low-pass switched capacitor filter (SCF) sampled at 288 kHz, whose cut-off frequency is 3.2 kHz. As the Sin x/x correction depends on the DAC sampling frequency, it has not been included in the transmit filter and must be performed by the DSP. The transmit filter is followed by a second order, continuous time low-pass filter

that removes the residual high frequency parasitic signals.

The transmit attenuator allows the transmit signal gain to be programmed from 0 dB to -22 dB with 2 dB steps. Infinite attenuation is also programmable. The output amplifier can directly drive a 1200 Ω load. For special applications, the EX1 input can be programmed to give access to the input of the transmit filter or to the input of the attenuator.

RECEIVE CHANNEL

The receive channel begins with a second order continuous time anti-aliasing filter followed by a subtractor used to implement the two-wire to four-wire conversion with few external components. The receive signal is then directed to the receive filter input and also, after programmable attenuation, to the LAO output for line monitoring purpose during call progress. Attenuation can be 0 dB, 6 dB, 12 dB or infinite. The receive switched capacitor bandpass filter is composed of three programmable sections : A 5th order low-pass section, a 4th order optional 1800 Hz notch section and a 6th order high-pass section. It also includes an input pre-filtering gain programmable from 0 dB to 9 dB with 3 dB steps. This feature is useful to optimize the dynamic range of the signal by setting the maximum receive level value close to 5 V peak to peak. The transfer function of the receive low-pass and high-pass filter sections can be translated by changing their sampling clock frequencies to support different communication standards. Ten modes are programmable to comply with CCITT V.21, V.22, V.22 bis, V.23, V.26,

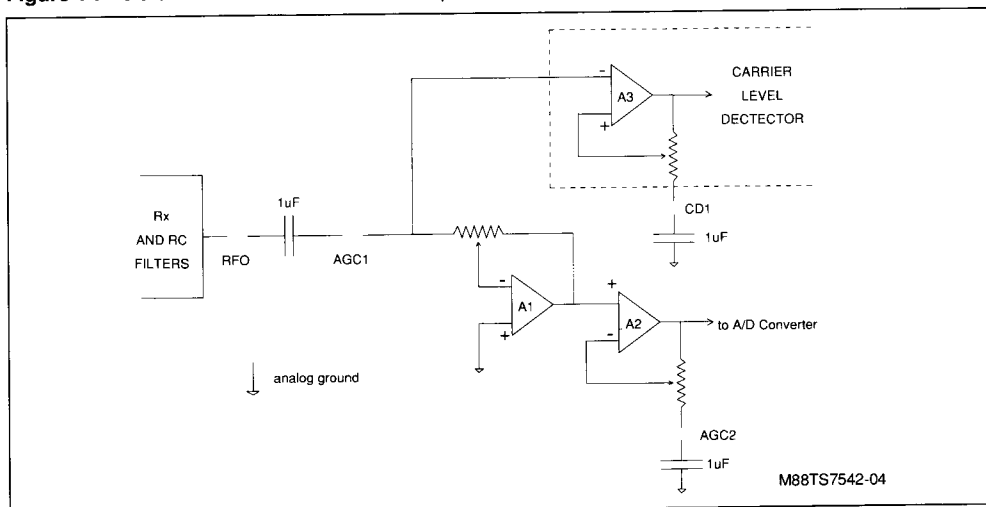
V.27, V.29 or V.33 as well as BELL 103, 202 or 212A. The typical curves obtained are given in the TRANSMISSION CHARACTERISTICS section of the data sheet. The receive filter output is smoothed in a continuous time low-pass filter and then directed to the automatic gain control (AGC) amplifier programmable from 0 dB to 46.5 dB with 1.5 dB steps. The same signal is also connected to the carrier level detector input. Three external capacitors are needed to eliminate the offset voltage as indicated in Fig.1. The residual DC level at the analog to digital converter (ADC) input is kept low and independent of the selected gain.

The carrier level detector performs the comparison between the full wave rectified receive signal and programmable threshold voltage nominally equivalent to -45.5 dBm, -34.4 dBm or -28.6 dBm with a 2.5 dB hysteresis. The binary result of the comparison can be read by the DSP. The nominal response time of the carrier level detector to a signal settlement or removal is 1.78 ms. The receive signal delivered by the AGC amplifier is sampled and converted from analog to digital by a 12-bit monotonic A/D converter whose integral linearity is guaranteed better than 9 bit. The sampling frequency is the same as that programmed for the transmit DAC i.e. 7200, 8000, or 9600 samples per second.

CLOCK GENERATION

The 5.76 MHz master clock is obtained from either a crystal tied between XTAL1 and XTAL2 pins or an external generator connected to the XTAL1 pin. In the latter case the XTAL2 pin should be left open.

Figure 1 : AGC and Carrier Level Detector Amplifier Structure.



To meet the CCITT recommendation, the frequency tolerance requirement of the master clock must be better than ± 100 ppm. The different transmit (Tx) and receive (Rx) clocks are derived from the master clock via two independent digital phase locked loops (DPLL).

TRANSMIT CLOCKS

As shown in Fig.2 the transmit DPLL operates by adding or subtracting pulses to a 2.88 MHz internal clock at a rate of 600 Hz. Consequently the frequency capture range equals $\pm 600 \text{ Hz} / 2.88 \text{ MHz}$, i.e. ± 208 ppm, a value consistent with the worst case synchronization of two independent signals having ± 100 ppm of frequency accuracy. When V.27 clocks are selected, the DPLL up-dating rate is increased to 800 Hz which is a submultiple of the 1600 baud rate of that particular mode. In this case the frequency capture range is ± 278 ppm.

The transmit DPLL can be synchronized on an external terminal clock connected to the TxSCLK input or on the receive bit clock R x CLK internally generated from the receive DPLL. It can also free-run without any phase shift.

The TS7542 delivers three synchronous transmit clocks :

- a bit clock T x CLK whose frequency equals the bit rate of the MODEM
- a baud clock T x RCLK whose frequency equals the baud rate of the MODEM
- a conversion clock T x CCLK that gives the sampling frequency of the transmit D/A converter

The frequencies of these three clocks are programmable to support the different MODEM modes. Their duty cycle is exactly 1 : 2. These clocks are available on three dedicated pins. Their status can also be read by the DSP from an internal register, TCR. Resetting of all the transmit clock generator counters on the next negative transition of T x SCLK or R x CLK can be controlled from the data bus.

RECEIVE CLOCKS

The receive DPLL phase shifts are performed in two ways :

- a coarse phase lag is obtained by suppressing several 5.76 MHz master clock pulses from the input of the receive clock generator under the control of the DSP. The number of suppressed pulses is programmable from 20 to 4800 with a step value of 20 or 300. That feature will be used to quickly synchronize the receive DPLL on the recovered receive rate.
- a fine phase lead or lag is obtained by adding or suppressing two master clock pulses from the receive clock generator input, like for the transmit DPLL. But in that case the shifts are controlled by the DSP that also implements the phase comparator of the phase locked loop.

The TS7542 delivers three receive clocks with the same nominal frequency values as their transmit counterparts :

- a bit clock R x CCLK
- a baud clock R x RCLK
- a conversion clock R x CCLK

The status of these clocks can also be read from an internal register, RCR.

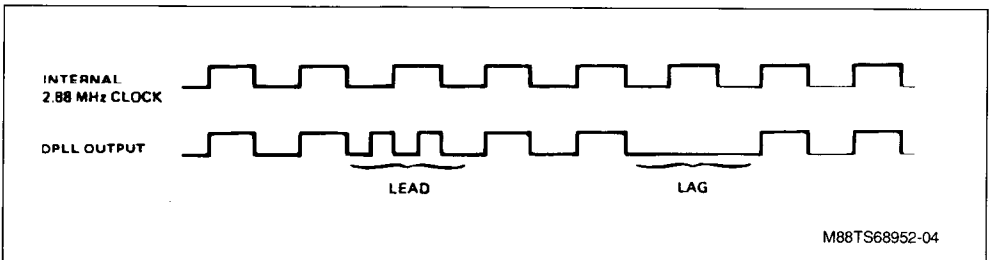
The receive and transmit clocks are plesiochronous.

INTERNAL REGISTERS

The 8-bit bidirectional data bus allows to access 15 internal registers as detailed in Fig.3. The data transfers are controlled by the six following signals :

- two chip select inputs $\overline{\text{CS0}}$ and CS1 that must be put respectively to 0 and 1 to allow a data transfer.
- The read/write input $\text{R}/\overline{\text{W}}$ that defines the transfer direction
- Two register select input that address one out of four registers for a read or a write operation. Actually indirect addressing is used to extend to eight the number of the control registers.

Figure 2 : DPLL Lead and Lag.



- The enable input \bar{E} that strobes on its positive going transition the data to be written, or that enables on its low level state the output buffers when a data is to be read from a register.

The timing diagram of the data transfers is given in the TIMING SPECIFICATIONS section of the data sheet.

The four registers only accessible in a write operation are :

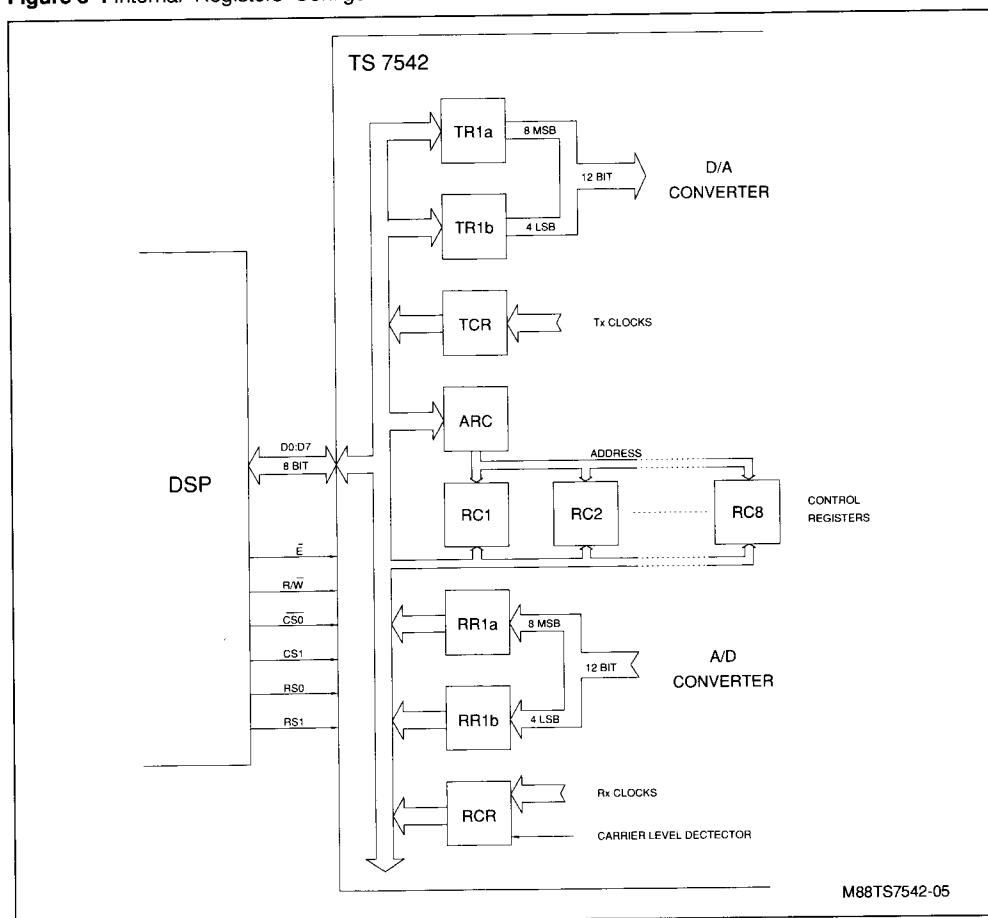
- TR1a that stores the 8 most significant bit (MSB) of the 12-bit transmit signal digital samples.
- TR1b that stores the 4 least significant bit (LSB) of the transmit signal digital samples.
- ARC that stores the 3-bit address of one out of eight control registers.

- The control register whose address is stored in the ARC register. The content of ARC is automatically incremented after each access to a control register. This allows cyclical access to these registers.

The four registers only accessible in a read operation are :

- RR1a that stores the 8 MSB of the 12-bit receive signal digital samples
- RR1b that stores the 4 LSB of the 12-bit receive signal digital samples
- RCR that stores the receive clock and the carrier level detector status
- TCR that stores the transmit clock status

Figure 3 : Internal Registers Configuration.



The addresses of the internal registers are given in table 1. Table 2 shows the formats used for the digital signal samples stored in the TR1a/b registers, the RR1a/b registers and for the status data stored

in the TCR and RCR registers. Table 3 summarizes the address and data format of the 8 control registers whose function is detailed in the PROGRAM-MABLE FUNCTIONS section.

Table 1.

| R/W | RS0 | RS1 | Accessed Register | Comment |
|-----|-----|-----|---------------------------------------|----------------------|
| 0 | 0 | 0 | TR1b | Write Only Registers |
| 0 | 0 | 1 | TR1a | |
| 0 | 1 | 0 | ARC | |
| 0 | 1 | 1 | The Control Register Addressed by ARC | |
| 1 | 0 | 0 | RR1b | Read Only Registers |
| 1 | 0 | 1 | RR1a | |
| 1 | 1 | 0 | RCR | |
| 1 | 1 | 1 | TCR | |

Table 2.

| Register Name | Register Content(note 1) | | | | | | | | Comment |
|---------------|--------------------------|--------|--------|--------|-----|-----|-----|-----|------------------------------------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| TR1a | Tx11 | Tx10 | Tx9 | Tx8 | Tx7 | Tx6 | Tx5 | Tx4 | |
| TR1b | Tx3 | Tx2 | Tx1 | Tx0 | X | X | X | X | |
| RR1a | Rx11 | Rx10 | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | |
| RR1b | Rx3 | Rx2 | Rx1 | Rx0 | 0 | 0 | 0 | 0 | |
| TCR | X | TxRCLK | TxCCLK | TxCCLK | X | X | X | X | |
| RCR | CDL | RxRCLK | RxCCLK | RxCCLK | X | X | X | X | CDL = 1 if Rx signal is greater than the programmed level. |

X = Don't care.
Note 1 :D0 to D7 refer to the data bus pins and gives the bit position in the read or written data.

Table 3.

| Control Register Name | ARC Content (address) (note 1) | | | Register Content (note 2) | | | | | | | | Programmed Function |
|-----------------------|--------------------------------|----|----|---------------------------|------|------|------|------|------|------|------|----------------------------------------------------|
| | D7 | D6 | D5 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| RC1 | 0 | 0 | 0 | HB3 | HB2 | HB1 | HR2 | HR1 | X | X | X | Bit/Baud Rate for Tx and Rx Clocks |
| RC2 | 0 | 0 | 1 | X | X | X | HS2 | HS1 | HTHR | FCLK | X | Conversion Frequency. Tx Synchronization Selection |
| RC3 | 0 | 1 | 0 | RF3 | RF2 | RF1 | REJ | RFG2 | RFG1 | LAT2 | LAT1 | Rx Filter and 1800Hz Notch. LAO Attenuation |
| RC4 | 0 | 1 | 1 | ATT4 | ATT3 | ATT2 | ATT1 | X | EM2 | EM1 | X | Tx Attenuation. EXI Input. |
| RC5 | 1 | 0 | 0 | RG5 | RG4 | RG3 | RG2 | RG1 | X | X | X | AGC Amplifier Gain |
| RC6 | 1 | 0 | 1 | CDG2 | CDG1 | CDH | X | X | X | X | X | Carrier Level Detector Gain and Hysteresis |
| RC7 | 1 | 1 | 0 | SP5 | SP4 | SP3 | SP2 | SP1 | X | X | X | RxDPLL Coarse Phase Shift |
| RC8 | 1 | 1 | 1 | MPE | SPR | AVRE | VAL | X | X | X | X | TxDPLL Reset. Rx DPLL Fine Phase Shifts. |

X = Don't care value.

Note 2 : D0 to D7 refers to the data bus pins and gives the bit position in the loaded address or data.

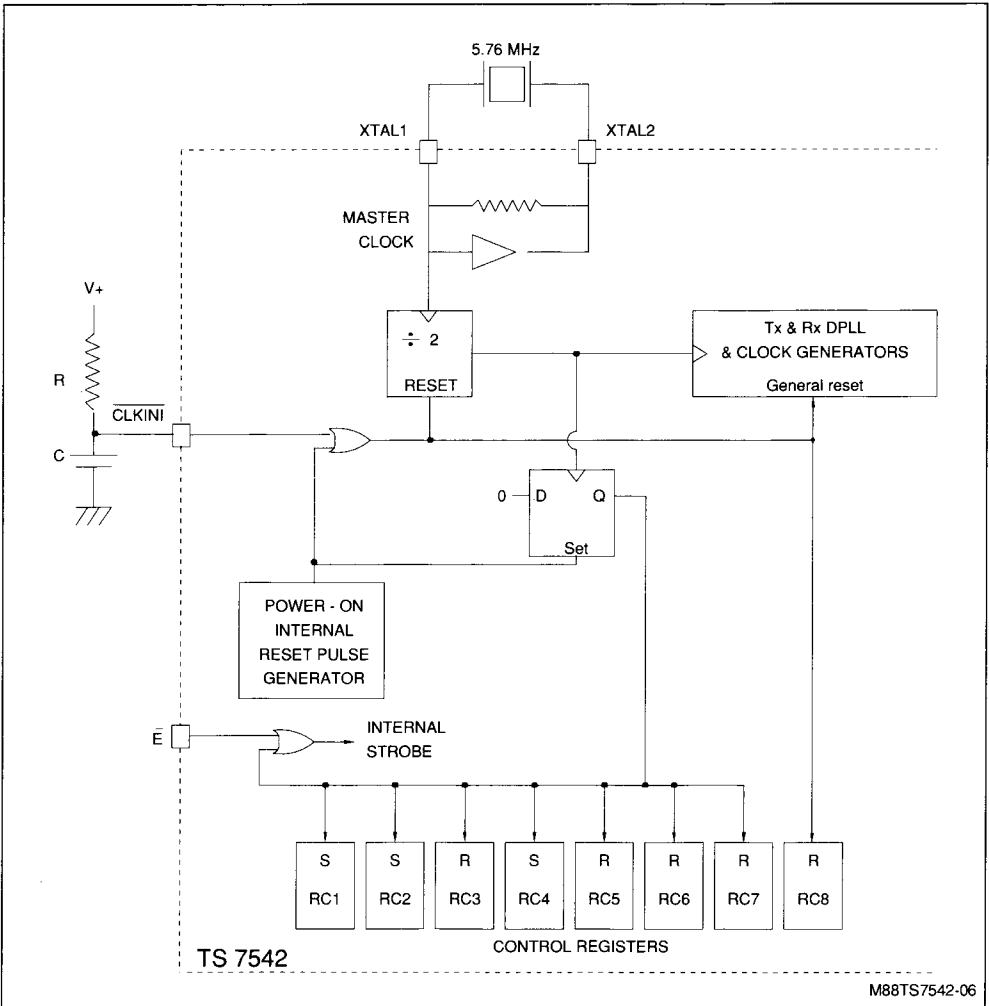
POWER-ON INITIALIZATION

Internal power-on circuitry (Fig.4) automatically resets the DPLL and the clock generators counters, and initializes the RC1 to RC8 control registers. The initial status of these registers are given in the PROGRAMMABLE FUNCTIONS section. The transmit attenuator is initialized to an infinite attenuation in order to avoid the transmission of undesirable signals on the phone line.

Access to the control registers is disabled during power-on reset until the clock oscillator starting. The

reset time duration can be increased by connecting the CLKINI input to an external RC timer as indicated in Fig.4. That feature will prevent, in particular applications, possible problems due to incontrolled signals coming from the DSP during power-on. In normal operation the CLKINI input can be used to reset the DPLL and clock generator counters and the RC8 control register. When that pin as not used, it must be tied to V⁺

Figure 4 : Power-on Initialization Circuitry.

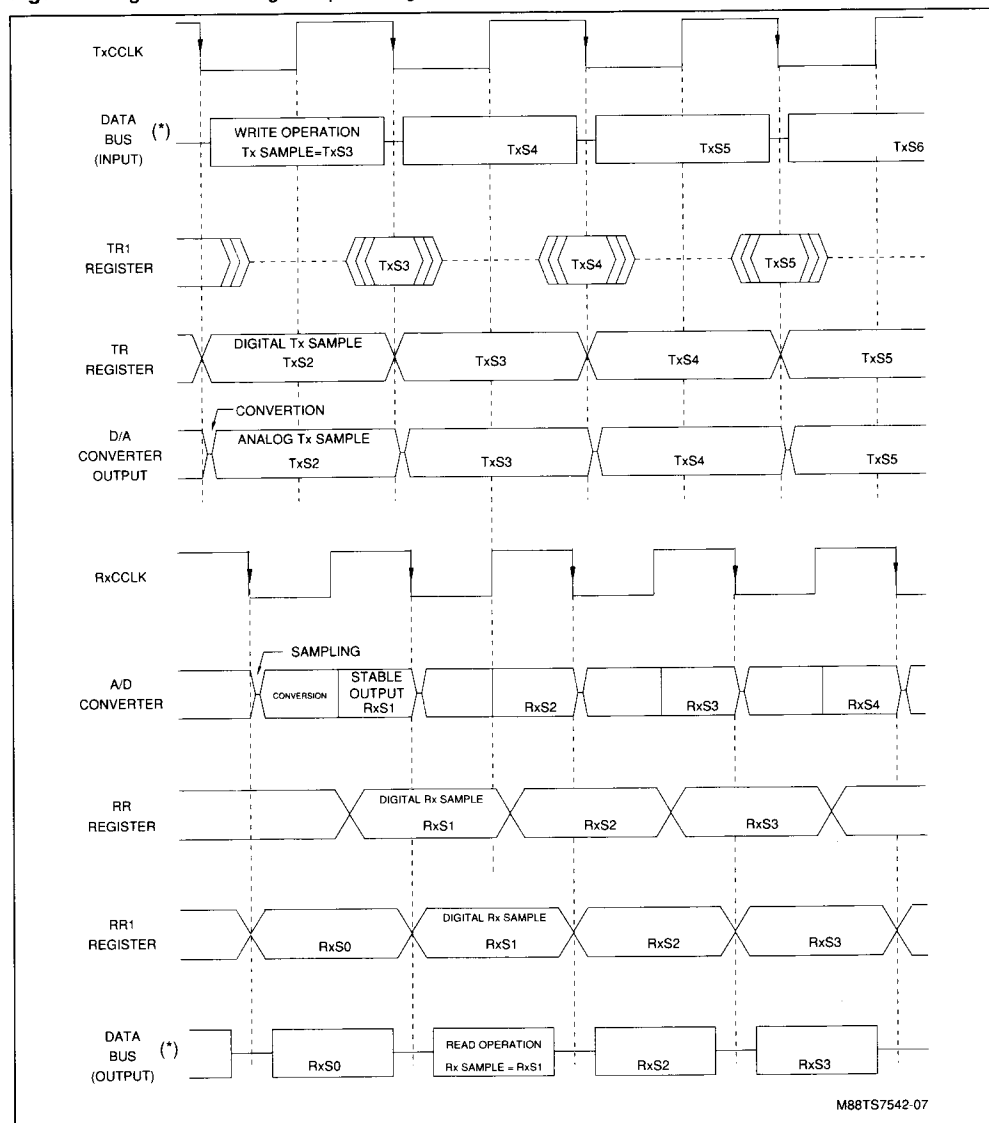


PROGRESSION OF SIGNAL SAMPLES

Fig.5 shows the progression in the TS7542 of the digital and analog signal samples. It appears that the transfers of the data representing the transmit and the receive signals have to be synchronized on

the TxCCLK or the RxCCLK conversion clock, respectively. This is the reason why the DSP needs to receive these clock signals or to read their status from the dedicated registers.

Figure 5 : Digital and Analog Samples Progress.



Notes : Txi = ith analog or digital sample of the Tx signal.

Rxi = ith analog or digital sample of the Rx signal.

(*) Data can be written (read) six master clock periods after the Tx x CCLK (Rx x CCLK) negative-going transition respectively

PROGRAMMABLE FUNCTIONS

Table 4 : Bit Clock Frequency Programming (Tx and Rx).

| | RC1 Register | | | | | | | | TxCLK or RxCLK Bit Clock Nominal Frequency (Hz) | Communication Standard |
|-----|--------------|-----|-----|-----|-----|----|----|----|-------------------------------------------------------|---------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | HB3 | HB2 | HB1 | HR2 | HR1 | — | — | — | | |
| | 0 | 0 | 0 | | | | | | 9600 | V.29 |
| | 0 | 0 | 1 | | | | | | 4800 | V.27 |
| | 0 | 1 | 0 | | | | | | 2400 | V.22 bis, V.26 |
| | 0 | 1 | 1 | | | | | | 1200 | V.22, BELL 212A |
| | 1 | 0 | 0 | | | | | | 600 | V.22 Fall-back |
| | 1 | 0 | 1 | | | | | | 600 | " |
| | 1 | 1 | 0 | | | | | | 2400 | V.22 bis, V.26 |
| P/O | 1 | 1 | 1 | | | | | | 1200 | V.22, BELL 212A |

P/O : Power on status.

Table 5 : Baud Rate Clock Frequency Programming (Tx and Rx).

| | RC1 Register | | | | | | | | TxRCLK or RxBCLK Baud Rate Clock Nominal Frequency(Hz) | Communication Standard (note 3) |
|-----|--------------|-----|-----|-----|-----|----|----|----|-----------------------------------------------------------------|------------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | HB3 | HB2 | HB1 | HR2 | HR1 | — | — | — | | |
| | | | | 0 | 0 | | | | 2400 | V.29, V.33 |
| | | | | 0 | 1 | | | | 1600* | V.27* |
| | | | | 1 | 0 | | | | 1200 | V.26 |
| P/O | | | | 1 | 1 | | | | 600 | V.22, V.22 Bis, BELL 212A |

Note 3 : The phase shift frequency of the transmit DPLL is 600 Hz, excepted for (*) 800 Hz.

Table 6 : Conversion Clock Frequency Programming (Tx and Rx).

| | RC2 Register | | | | | | | | TxCCLK or RxCLK Conversion (sampling) Clock Nominal Frequency(Hz) | Communication Standard |
|-----|--------------|----|----|-----|-----|------|------|----|-------------------------------------------------------------------------------|---------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | — | — | — | HS2 | HS1 | HTHR | FCLK | — | | |
| | | | | 0 | 0 | | | | 9600 | |
| | | | | 0 | 1 | | | | 8000 | V.27 |
| | | | | 1 | 0 | | | | 7200 | |
| P/O | | | | 1 | 1 | | | | 7200 | |

Table 7 : Tx Synchronization Signal Programming.

| | RC2 Register | | | | | | | | Selected Synchronisation Signal |
|-----|--------------|----|----|-----|-----|------|------|----|---------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | — | — | — | HS2 | HS1 | HTHR | FCLK | — | |
| | | | | | | 0 | 0 | | RxCLK |
| | | | | | | 1 | 0 | | TxSCLK (note 4) |
| P/O | | | | | | X | 1 | | Transmit DPLL free-runs |

Note 4 : The Tx DPLL free runs if there is no transition on this pin in that case.
X = Don't care value.

Table 8 : Tx Clock General Reset.

| RC8 Register (note 5) | | | | | | | | Resetting Transition |
|-----------------------|-----|------|-----|----|----|----|----|--------------------------------------------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| MPE | SPR | AVRE | VAL | — | — | — | — | |
| 1 | 0 | 0 | 0 | | | | | Next Negative-going Transition of Synchronizing Signal |

Note 5 : RC8 register is cleared after the programmed control operation is completed and on power-on.

Table 9 : Rx Clock Phase Shift Programming.

| RC8 Register (note 5) | | | | | | | Action on RxDPPL |
|-----------------------|-----|------|-----|----|----|----|-------------------------------------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| MPE | SPR | AVRE | VAL | — | — | — | |
| 0 | 1 | 0 | 0 | | | | Phase Lag of Programmed Amplitude |
| 0 | 0 | 0 | 1 | | | | Phase Lag of Two 5.76 MHz Master Clock Periods |
| 0 | 0 | 1 | 1 | | | | Phase Lead of Two 5.76 MHz Master Clock Periods |

Note 5 : RC8 register is cleared after the programmed control operation is completed and on power-on.

Table 10 : Rx Clock Phase Shift Amplitude Programming.

| | RC7 Register | | | | | | | Phase Shift in Degrees | | Number of Master Clock Pulses Suppressed |
|-----|--------------|-----|-----|-----|-----|----|----|------------------------|------------|------------------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | |
| | SP5 | SP4 | SP3 | SP2 | SP1 | — | — | 1200 Bauds* | 1600 Bauds | |
| 0 | 0 | 0 | 0 | 0 | 0 | | | 1.5 | 2 | 20 |
| 0 | 0 | 0 | 0 | 0 | 1 | | | 3 | 4 | 40 |
| 0 | 0 | 0 | 0 | 1 | 0 | | | 4.5 | 6 | 60 |
| 0 | 0 | 0 | 0 | 1 | 1 | | | 6 | 8 | 80 |
| 0 | 0 | 1 | 0 | 0 | 0 | | | 7.5 | 10 | 100 |
| 0 | 0 | 1 | 0 | 0 | 1 | | | 9 | 12 | 120 |
| 0 | 0 | 1 | 1 | 0 | 0 | | | 10.5 | 14 | 140 |
| 0 | 0 | 1 | 1 | 1 | 1 | | | 12 | 16 | 160 |
| 0 | 1 | 0 | 0 | 0 | 0 | | | 13.5 | 18 | 180 |
| 0 | 1 | 0 | 0 | 0 | 1 | | | 15 | 20 | 200 |
| 0 | 1 | 0 | 1 | 0 | 0 | | | 16.5 | 22 | 220 |
| 0 | 1 | 0 | 1 | 1 | 1 | | | 18 | 24 | 240 |
| 0 | 1 | 1 | 0 | 0 | 0 | | | 19.5 | 26 | 260 |
| 0 | 1 | 1 | 0 | 0 | 1 | | | 21 | 28 | 280 |
| 0 | 1 | 1 | 1 | 0 | 0 | | | 22.5 | 30 | 300 |
| 0 | 1 | 1 | 1 | 1 | 1 | | | 24 | 32 | 320 |
| 1 | 0 | 0 | 0 | 0 | 0 | | | 22.5 | 30 | 300 |
| 1 | 0 | 0 | 0 | 0 | 1 | | | 45 | 60 | 600 |
| 1 | 0 | 0 | 0 | 1 | 0 | | | 67.5 | 90 | 900 |
| 1 | 0 | 0 | 0 | 1 | 1 | | | 90 | 120 | 1200 |
| 1 | 0 | 1 | 0 | 0 | 0 | | | 112.5 | 150 | 1500 |
| 1 | 0 | 1 | 0 | 0 | 1 | | | 135 | 180 | 1800 |
| 1 | 0 | 1 | 1 | 0 | 0 | | | 157.5 | 210 | 2100 |
| 1 | 0 | 1 | 1 | 1 | 1 | | | 180 | 240 | 2400 |
| 1 | 1 | 0 | 0 | 0 | 0 | | | 202.5 | 270 | 2700 |
| 1 | 1 | 0 | 0 | 0 | 1 | | | 225 | 300 | 3000 |
| 1 | 1 | 0 | 0 | 1 | 0 | | | 247.5 | 330 | 3300 |
| 1 | 1 | 0 | 0 | 1 | 1 | | | 270 | 360 | 3600 |
| 1 | 1 | 1 | 0 | 0 | 0 | | | 292.5 | | 3900 |
| 1 | 1 | 1 | 0 | 0 | 1 | | | 315 | | 4200 |
| 1 | 1 | 1 | 1 | 0 | 0 | | | 337.5 | | 4500 |
| 1 | 1 | 1 | 1 | 1 | 0 | | | 360 | | 4800 |
| P/O | 1 | 1 | 1 | 1 | 1 | | | | | |

(*) 2400 bauds : multiply by two. 600 bauds : divide by two.

Table 11 : Tx Attenuator Programming.

| | RC4 Register | | | | | | | | Attenuation (dB) |
|-----|--------------|------|------|------|----|-----|-----|----|------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | ATT4 | ATT3 | ATT2 | ATT1 | – | EM2 | EM1 | – | |
| 0 | 0 | 0 | 0 | 0 | | | | | 0 |
| 0 | 0 | 0 | 0 | 1 | | | | | 2 |
| 0 | 0 | 1 | 0 | | | | | | 4 |
| 0 | 0 | 1 | 1 | | | | | | 6 |
| 0 | 1 | 0 | 0 | | | | | | 8 |
| 0 | 1 | 0 | 1 | | | | | | 10 |
| 0 | 1 | 1 | 0 | | | | | | 12 |
| 0 | 1 | 1 | 1 | | | | | | 14 |
| 1 | 0 | 0 | 0 | | | | | | 16 |
| 1 | 0 | 0 | 1 | | | | | | 18 |
| 1 | 0 | 1 | 0 | | | | | | 20 |
| 1 | 0 | 1 | 1 | | | | | | 22 |
| P/O | 1 | 1 | X | X | | | | | Infinite |

X = Don't care value.

Table 12 : EXI and AGC1 Inputs Programming.

| | RC4 Register | | | | | | | | EXI Input Status | AGC1 Input Status |
|-----|--------------|------|------|------|----|-----|-----|----|-----------------------------|-----------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | ATT4 | ATT3 | ATT2 | ATT1 | – | EM2 | EM1 | – | | |
| | | | | | | 0 | 0 | | Disabled | Tied to AGC Amplifier Input |
| | | | | | | 0 | 1 | | Tied to Tx Filter Input | " |
| | | | | | | 1 | 0 | | Tied to Tx Attenuator Input | " |
| P/O | | | | | | 1 | 1 | | Disabled | Tied to A/DC Input |

Table 13 : Rx Filter Programming.

| | RC3 Register | | | | Sampling (Fs) and Cut-off (Fc) Frequencies (note 6) | | | | Communication Standard | See Figure N° |
|-----|--------------|-----|-----|-----|-----------------------------------------------------|--------|-------------------|--------|-------------------------------------------------------------|---------------|
| | D7 | D6 | D5 | D4 | Low Pass Section | | High Pass Section | | | |
| | RF3 | RF2 | RF1 | RF0 | Fs(kHz) | Fc(Hz) | Fs(kHz) | Fc(Hz) | | |
| P/O | 0 | 0 | 0 | X | 288 | 3200 | 144 | 1820 | V.22, V.22 bis, BELL 212A and BELL 103 High Channels | 7 |
| | 0 | 0 | 1 | X | 192 | 2133 | 115.2 | 1456 | V.21 High Channel | 8 |
| | 0 | 1 | 0 | X | 288 | 3200 | 82.3 | 1040 | V.27 ter 2400 bps | 9 |
| | 0 | 1 | 1 | X | 288 | 3200 | 72 | 910 | V.27 ter 4800 bps, V.23, V.26 and BELL 202 | 10 |
| | 1 | 0 | 0 | 0 | 144 | 1600 | 64 | 809 | V.22, V.22 bis, BELL 212A and BELL 103 Low Channels | 11 |
| | 1 | 0 | 0 | 1 | 144 | 1600 | 64 | 809 | V.22, V.22 bis Low Channels with 1800 Hz Tone Rejection (*) | 12 |
| | 1 | 0 | 1 | X | 115.2 | 1280 | 64 | 809 | V.21 Low Channel | 13 |
| | 1 | 1 | 0 | X | 288 | 3200 | 36 | 455 | V.29, V.33 | 14 |
| | 1 | 1 | 1 | X | 288 | 3200 | 18 | 228 | Full Channel Bandwidth | 15 |
| | 1 | 1 | 1 | X | 48 | 533 | 27.4 | 347 | 75 bps Back Channel | 16 |

(*) In this mode the 1800 Hz notch filter section is enabled.

X = Don't care values. The notch section is disabled in all these cases.

Note 6 : The sampling clocks used by the Rx switched capacitor filters are straightly derived from the crystal oscillator. The Tx switched capacitor filter is driven from the Tx DPLL.

Table 14.

| | RC3 Register | | | | | | | | Rx Filter Gain (dB) |
|-----|--------------|-----|-----|-----|------|------|------|------|---------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | RF3 | RF2 | RF1 | RF0 | RFG2 | RFG1 | LAT2 | LAT1 | |
| P/O | | | | | 0 | 0 | | | 0 |
| | | | | | 0 | 1 | | | 3 |
| | | | | | 1 | 0 | | | 6 |
| | | | | | 1 | 1 | | | 9 |

Table 15 : Line Output Attenuator Programming.

| | RC3 Register | | | | | | | | LAO Output Attenuation (dB) |
|-----|--------------|-----|-----|-----|------|------|------|------|-----------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | RF3 | RF2 | RF1 | RF0 | RFG2 | RFG1 | LAT2 | LAT1 | |
| P/O | | | | | | | 0 | 0 | Infinite |
| | | | | | | | 0 | 1 | 0 |
| | | | | | | | 1 | 0 | 6 |
| | | | | | | | 1 | 1 | 12 |

Table 16 : Carrier Level Detector Programming.

| | RC6 Register | | | | | | | | Carrier Level Detector Threshold(dBm) (note 7) |
|-----|--------------|------|-----|----|----|----|----|----|---------------------------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | CDG2 | CDG1 | CDH | – | – | – | – | – | |
| P/O | 0 | 0 | 0 | | | | | | – 29.85 |
| | 0 | 0 | 1 | | | | | | – 27.35 |
| | 0 | 1 | 0 | | | | | | – 36.65 |
| | 0 | 1 | 1 | | | | | | – 34.15 |
| | 1 | 0 | 0 | | | | | | – 46.75 |
| | 1 | 0 | 1 | | | | | | – 44.25 |
| | 1 | 1 | 0 | | | | | | – 46.75 |
| | 1 | 1 | 1 | | | | | | – 44.25 |

Note 7 : These values applies when the total Rx gain from the phone line to the Rx filter output is 0 dB.

Table 17 : AGC Amplifier Gain Programming.

| P/O | RC5 Register | | | | | AGC Amplifier Gain (dB) | |
|-----|--------------|-----|-----|-----|-----|-------------------------|------------|
| | D7 | D6 | D5 | D4 | D3 | AGC1 Input | AGC2 Input |
| | RG5 | RG4 | RG3 | RG2 | RG1 | | |
| P/O | 0 | 0 | 0 | 0 | 0 | 0 | - ∞ |
| | 0 | 0 | 0 | 0 | 1 | | 1.5 |
| | - ∞ | 0 | 0 | 0 | 1 | 0 | 3 |
| | - ∞ | 0 | 0 | 0 | 1 | 1 | 4.5 |
| | - ∞ | 0 | 0 | 1 | 0 | 0 | 6 |
| | - ∞ | 0 | 0 | 1 | 0 | 1 | 7.5 |
| | - ∞ | 0 | 0 | 1 | 1 | 0 | 9 |
| | - ∞ | 0 | 0 | 1 | 1 | 1 | 10.5 |
| | - ∞ | 0 | 1 | 0 | 0 | 0 | 12 |
| | - ∞ | 0 | 1 | 0 | 0 | 1 | 13.5 |
| | - ∞ | 0 | 1 | 0 | 1 | 0 | 15 |
| | - ∞ | 0 | 1 | 0 | 1 | 1 | 16.5 |
| | - ∞ | 0 | 1 | 1 | 0 | 0 | 18 |
| | - ∞ | 0 | 1 | 1 | 0 | 1 | 19.5 |
| | - ∞ | 0 | 1 | 1 | 1 | 0 | 21 |
| | - ∞ | 0 | 1 | 1 | 1 | 1 | 22.5 |
| | - ∞ | 1 | 0 | 0 | 0 | 0 | 24 |
| | - 14.5 | 1 | 0 | 0 | 0 | 1 | 25.5 |
| | - 7.7 | 1 | 0 | 0 | 1 | 0 | 27 |
| | - 3.4 | 1 | 0 | 0 | 1 | 1 | 28.5 |
| | 0 | 1 | 0 | 1 | 0 | 0 | 30 |
| | 2.7 | 1 | 0 | 1 | 0 | 1 | 31.5 |
| | 5.2 | 1 | 0 | 1 | 1 | 0 | 33 |
| | 7.4 | 1 | 0 | 1 | 1 | 1 | 34.5 |
| | 9.5 | 1 | 1 | 0 | 0 | 0 | 36 |
| | 11.4 | 1 | 1 | 0 | 0 | 1 | 37.5 |
| | 13.3 | 1 | 1 | 0 | 1 | 0 | 39 |
| | 15.1 | 1 | 1 | 0 | 1 | 1 | 40.5 |
| | 16.8 | 1 | 1 | 1 | 0 | 0 | 42 |
| | 18.5 | 1 | 1 | 1 | 0 | 1 | 43.5 |
| | 20.2 | 1 | 1 | 1 | 1 | 0 | 45 |
| | 21.8 | 1 | 1 | 1 | 1 | 1 | 46.5 |

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = +5\text{ V}$, $V^- = -5\text{ V}$ and $t_{\text{amb}} = 25\text{ }^{\circ}\text{C}$.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------|---------------------------------------------|----------------------------|--------------------|
| | DGND Digital Ground to AGND Analog Ground | - 0.3 to + 0.3 | V |
| | V^+ Supply Voltage to DGND or AGND Ground | - 0.3 to + 7 | V |
| | V^- Supply Voltage to DGND or AGND Ground | - 7 to + 0.3 | V |
| V_I | Voltage at any Digital Input or Output | DGND - 0.3 to $V^+ + 0.3$ | V |
| I_I | Digital Output Current | - 20 to + 20 | mA |
| V_{in} | Voltage at any Input or Output | $V^- - 0.3$ to $V^+ + 0.3$ | V |
| I_{out} | Analog Output Current | - 10 to + 10 | mA |
| P_{tot} | Power Dissipation | 500 | mW |
| t_{amb} | Operating Temperature Range | 0 to + 70 | $^{\circ}\text{C}$ |
| t_{stot} | Storage Temperature Range | - 65 to + 150 | $^{\circ}\text{C}$ |
| t_{sold} | Pin Temperature (soldering 10 s.) | + 260 | $^{\circ}\text{C}$ |

POWER SUPPLIES

DGND = AGND = 0 V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|------------------------------------------------------|--------|------|--------|------|
| V^+ | Positive Power Supply | 4.75 | | 5.25 | V |
| V^- | Negative Power Supply | - 5.25 | | - 4.75 | V |
| I^+ | Positive Supply Current (receive signal level 0 dBm) | | | 35 | mA |
| I^- | Negative Supply Current (receive signal level 0 dBm) | - 35 | | | mA |

DIGITAL INTERFACE

Control Inputs, Data Bus and Clock Outputs. Voltages referenced to DGND = 0 V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------------------------------------|-----------------------------------------------------------------------------|------|------|------|---------------|
| V_{IL} | Low Level Input Voltage | | | 0.8 | V |
| V_{IH} | High Level Input Voltage | 2.2 | | | V |
| I_{IL} | Low Level Input Current DGND < V_I < 0.8 V | - 10 | | 10 | μA |
| I_{IH} | High Level Input Current 2.2 V < V_I < V^+ | - 10 | | 10 | μA |
| V_{OL} | Low Level Output Voltage ($I_{\text{OL}} = 2.5\text{ mA}$) | | | 0.4 | V |
| V_{OH} | High Level Output Voltage ($I_{\text{OH}} = - 2.5\text{ mA}$) | 2.4 | | | V |
| I_{OZ} | High Impedance Output Current (when E is high and DGND < V_O < V^+) | - 50 | | 50 | μA |
| Crystal Oscillator Interface (XTAL1 input) | | | | | |
| V_{IL} | Low Level Input Voltage | | | 1.5 | V |
| V_{IH} | High Level Input Voltage | 3.5 | | | V |
| I_{IL} | Low Level Input current DGND $\leq V_I \leq V_{\text{ILmax}}$ | - 15 | | | μA |
| I_{IH} | High Level Input Current $V_{\text{IHmin}} \leq V_I \leq V^+$ | | | 15 | μA |

ELECTRICAL SPECIFICATIONS (continued)

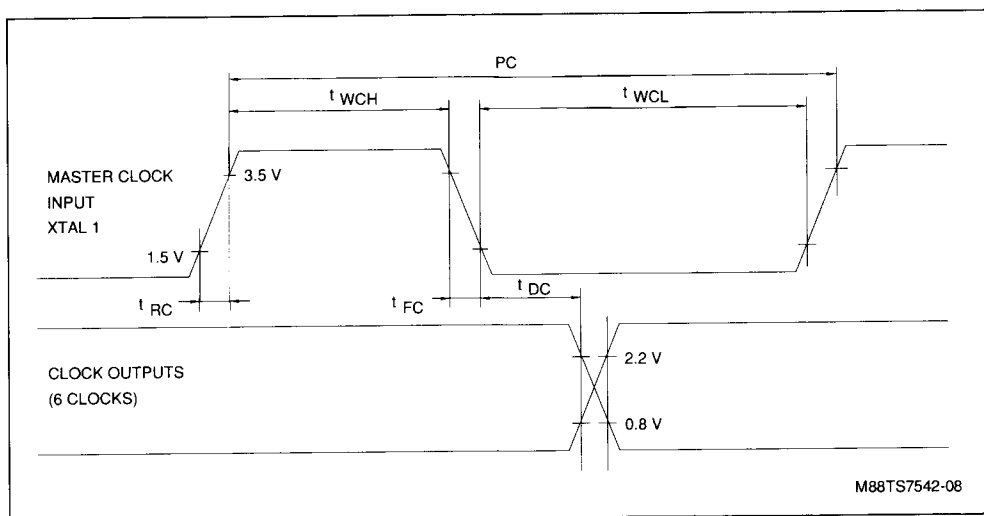
ANALOG INTERFACE All voltages referenced to AGND = 0 V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|------------------------------------------------------------------------------|-------|------|---------------|------------------|
| V_{in} | Input Voltage EXI, DXI, RAI | - 2.5 | | 2.5 | V |
| I_{in} | Input Current EXI, DXI, RAI ($-2.5\text{ V} < V_{in} < 2.5\text{ V}$) | - 1 | | 1 | μA |
| R_{in} | Input Resistance AGC1, AGC2 | 1.5 | | | $\text{k}\Omega$ |
| R_{in} | Input Resistance CD1 | 0.7 | | | $\text{k}\Omega$ |
| V_{out} | Output Voltage ATO, LAO, RFO $R_L = 1\text{ k}\Omega$, $C_L = 50\text{ pF}$ | - 2.5 | | 2.5 | V |
| R_{out} | Output Resistance ATO LAO RFO | | | 4 50 15 | Ω |
| R_L | Load Resistance ATO, RFO | 1 | | | $\text{k}\Omega$ |
| C_L | Load Capacitance ATO, RFO | | | 50 | pF |
| R_L | Load Resistance LAO | 10 | | | $\text{k}\Omega$ |
| C_L | Load Capacitance LAO | | | 20 | pF |

TIMING SPECIFICATIONS

TIMING SPECIFICATIONS Clock Timing Characteristics (XTAL1 input)

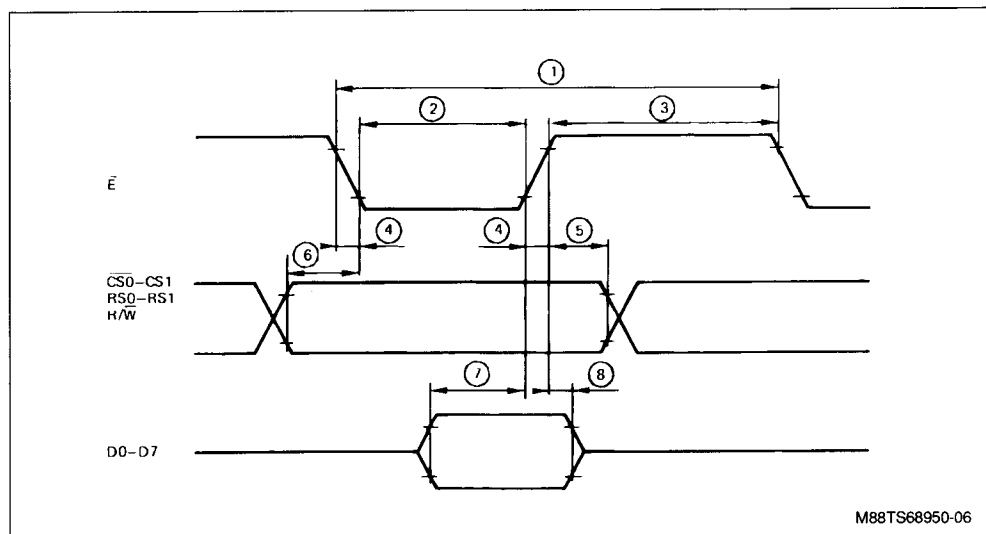
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------|------|-------|------|------|
| PC | Master Clock Period | | 173.6 | | ns |
| t_{WCL} | Master Clock Width Low Level | 50 | | | ns |
| t_{WCH} | Master Clock Width High Level | 50 | | | ns |
| t_{RC} | Master Clock Rise Time | | | 50 | ns |
| t_{FC} | Master Clock Fall Time | | | 50 | ns |
| t_{DC} | Clock Output Delay Time $C_L = 50\text{ pF}$ | | | 500 | ns |
| t_{TC} | Clock Output Transition Time $C_L = 50\text{ pF}$ | | | 100 | ns |



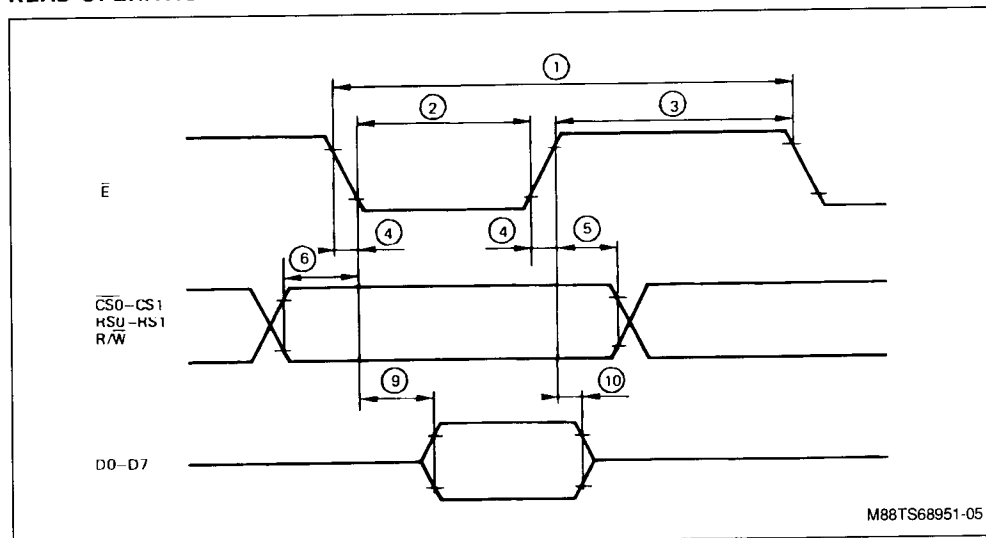
ELECTRICAL SPECIFICATIONS (continued)

BUS TIMING CHARACTERISTICS (see foot notes 1 and 2 on timing diagrams)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------|----------------------------------------------------------------|------|------|------|------|
| t_{CYC} | Cycle Time (1) | 320 | | | ns |
| t_{WEL} | Pulse Width \bar{E} Low Level (2) | 180 | | | ns |
| t_{WEH} | Pulse Width \bar{E} High Level (3) | 100 | | | ns |
| t_r, t_f | Clock Rise and Fall Time (4) | | | 20 | ns |
| t_{HCE} | Control Signal Hold Time (5) | 10 | | | ns |
| t_{SCE} | Control Signal Set-up Time (6) | 40 | | | ns |
| t_{SDI} | Input Data Set-up Time (7) | 120 | | | ns |
| t_{HDI} | Input Data Hold Time (8) | 10 | | | ns |
| t_{SDO} | Output Data Set-up Time (1 TTL load and $CL = 50$ pF) | | | 150 | ns |
| t_{dz} | Output High Impedance Delay Time (1 TTL load and $CL = 50$ pF) | | | 80 | ns |

WRITE OPERATION**Note 1 :** Voltage levels shown are $V_{IL} < 0.4$ V, $V_{IH} > 2.4$ V, unless otherwise specified.**Note 2 :** Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

READ OPERATION



Note 1 : Voltage levels shown are $V_{IL} < 0.4 \text{ V}$, $V_{IH} > 2.4 \text{ V}$, unless otherwise specified.

Note 2 : Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

TRANSMISSION CHARACTERISTICS

PERFORMANCES OF THE WHOLE TRANSMISSION CHAIN (Input TR1, Output ATO)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|----------------------------------------------------------------------------------------------------|-------|------|------|---------------|
| G_{abs} | ATO Absolute Gain at 1 kHz | - 0.5 | 0 | 0.5 | dB |
| N | ATO Psophometric Noise | | | 100 | μV |
| $PSRR^+$ | ATO Positive Power Supply Rejection Ratio $V_{ac} = 200 \text{ mV}_{pp}$ $f = 1 \text{ kHz}$ | | 40 | | dB |
| $PSRR^-$ | ATO Negative Power Supply Rejection Ratio $V_{ac} = 200 \text{ mV}_{pp}$ $f = 1 \text{ kHz}$ | | 40 | | dB |
| THD | Total Harmonic Distortion | | | - 54 | dB |

DAC TRANSFER CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------|----------------------------------------------------|------|---------|-----------|------|
| | Converter Resolution | | 12 | | Bit |
| $V_{out(max)}$ | Nominal Output Peak to Peak Amplitude | | 5.0 | | V |
| LSB | Least Significant Bit Amplitude | | 1.2 | | mV |
| E_{il} | Integral Linearity Error Relative to Best Fit Line | | ± 4 | ± 8 | LSB |
| E_{dl} | Differential Linearity Error | | | ± 0.7 | LSB |

TRANSMISSION CHARACTERISTICS

TRANSMIT FILTER TRANSFER CHARACTERISTICS (input EX1, output ATO)
(see figure 6)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|---------------------------------|----------------------------|
| G_{abs} | Absolute Gain at 1 kHz | - 0.3 | 0 | 0.3 | dB |
| G_{rel} | Gain Relative to G_{abs} without Sin x/x Correction of DAC Sampling Below 3100 Hz 3200 Hz 4000 Hz 5000 Hz to 12000 Hz 12000 Hz and Above | - 0.4 - 3 | | 0.3 - 36 - 46 - 50 | dB dB dB dB dB |
| T_{gp} | Group Propagation Delay Time ($f = 1800$ Hz) | | 250 | | μ s |
| T_{gpd} | Group Propagation Delay Time Distortion ($600 \text{ Hz} < f < 3000 \text{ Hz}$) | | 430 | | |

Tx ATTENUATOR TRANSFER CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------|--------------------------------------------|-------|------|------|------|
| AT_{abs} | Absolute Attenuation at 0 dB Nominal Value | - 0.3 | 0 | 0.3 | dB |
| AT_{rel} | Attenuation Relative to Nominal Value | - 0.5 | | 0.5 | dB |
| AT_{max} | Maximum Attenuation | 50 | | | dB |

RECEPTION CHARACTERISTICS

PERFORMANCE OF THE WHOLE RECEPTION CHAIN (input RAI or Dx1, output RR1)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|------------|
| G_{abs} | Absolute Gain (AGC gain = 0 dB, RxCLK = 9600 Hz, $V_{in} = 775 \text{ mVrms}$, $f = 2000 \text{ Hz}$) | - 0.5 | 0 | 1.5 | dB |
| HD_T | Total Harmonic Distortion (AGC gain = 0 dB, RxCLK = 9600 Hz, $V_{in} = 775 \text{ mVrms}$, $f = 2000 \text{ Hz}$, programmed band = 475 Hz - 3200 Hz) | | | - 54 | dB |
| N | Equivalent RMS Noise (see note) (AGC gain = 0 dB, RAI, Dx1 tied to AGND, frequency band = 228 Hz - 3200 Hz) | | | 800 | μ Vrms |

Note : Noise depends on AGC gain value.

RECEPTION CHARACTERISTICS (continued)

RECEIVE BAND-PASS FILTER AND REJECTION FILTER (input RAI or Dxl, output RFO)

The characteristics and specifications (templates) of the ten programmable transfer functions are given on figures 7 to 16.

RECEIVE FILTER INPUT GAIN CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|----------------------------------|-------|------|------|------|
| G_{rel} | Relative Gain to Programmed Gain | - 0.5 | | 0.5 | dB |

LINE MONITORING ATTENUATOR CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------|-----------------------------------------------------------------------------------|-------|------|------|------|
| AT_{abs} | Absolute Attenuation at 0 dB Nominal Value | - 0.3 | 0 | 0.3 | dB |
| AT_{rel} | Attenuation Relative to Nominal Value ($2\text{ dB} \leq AT \leq 22\text{ dB}$) | - 0.5 | | 0.5 | dB |
| AT_{max} | Maximum Attenuation ($AT = \infty$) | 50 | | | dB |

AGC AMPLIFIER AND A/D CONVERTER (input AGC1, output RR1)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------------------------------------------------------------------------|--------------|------|----------|----------|
| G_{rel} | Relative Gain to Programmed Gain $0\text{ dB} \leq AGC \leq 24\text{ dB}$ $25.5 \leq AGC \leq 46.5\text{ dB}$ | - 0.5 - 1 | | 0.5 1 | dB dB |
| V_{os} | Offset Voltage | - 70 | | 70 | LSB |

CARRIER LEVEL DETECTOR (input AGC1, output CDR)

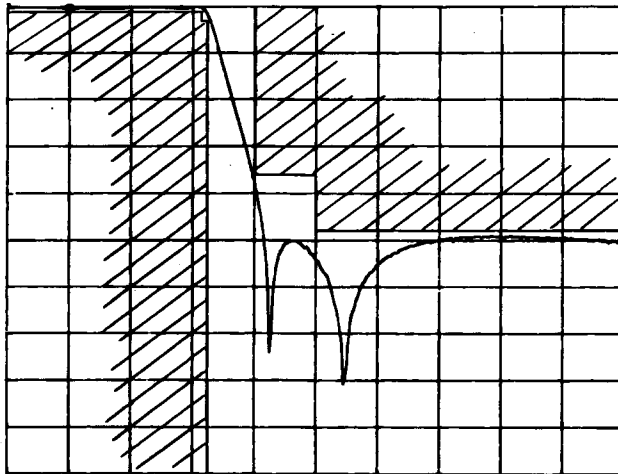
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------------------------------------------------------------------------------|-------------------|------|-------------|----------------|
| T_{rel} | Relative Threshold to Programmed Value T $-36.65 < T \leq -27.35\text{ dBm}$ $-46.75 \leq T \leq -36.65\text{ dBm}$ | 0.5 1 | | 0.5 1 | dB dB |
| H_{yst} | Hysteresis | 2 | | 3 | dB |
| V_{os} | Input Offset Voltage 1st Threshold Pair (see table 16 and fig. 2) 2nd Threshold Pair 3rd Threshold Pair | - 1 - 2 - 3 | | 1 2 3 | mV mV mV |
| T_{dd} | Detection Delay Time 0 mVrms to 775 mVrms Transition or 775 mVrms to 0 mVrms Transition | 1 | | 3 | ms |

PERFORMANCE OF THE A/D CONVERTER (input AGC1, output RR1)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|----------------------------------------------------|-------|---------|-----------|------|
| $V_{in(max)}$ | Input Voltage (peak to peak) | | | 5 | V |
| R_{esh} | A/D Converter Resolution | | | 12 | Bit |
| LSB | Analog Increment | | 1.2 | | mV |
| E_{il} | Integral Linearity Error Relative to Best Fit Line | | ± 4 | ± 8 | LSB |
| E_{dl} | Differential Linearity Error | | | ± 0.7 | LSB |
| V_{os} | Offset Voltage | - 100 | | 100 | LSB |

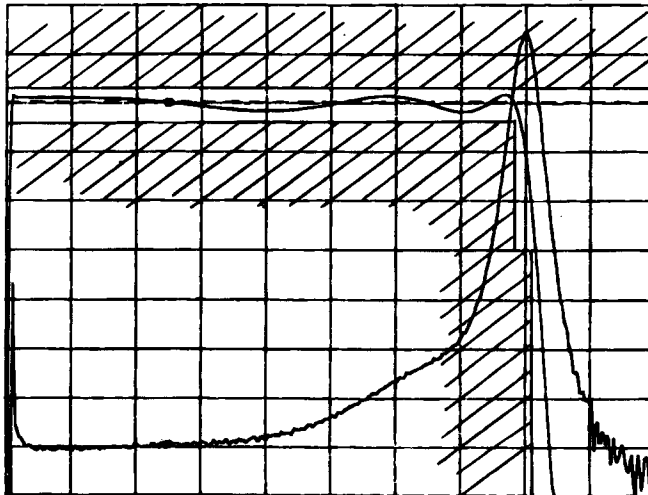
Figure 6 : Tx Filter Frequency Response.

REF LEVEL 0.000dB /DIV 10.000dB MARKER 1 000.000Hz
MAG (UDF) -0.150dB



START 0.000Hz STOP 10 000.000Hz
AMPTD 50.119mV

REF LEVEL -0.150dB /DIV 1.000dB MARKER 1 000.000Hz
MAG (UDF) -0.157dB
400.00μSEC 100.00μSEC MARKER 1 000.000Hz
DELAY (A/R) 205.80μSEC

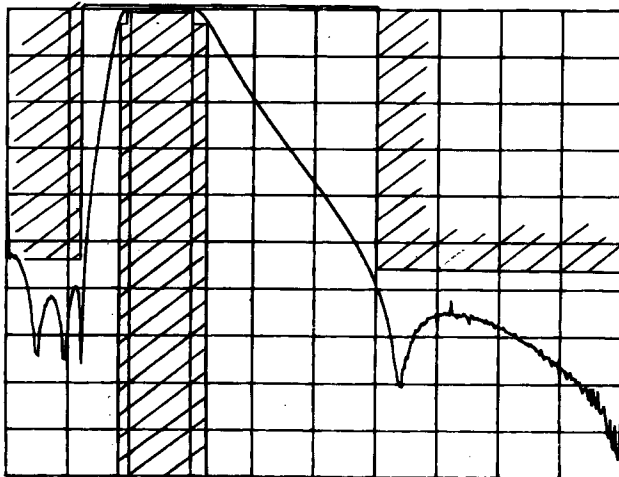


START 0.000Hz STOP 4 000.000Hz
AMPTD 50.119mV DELAY APER 20.00Hz

M88TS7542-09

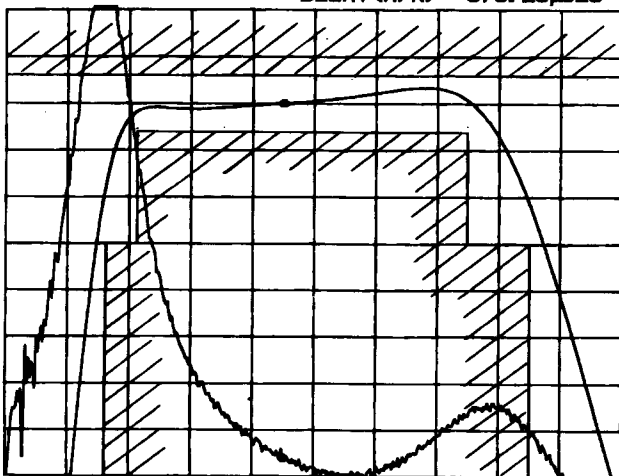
Figure 7 : Rx Filter Frequency Response for V.22, V.22bis, BELL212A and BELL103 High Channels (see table 13).

REF LEVEL 0.000dB /DIV 10.000dB MARKER 2 400.000Hz
MAG (A/R) 0.117dB



START 0.000Hz STOP 10 000.000Hz
AMPTD 199.53mV

REF LEVEL 0.129dB /DIV 1.000dB MARKER 2 400.000Hz
MAG (A/R) 0.138dB
1.1950mSEC 100.00μSEC MARKER 2 400.000Hz
DELAY (A/R) 675.20μSEC

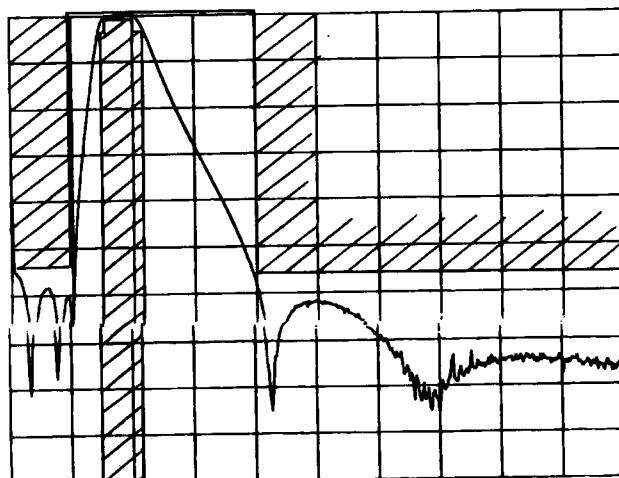


START 1 500.000Hz STOP 3 500.000Hz
AMPTD 100.00mV

M88TS7542-10

Figure 8 : Rx Filter Frequency Response for V.21 High Channel (see table 13).

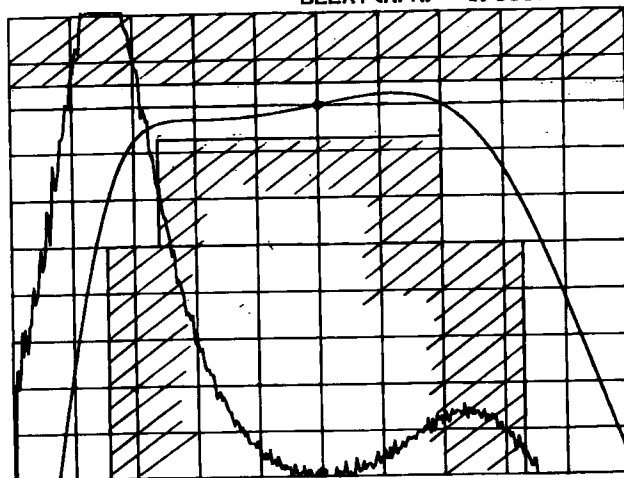
| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 1 | 800.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | 0.079dB |



START 0.000Hz
AMPTD 199.53mV

STOP 10 000.000Hz

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 1 | 800.000Hz |
| 0.100dB | 1.000dB | MAG (A/R) | 0.105dB |
| 1.6000mSEC | 100.00μSEC | MARKER 1 | 800.000Hz |
| | | DELAY (A/R) | 1.1109mSEC |



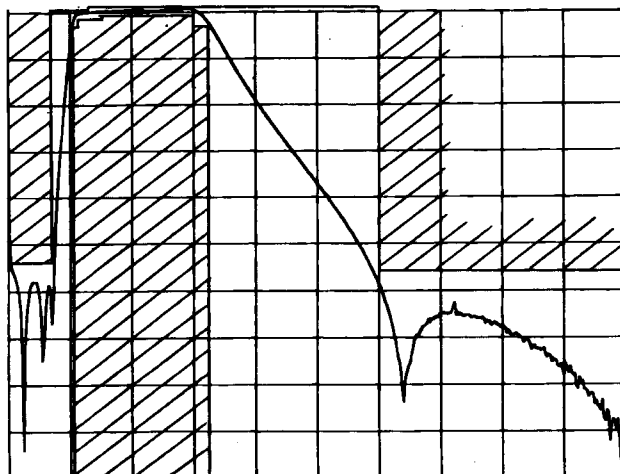
START 1 300.000Hz
AMPTD 100.00mV

STOP 2 300.000Hz

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Figure 9 : Rx Filter Frequency Response for V.27ter 2400bps (see table 13).

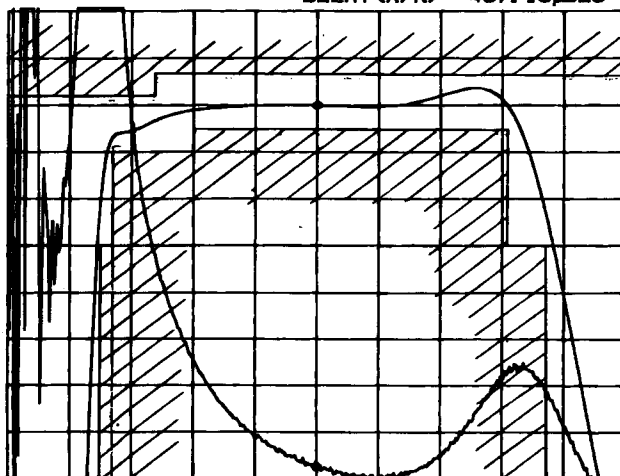
| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 2 | 100.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | 0.383dB |



START 0.000Hz
AMPTD 199.53mV

STOP 10 000.000Hz

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 2 | 100.000Hz |
| 0.380dB | 1.000dB | MAG (A/R) | 0.381dB |
| 970.00μSEC | 100.00μSEC | MARKER 2 | 100.000Hz |
| | | DELAY (A/R) | 497.19μSEC |



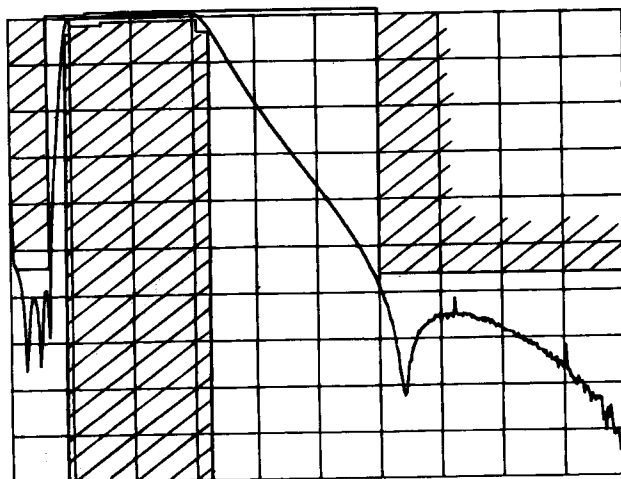
START 800.000Hz
AMPTD 100.00mV

STOP 3 600.000Hz

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Figure 10 : Rx Filter Frequency Response for V.27ter 4800bps, V.23, V.26 and BELL202 (see table 13).

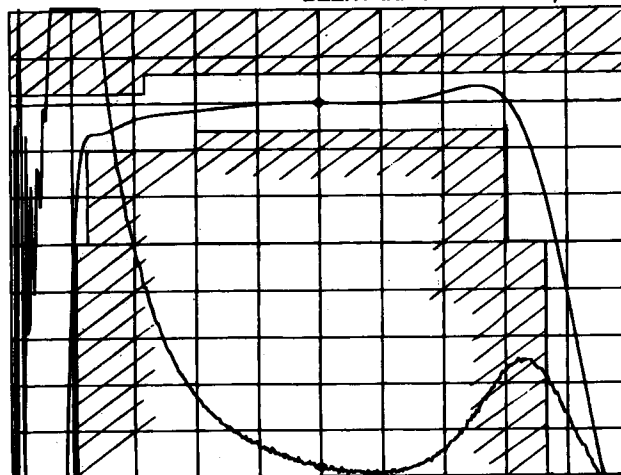
| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 2 | 100.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | 0.509dB |



START 0.000Hz
AMPTD 199.53mV

STOP 10.000.000Hz

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 2 | 100.000Hz |
| 0.480dB | 1.000dB | MAG (A/R) | 0.495dB |
| 950.00μSEC | 100.00μSEC | MARKER 2 | 100.000Hz |
| | | DELAY (A/R) | 471.00μSEC |



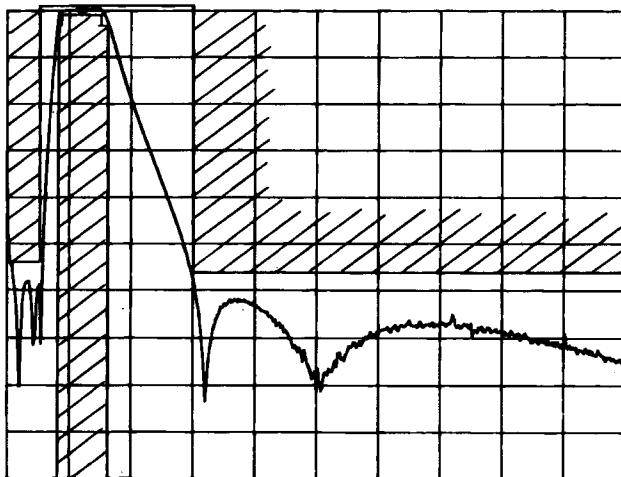
START 800.000Hz
AMPTD 100.00mV

STOP 3.800.000Hz

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Figure 11 : Rx Filter Frequency Response for V.22, V.22bis, BELL212A and BELL103 Low Channel (see table 13).

REF LEVEL 0.000dB /DIV 10.000dB MARKER 1 200.000Hz
MAG (A/R) 0.220dB



START 0.000Hz
AMPTD 199.53mV

STOP 10 000.000Hz

REF LEVEL 0.230dB /DIV 1.000dB MARKER 1 200.000Hz
MAG (A/R) 0.232dB
1.5800mSEC 100.00μSEC MARKER 1 200.000Hz
DELAY (A/R) 1.0805mSEC



START 700.000Hz
AMPTD 100.00mV

STOP 1 700.000Hz
DELAY APER 5.000Hz

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Figure 12 : Rx Filter Frequency Response for V.22 and V.22bis Low Channels with 1800Hz Tone Rejection (see table 13).

REF LEVEL 0.000dB /DIV 10.000dB MARKER 1 200.000Hz
MAG (A/R) 0.429dB



START 0.000Hz
AMPTD 199.53mV

STOP 10 000.000Hz

REF LEVEL 0.430dB /DIV 1.000dB MARKER 1 200.000Hz
1.6250mSEC 100.00μSEC MAG (A/R) 0.439dB
MARKER 1 200.000Hz
DELAY (A/R) 1.1997mSEC



START 700.000Hz
AMPTD 100.00mV

STOP 1 700.000Hz

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Figure 12 (continued) :Rx Filter Frequency Response for V.22 and V.22bis Low Channels with 1800Hz Tone Rejection (see table 13).

REF LEVEL /DIV MARKER 1 800.000Hz
 -30.000dB 2.000dB MAG (A/R) -31.540dB

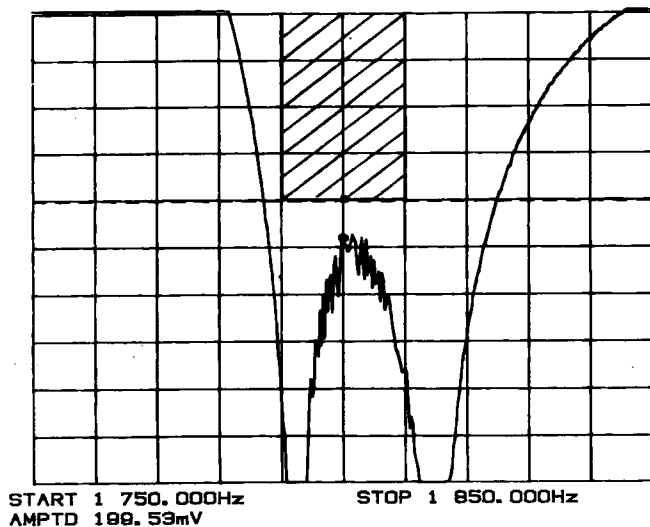
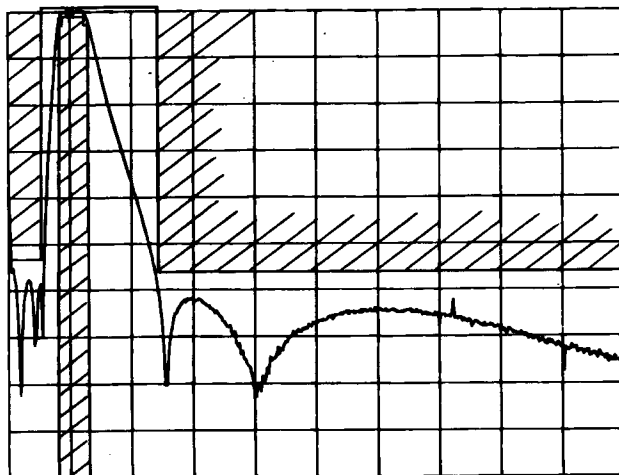


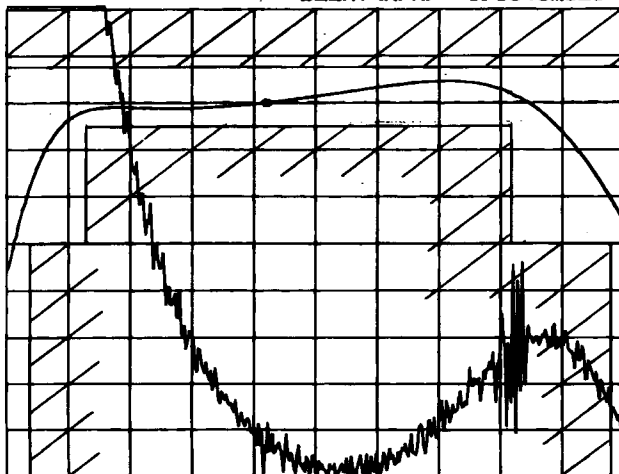
Figure 13 : Rx Filter Frequency Response for V.21 Low Channel (see table 13).

| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 1 | 000.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | -0.033dB |



| | | | |
|-------|----------|------|--------------|
| START | 0.000Hz | STOP | 10 000.000Hz |
| AMPTD | 199.53mV | | |

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 1 | 000.000Hz |
| 0.000dB | 1.000dB | MAG (A/R) | 0.004dB |
| 2.1250mSEC | 100.00μSEC | MARKER 1 | 000.000Hz |
| | | DELAY (A/R) | 1.6848mSEC |



| | | | |
|-------|-----------|------|-------------|
| START | 790.000Hz | STOP | 1 290.000Hz |
| AMPTD | 100.00mV | | |

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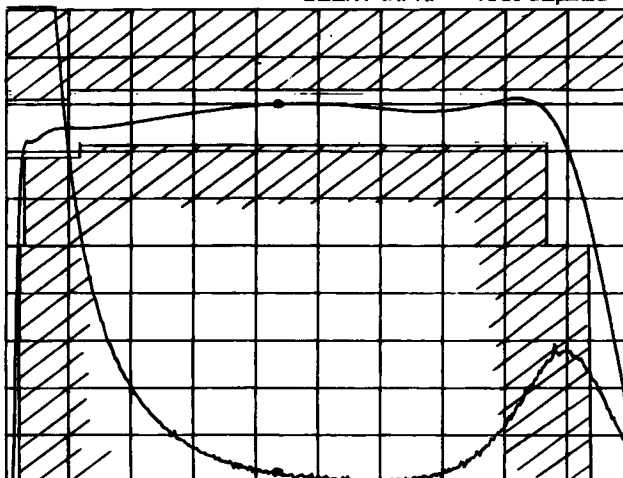
Figure 14 : Rx Filter Frequency Response for V.29 and V.33 (see table 13).

| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 1 | 700.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | 0.749dB |



| | | | |
|-------|----------|------|--------------|
| START | 0.000Hz | STOP | 10.000.000Hz |
| AMPTD | 199.53mV | | |

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 1 | 705.000Hz |
| 0.725dB | 1.000dB | MAG (A/R) | 0.731dB |
| 895.00μSEC | 100.00μSEC | MARKER 1 | 705.000Hz |
| | | DELAY (A/R) | 418.92μSEC |

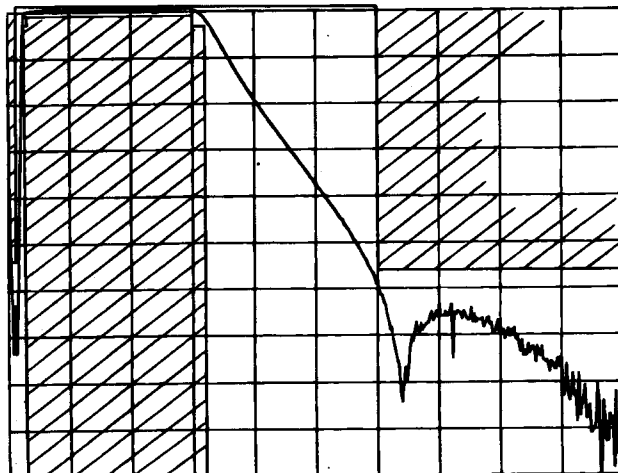


| | | | |
|-------|-----------|------|-------------|
| START | 400.000Hz | STOP | 3.400.000Hz |
| AMPTD | 100.00mV | | |

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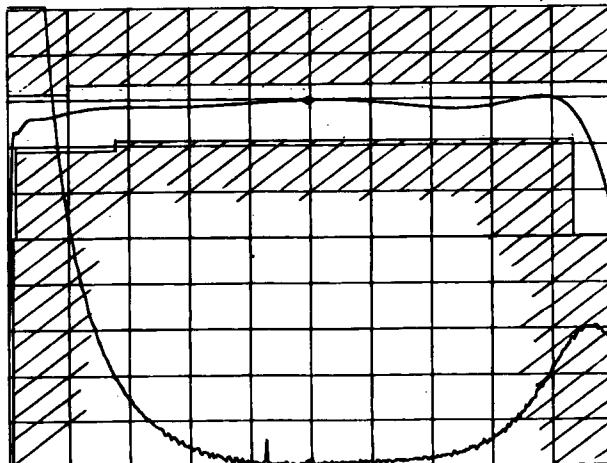
Figure 15 : Rx Filter Frequency Response with Full Channel Bandwidth (see table 13).

| | | | |
|-----------|----------|-----------|-----------|
| REF LEVEL | /DIV | MARKER 2 | 400.000Hz |
| 0.000dB | 10.000dB | MAG (A/R) | 0.484dB |



| | | | |
|-------|----------|------|--------------|
| START | 0.000Hz | STOP | 10 000.000Hz |
| AMPTD | 100.00mV | | |

| | | | |
|------------|------------|-------------|------------|
| REF LEVEL | /DIV | MARKER 1 | 702.550Hz |
| 0.700dB | 1.000dB | MAG (A/R) | 0.682dB |
| 880.00μSEC | 100.00μSEC | MARKER 1 | 702.550Hz |
| | | DELAY (A/R) | 387.39μSEC |

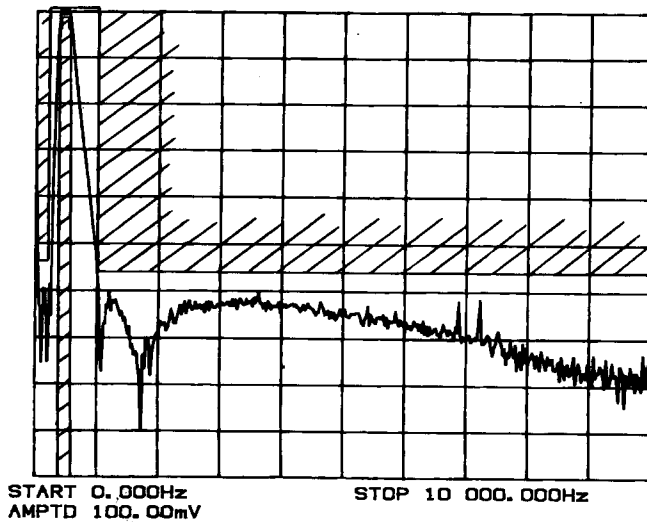


| | | | |
|-------|-----------|------|-------------|
| START | 220.000Hz | STOP | 9 200.000Hz |
| AMPTD | 100.00mV | | |

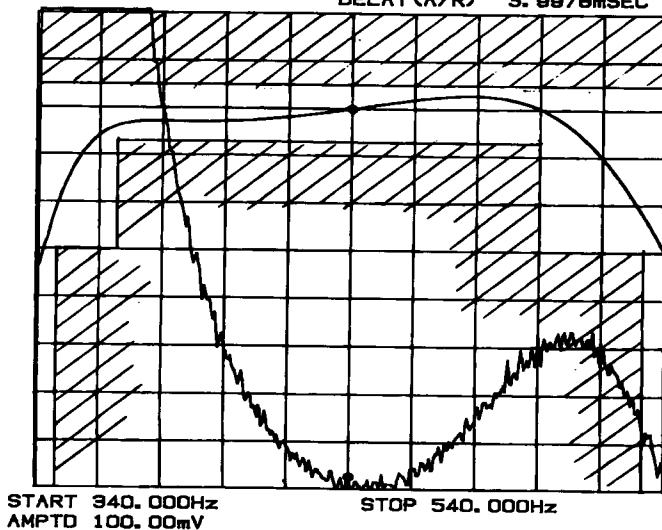
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Figure 16 : Rx Filter Frequency Response for 75bps Back Channel (see table 13).

REF LEVEL 0.000dB /DIV 10.000dB MARKER 450.000Hz
MAG (A/R) 0.090dB



REF LEVEL 0.200dB /DIV 1.000dB MARKER 440.000Hz
MAG (A/R) 0.197dB
4.9450mSEC 200.00μSEC MARKER 440.000Hz
DELAY (A/R) 3.9978mSEC



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